

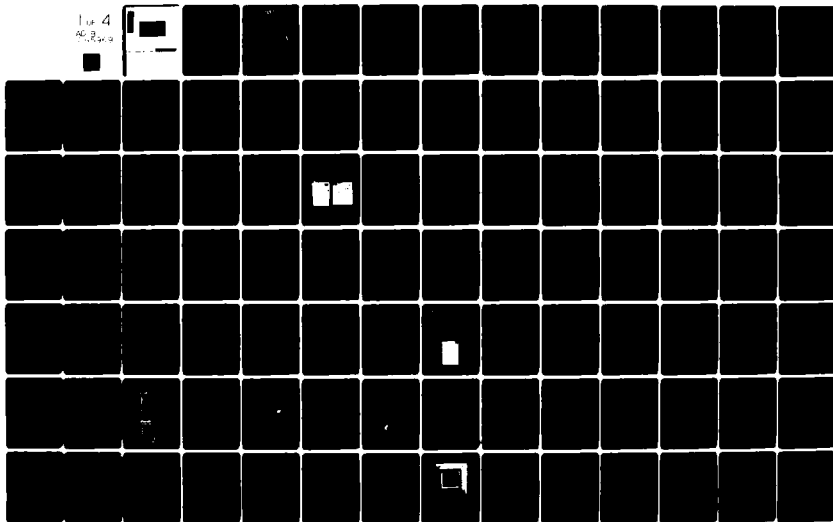
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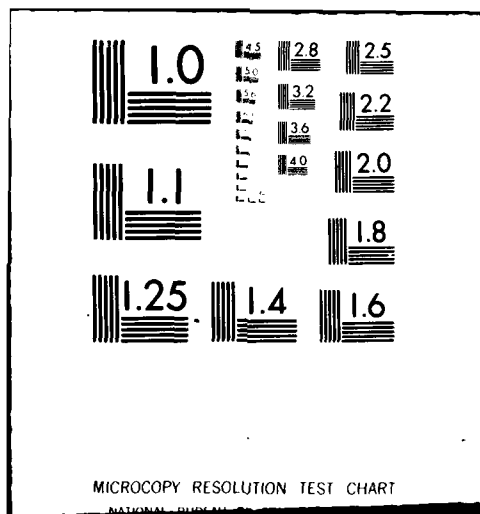
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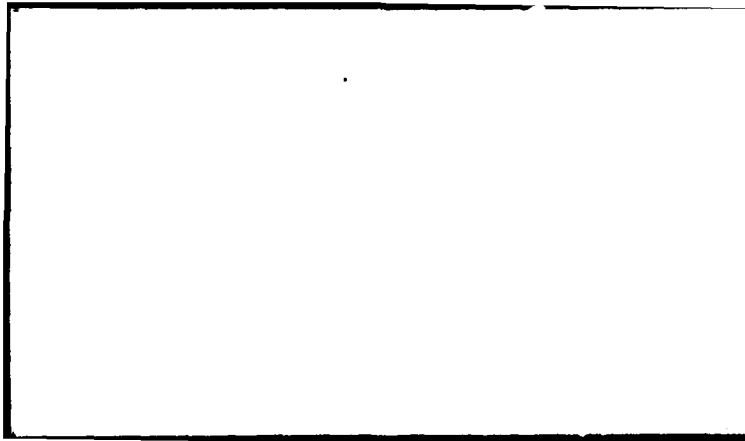
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FINAL REPORT: MX ACT I: FEB 75-JAN 79  
SECTION I  
INTRODUCTION

The objective of the Advanced Computer Technology (ACT) Program was to provide a hardware demonstration of the maturity of critical technologies required to build an advanced missile computer utilizing radiation-hardened CMOS/SOS logic and MNOS/SOS memory devices.

The ACT-I program was sponsored and managed by the Space and Missile Systems Organization (SAMSO), Norton AFB, CA. Two parallel contracts were awarded in February 1975 to Northrop and Rockwell. This report addresses only that effort of Northrop, Electronics Division and our subcontractor Westinghouse, Defense and Electronic Systems Center, Baltimore, MD.

The primary specific goal of this program was to design, process and test four LSIC (Large Scale Integrated Circuit) parts which were representative of those needed for an advanced missile guidance computer. Two LSIC parts were to be appropriated to the CPU (Central Processor Unit) of the computer, and two were to be appropriate to the Memory Unit of the computer. The specific parts are a 4-bit slice GPU (General Processor Unit), a 256 word by 4-bit wide MPRM (Mask Programmable Read-Only Memory), a 256 word by 4-bit wide PSM (nonvolatile slow-write Permanent Store Memory for program store) and a 512 word by 1-bit wide TSM (nonvolatile fast-write Temporary Store Memory for scratchpad/data store). These four LSIC parts were designed, processed and tested on this program. This activity was preceded by a Basic Parts phase. It involved the design, process and evaluation of test vehicles to establish the necessary baseline of design rules and process sequences to meet the performance requirements on the LSIC parts.

## MX ACT I LSIC PARTS

### CMOS/SOS Logic Devices

GPU -- 4-bit slice, general processor  
ROM -- 256 x 4 micro program store

### MNOS/SOS Nonvolatile Memories

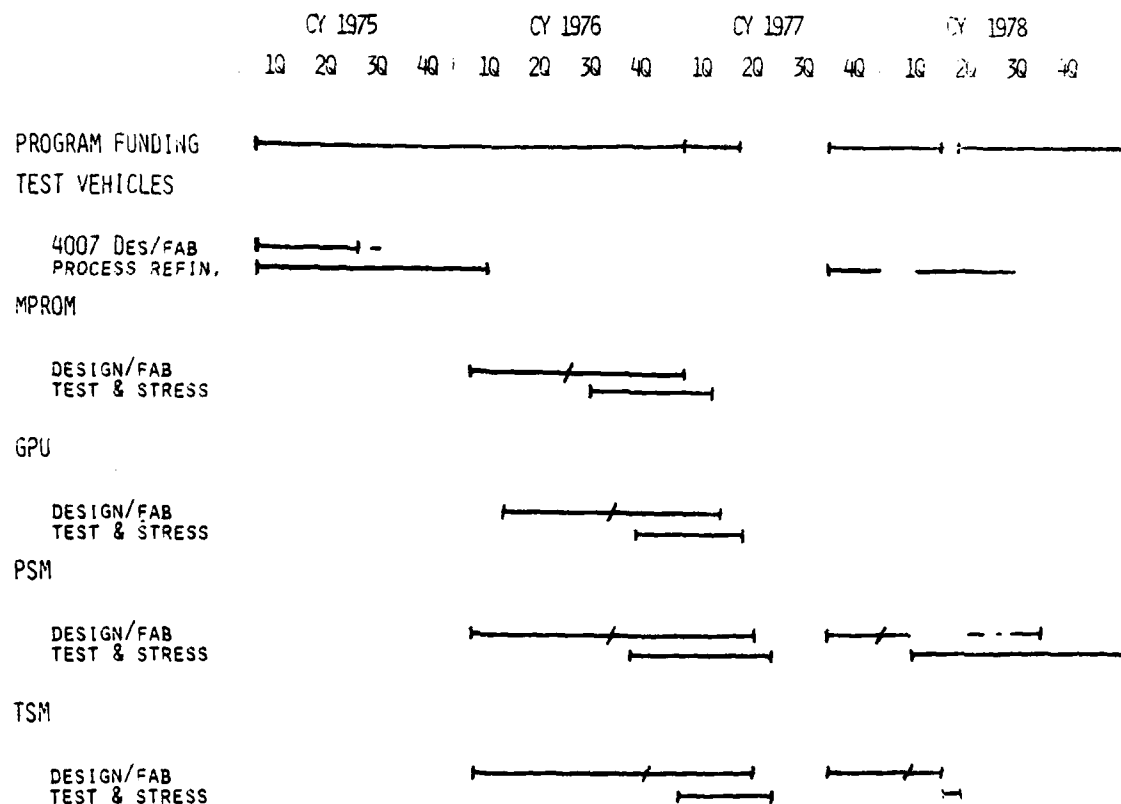
PSM -- 256 x 4 program store, long retention  
TSM -- 512 x 1 data store, fast write

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## 1.1 PROGRAM SCHEDULE

This MX ACT 1 program began in February 1975. The initial scope and funding carried the program for somewhat over two years, through April 1977. After a gap of several months, funding was continued effective October 1977 with additions to the Statement of Work. This funding carried the effort through mid-April 1978. In early May 1978 funding again resumed, with more additions to the Statement of Work. The activity on this second continuation was essentially completed in early January 1979. The range of activity during these four years is shown in Figure 1-1 as a PROGRAM OVERVIEW. Within Westinghouse, these three funding intervals of the program have commonly been referred to as "scenes", and this terminology may be found in some parts of this final technical report. Scene 1 is the original program: February 1975 through April 1977. Scene 2 is the first continuation: October 1977 through mid-April 1978. Scene 3 is the second continuation: May 1978 through January 1979.



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FIGURE 1-1 MX ACT I PROGRAM OVERVIEW

## 1.2 PROGRAM ACCOMPLISHMENTS

The MX ACT-I Programs was successful in advancing the critical technologies required to build an advanced hardened missile computer utilizing CMOS/SOS logic and MNOS/SOS memory devices. The maturity of the processing was advanced considerably, but was much more difficult than originally envisioned, and requires additional effort.

A basic parts phase produced a group of 4007 triple inverters using the nitride thick 100Å oxide gate CMOS/SOS process. This activity established the base line processing, and led to improvements of cell geometry, better short channel modeling and established the device basic parameters prior to modeling and fabrication of the LSI parts. These parts were delivered to RADC for reliability and radiation tests - see "MX ACT-I CMOS/SOS Reliability and Radiation Tolerance Studies" RADC-TR-77-301. Also test vehicles were built and tested for the ROM and PSM which improved their following LSI designs.

Improved input and output protect circuitry was developed, tested and refined such that no static discharge problem associated with handling, testing or burn-in activities occurred with the hundreds of LSI parts built during the program. In contrast, unprotected test transistors did experience static electricity handling failures similar to the well know difficulties found in many industrial MOS parts. Later test transistor designs had to include input protection.

A MX/ACT-I Concepts Review Report (CDRL Item A01M, NORT 76-4) was prepared which developed and improved the functional and parametric requirements for the LSI parts to be developed. Computer aided circuit analysis and synthesis was done on all the LSI parts to assist meeting the design requirements.

The CMOS/SOS technology was carried to a maturity where adequate yields of satisfactory MPROM parts were produced, then taken through design verification and radiation tests. A Developmental Test Report and a Design Verification Test Report were written (CDRL C006). The success with the MPROM, which was done ahead of the GPU, lead to direction to halt development and tests on the GPU fabrication since it utilized the same technology as that proven with the ROM, and more resources were needed for the memory developments. Some GPU parts were carried through fabrication, and tested, functionality and design speed goals were demonstrated, but design verification tests and complete radiation tests were cancelled.

The memory developments were more difficult and frustrated by variabilities in processing. During the first contract interval a slow write PSM, type 6013, was developed, and finally matured to acceptable yields for a very large 60K mil<sup>2</sup> chip. This large size resulted partly from keeping the single word clear/write organization originally requested.

Much testing was done, and a Developmental Test Report and Design Verification Test Report were prepared (CDRL C006). During the evaluation of the 6013 PSM, several problems were revealed. In scene 2, and improved PSM design, type 6023.

was undertaken with new mask sets, but the changes were limited and the same large chip size remained. Many process studies and test patterns were evaluated, including unexpected processing difficulties on the few lots processed. The incorporation of low pressure chemical vapor deposition and other process changes, new mask sets, improved test software and window test measurements produced a group of fully functional parts that performed well in burn-in and radiation testing. Improvements in total dose hardness and cell uniformity was confirmed. The process problems and limited funding prevented maturing this design to a demonstrated satisfactory yield.

The fast write temporary store memory, TSM 6012, was designed and fabricated. The technique of compare before write to inhibit window saturation and differential detection approaches were proven. Test vehicle and TSM part tests proved the feasibility of a fast write nonvolatile memory, but the goal of retention for 48 hours after a worst case 1 usec write was not uniformly achieved, nor were enough parts produced to establish a mature process with acceptable yields. A redesign of the TSM, Part Type 6024, was completed, but funds to fabricate this new design were reallocated to complete the new 6023 PSM part.

The specified radiation hardness was met by both the CPU and Memory slow write processes. Details of the total dose radiation tests are covered in this report and details of the transient upset and survivability tests are contained Radiation Test results in section 4.0.

### 1.3 TRACEABILITY AND CONFIGURATION CONTROL

All parts packaged on the MX ACT I program are serialized and can be traced through all processing steps to the SOS starting material. Each dual-in-line package (DIP) is marked with the part number (mask number) of the die contained, the date code (week and year) when lidded, and a unique serial number. Mask design, process parameters, packaging procedure and test data are all controlled with defined initial review and change notice approvals, assuring configuration control of the parts designed, fabricated and tested on the program.

The procedure for packaging each MX part includes entry in the MX Packaging Log of the following information: serial numbers, mask set, run folder (lot) number, wafer number, die number, bonding diagram number, type of bonding wire (Au or Al), method of die mount (epoxy or eutectic) and date of packaging. The serial numbers are assigned sequentially to all MX packaged parts, independent of part number or date. This Packaging Log is maintained by the MX ACT I Program Office. It begins with CMOS/SOS test pattern 4020 parts, MNOS/SOS test pattern 6003T parts, and 4007-type CMOS/SOS Triple inverter parts assembled in May 1975, continues through the 4007s assembled for delivery in July 1975, the first LSIC parts assembled in August 1976, to the present time (October 1978). It now contains over 5000 entries.

The mask set for each LSIC part type includes a means for photoengraving a unique die number on the wafer at each die site on the mask. This has been

accomplished either by etching in the silicon film or the aluminum metallization. The processing of every lot includes a laser marking step, either before or after the first photomasking, when each wafer is marked with the lot number and wafer number in that lot. This marking is near the edge of the wafer parallel to the flat.

Release of the mask design to mask making requires a design review meeting which includes process and mask making engineers as well as design engineers not involved in the layout being reviewed. Changes or corrections to the mask set are not implemented without an Engineering Change Notice listing the reasons for change and signed by the responsible persons.

The sequence of steps for processing each lot, with all mask numbers and revisions, standard process references, and specific conditions, is contained in a run folder. The master run folder is developed by program engineering, under direction of the Technical Director, in consultation with process engineering. It must be signed/ approved by process engineering, including the engineers responsible for diffusions, oxidation, photo chemistry, ion implantation, chemical vapor deposition, and vacuum deposition. Each run folder must also be signed by the laboratory manager. A separate run folder is provided for each lot. It begins with instructions for drawing the desired quantity and type of wafers for that run. At that page, the eight-digit date code for the SOS wafers, provided by the vendor, Union Carbide Company, is recorded in the run folder. That date code contains information on the UCC epitaxial reactor used, the year, month and day processed and the epitaxial run(s) which provided the wafers. From this number, UCC can trace back to the sapphire boule from which the SOS wafers were cut.

As the lot is processed, all steps are checked, dated and initialed in the run folder. Points for engineering inspection are included, serving to halt processing until each is signed off, with notes of any unusual condition observed. Measurements of film thicknesses and other processing parameters are required and the results are recorded in the run folder. The quantity of wafers, whole and partial, into and out of each appropriate step is recorded, with the number(s) of the wafer(s) rejected. Wafer breakage is noted in the run folder, and partial wafers larger than half size are generally continued with the lot. If the number on the wafer is missing due to breakage, a sketch of the shape of that wafer, with the wafer number, serves to preserve traceability. Completed run folders and all in-process test data therein are filed by the program office, available for study.

When the lot reaches wafer test, a map of that wafer type, with die numbers and test patterns shown, serves to identify functional dice. Printout from the automatic tester is keyed to the die number as well as wafer and lot number. Tester "binning" information, which is a measure of functionality, is displayed and recorded at the respective die site on the map for that wafer. These maps are used to select parts for packaging and visually to define for assembly personnel the dice to saw and package (in addition to listing the die numbers). Assembly of parts is initiated by a Packaging Request form, which specifies which dice are to be assembled and to what procedures. It is initialed by Program Management. It references a Die

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Mount and Wire Bonding Diagram, which is a document controlled by the Program Office. The wafer maps are also studied for yield enhancement.

After dice are mounted in the packages, which are marked with serial numbers, all subsequent inspections and tests are referenced to the package serial number. This begins with prelid visual inspection, and continues through QA screen and subsequent life tests, radiation tests and any other stresses.

The preceeding paragraphs of this section have described the methods and procedures used on this program to ensure configuration definition and traceability of all parts to detailed processing, packaging and testing. By these methods and procedures, MIL-STD-483 has been implemented as applicable to this advanced technology program, recognizing that the desired fabrication techniques were evolving throughout the program and that there were no interchangeability requirements on the LSIC parts being designed, fabricated and tested.

SECTION 2  
CPU (CMOS/SOS) PARTS

On this task, five CMOS logic parts were designed and fabricated. All were directed at Central Processor Unit (CPU) applications. All were designed using CMOS (Complementary Metal Oxide Semiconductor) circuitry, to be fabricated using CMOS/SOS technology (using Silicon film on Sapphire wafers). This circuitry and technology were chosen as most suitable for low power and radiation hardness as required for the intended missile guidance computer application.

The first part to be designed was a simple circuit comprising three n-channel and three p-channel MOS transistors, essentially the same as the commercial part type 4007 "dual complementary pair plus inverter." It was designed at the start of the program and served as a useful and easily evaluated test vehicle for adjustments to the CMOS process to meet the radiation requirement. A quantity of fifty parts were shipped to the SAMSO program office by the end of July 1975, as required by the SOW. The part was redesigned in 1977 to incorporate design improvements. It is labeled the 4007B and was used as a CMOS/SOS test vehicle in the continuation phase of the ACT I program.

The second part to be designed was a CPU test vehicle, Westinghouse mask set number 4021. It included the following cells: latch, output select, shift select, adder with four-bit carry, 3-state I/O buffer, several ring oscillators and some test point buffers. These cells are typical of those needed in the full LSIC General Processor Unit (GPU) to be designed later in the program using test results from this CPU test vehicle.

The third CMOS part to be designed was a Read-Only Memory (ROM) test vehicle, Westinghouse mask set number 4022. It was not included in the CPU test vehicle to permit earlier test results from that part and additional study on the ROM circuitry. This part simulated a 32-row by 16-column array, with only a partial row decoder included. This design effort included much study applicable to the LSIC ROM.

The fourth and fifth CMOS parts to be designed were the LSICs. These parts are a 4-bit slice of a general processor, the GPU, and a 256 word by 4-bit wide Read-Only Memory, the MPROM. The Westinghouse mask set numbers are 4027 for the GPU and 4028 for the MPROM. Design on these was begun after the Concept Review Meeting, 26 February 1976. Designs, simulations and layout were well underway by the Part Design Review Meeting II (PDR II), 3 June 1976. The MPROM was closest to completion. Priority on the LSIC MNOS memory parts was higher than for the GPU, so effort on the GPU was sometimes deferred in favor of the MNOS parts. Design had progressed sufficiently by PDR II to present characteristics, features, block and timing diagrams, circuits and simulations, approximate transistor counts, and estimated die sizes.

Layout on the MPROM was complete by mid July 1976. Processing, diagnostic testing and some mask iteration was complete in November 1976. A full complement

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of MPROM parts were processed and screened by early March 1977. Good yield in processing was obtained. A total of 114 fully functional parts were screened. Yield for the 168 hour, 125C burn-in was 94%. All desired testing on these parts was completed successfully.

Layout on the GPU was complete by early October 1976. Processing, diagnostic testing and some mask iteration was complete by February 1977. Fully functional parts were obtained, showing fast operation. Effort on the GPU was finished in March 1977.

## 2.1 CMOS/SOS DESIGN

Prior to circuit design, many device design factors were determined. These relate to MOSFET parameter values and to circuit design rules. These topics are discussed in the subsections that follow. Also included is a subsection on use of the model for circuit simulation.

### 2.1.1 CMOS Design Parameters

The device parameters, design equations and computer simulation approach were evaluated and improved over those used for test vehicle design. The design parameter activity involved the collection of new data, the development of new design equations, adoption of a modified device model in the ISPIICE program (the ISPIICE short channel model) and cross-correlation with previous data.

The major new findings that prompted this activity were the following:

- a) Channel lengths after processing varied between 3.5 and 5.0 microns for the parts that were nominally 5 $\mu$ m. (Therefore, mobility values were recalculated on the basis of the shorter channel length).
- b) The parameters and computer simulations for the test vehicles did not provide a good fit in both the triode and pentode regions of the  $I_{DS}$  vs  $V_{DS}$  characteristic. (Therefore, triode mode values are now entered and corrected for the pentode mode by the ISPIICE program).
- c) For gate voltages above 12 volts a significant gate voltage dependent mobility correction (normal field) is needed. (The ISPIICE short channel model provides this correction).
- d) The reduction of the body contact spacing from 100 $\mu$ m to 52 and 26 $\mu$ m was found to increase  $V_{TN}$  and reduce the  $V_{TN}$  hysteresis. The onset of kink is moved to larger values of  $V_{DS}$  (typically >7 volts). (Body contact spacing is now 40 $\mu$ m maximum).
- e) The high voltage n-channel structures have a much reduced kink effect and behave more like devices with a minimum body contact spacing.
- f) Channel length modulation effects are significant for the short channel devices and need to be taken into account when calculating mobility. (More conservative mobility values were calculated using after-processing channel lengths of  $L_0 = 3.5\mu$ m (worst case for mobility calculations from 4007 data). The electrical channel lengths at  $V_{DD} = 10V$

including channel length modulation effects are p channel  $L_{EFF} = 2.8\mu m$  and n channel  $L_{EFF} = 3.1\mu m$ .

The results of this design activity are summarized below:

- a) N-Channel Threshold voltages within an LSI array are kept uniform for transistors of various widths by fixing the maximum body contact spacing to be no greater than  $40\mu m$ . This also minimizes threshold hysteresis to less than 0.2.
- b) The design channel length after processing is  $L_0 = 3\mu m$ . (This corresponds to an "as-drawn" channel length of 4 micrometers), New mask making procedures insure  $\pm 0.5\mu m$  tolerance on  $L_0$ .
- c) The mobility in the triode region ( $V_{DS} \ll V_{gs} - V_T$ ) has been measured and correlated with previous measurements in the pentode region. The mobility values entered in the ISPICE simulations are the triode values. The relationships are  $\mu_n$  (triode) =  $1.28\mu_n$  (pentode) and  $\mu_p$  (triode) =  $\mu_p$  (pentode).
- d) The post-rad,  $125^\circ C$  mobility (triode) design values entered in the ISPICE program are:

$$\mu_p = 75 \text{ cm}^2/\text{v-sec}$$

$$\mu_n = 130 \text{ cm}^2/\text{v-sec}$$

These values were derived from the values of  $\mu_p$  and  $\mu_n$  measured on the 4007 parts. The shorter channel length ( $L_0$ ), channel length modulation ( $L_{EFF}$ ) and the  $\mu_n$  (triode)/ $\mu_p$  (pentode) correction are taken into account in these mobility calculations.

Additional details of calculations of the parameters used in the ISPICE program and the ISPICE model are described the MPRM Design and Simulation Report. The calculation for threshold voltage and mobility are summarized below. A summary of the ISPICE model parameter used for the ACT-I CMOS LISC's is shown in Table 2.1-1, for both pre and post rad models.

## 2.1.1.1 Threshold Voltage ( $V_T$ )

The threshold voltage and mobility are both determined from the triode mode transconductance  $g_{ds}$  vs.  $V_{gs}$  relationship. The mobility is determined from the slope and the threshold is determined from the intercept, since  $g_{ds} = 2\beta (V_{gs} - V_T)$  as shown in figure 2.1-1.

TABLE 2.1-1 ISPICE SCMOSFET Parameters  
Used for CMOS/SOS Design

String Input Order	Keyword	Used for 25°C Values		CMOS/SOS 125°C Values		Units
		Pre-rad		Post-Rad		
		n-ch	p-ch	n-ch	p-ch	
1	VTO	2.6	2.5	2.1	4.5	Volts
2	PHI	0.77	0.58	0.77	0.58	-
3	UO	200	160	130	75	cm <sup>2</sup> /V-sec
4	NB	4E16	1E15	4E16	1E15	cm <sup>-3</sup>
5	RD	.03	.05	.03	.05	Ω-cm
6	RS	.03	.05	.03	.05	Ω-cm
7	CO	3.84E-8	3.84E-8	3.84E-8	3.84E-8	F/cm <sup>2</sup>
8	C1	3.84E-12	3.84E-12	3.84E-12	3.84E-12	F/cm
9	C2	7.68E-12	7.68E-12	7.68E-12	7.68E-12	F/cm
10	CBD	3E-12	5E-13	3E-12	5E-13	F/cm
11	CBS	3E-12	5E-13	3E-12	5E-13	F/cm
12	PB	0.5	0.5	0.5	0.5	Volts
13	IS	1E-14	1E-14	1E-14	1E-14	Amps
14	KN	0	0	0	0	-
15	MN	0	0	0	0	-
16	KL	0	0	0	0	-
17	ECRIT	∞	∞	∞	∞	-
18	BETA	3.84-6	3.07E-6	2.49E-6	1.44E-6	A/V <sup>2</sup>
19	GAMMA	3	0.47	3	0.47	V
20	LAMBDA	1.8E-5	3.6E-5	1.8E-5	3.6E-5	-

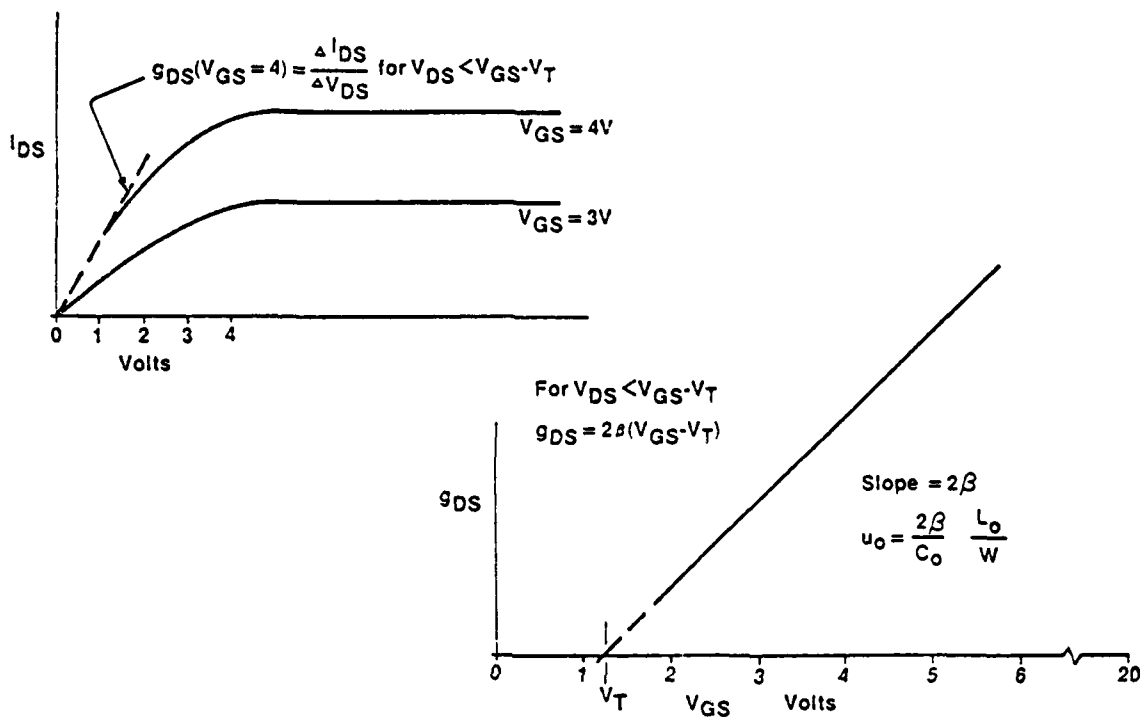


FIGURE 2.1-1 CALCULATION OF  $\mu_o$  FOR  $V_{DS} < V_{GS} - V_T$

## 2.1.1.2 Mobility ( $\mu$ )

Mobility is calculated at  $V_{DS} = 1$  from the  $g_{ds}$  slope as shown in figure 2.1-1 to limit the effect of channel length modulation.

However, to calculate mobility from the  $k'$  data obtained from 4007 tests, the effect of channel length modulation and length must be factored in. The effective length is obtained by:

$$L_{eff} = \left[ 1 + \left( \text{LAMBDA} \frac{1}{L_o} \right) (\sqrt{\phi + V_{DS}} - \sqrt{\phi}) \right]^{-1} (L_o) \quad (3)$$

The values of  $k'$  calculated from data on 4007's assumed the 5um channel length. A correction to the data is obtained by calculating the ratio of assumed to actual width-to-length:

$$w/L_{eff} \div w/L \text{ (5um)} \quad (4)$$

The value of  $K'$  chosen from 4007 data and these correction factors are shown for both p- and n-channel MOSFET's in table 2.1-2 Mobility. Also included in the table are degradation factors for operation at +125°C and post-radiation.

## 2.1.2 Circuit Design Rules

The basic device operating requirements and mask design rules form the basis for the circuit design rules. In this case minimum propagation delay for the worst case conditions of high temperature (125°C) and post-radiation operation is required, consistent with reasonable area. Also the effect of the minimum power supply voltage must be taken into account. External capacitance drive requirements and the mask design rules determine the internal node capacitance values which must be factored into the circuit design calculations. From consideration of these factors, circuit design equations have been developed and are being used for preliminary hand calculation of MOSFET dimensions. The circuit performance is then verified by the computer simulation using the ISPIICE program described in the preceeding section. Size adjustments are made when indicated by the simulation.

### 2.1.2.1 General Rules for Circuit Design

General rules for circuit design are listed below:

- a) Internal transition times (both low to high and high to low) will be designed for 10ns wherever possible, for post-radiation, 125C conditions.
- b) The channel length of CMOS p- and n-channel transistors shall be 3 microns. Length at layout is 4 microns, it becomes about 3 microns after diffusion.
- c) The end capacitance associated with the edge channel stop regions must be included in the input capacitance. These regions are repeated every 40um of channel width for n-channel devices and every 100um for p-channel devices.
- d) The output capacitance term must include the drain gate overlap capacitance (taken as 2um for worst case alignment), the drain junction capacitance, and the input capacitance of the next stage.
- e) Buffering (cascaded inverters) will be used to prevent the transistor input capacitances from exceeding 5pf at a cell input, provided circuit speed is adequate.
- f) Logic functions will be reconfigured when advantageous for area considerations.

Table 2.1-2 Mobility

	<u>Symbol</u>	<u>p-channel</u>	<u>n-channel</u>	<u>Units</u>
1. Value chosen from 4007 data: 25°C, pre-rad:	k'	$5.8 \times 10^{-6}$	$4.8 \times 10^{-6}$	A/V <sup>2</sup>
2. Effect of channel length modulation and actual channel length:	L <sub>eff</sub>	2.79	3.11	um
3. MOSFET width in 4007	W	1200	800	um
4. Correction of length-to-width ratio: $W/L(5\mu m) \div W/L_{eff}$		0.56	0.62	-
5. Adjust from k' in pentode region to triode region:	k'/k'	1.0	1.28	-
6. Resulting k' for 25°C:	k'	$3.25 \times 10^{-6}$	$3.84 \times 10^{-6}$	A/V <sup>2</sup>
7. Worst-case degradation for +125°C:		0.66	0.76	-
8. Worst-case degradation for post-rad:		0.67	0.86	-
9. Design value of k' for operation at +125°C, post-rad:	k'	$1.44 \times 10^{-6}$	$2.49 \times 10^{-6}$	A/V <sup>2</sup>
10. Design value of $\mu$ for operation at +125°C, post-rad:	$\mu$	75	130	cm <sup>2</sup> /V-sec.

g) The maximum number of logic gate inputs should not exceed four. Designs for 4, 6, and 8-input AND and OR functions were developed using both:

- 1) A single multiple-input NAND or NOR followed by an Inverter and
- 2) two NAND or NOR gates with 2, 3, or 4 inputs followed by a two-input NOR or NAND.

The latter design choice was preferable, having less input capacitance, less total channel width and simpler layout.

## 2.1.2.2 Inverter Design Equation Development

An example of the design equation development is given here for the case of an inverter circuit. Further developments are detailed in the MPROM design and simulation report, see Appendix A. In a series of cascaded inverters the channel time constant ( $\tau$ ) of each device in each stage and the transition time ( $t_p$ ) of the input signal are variable factors which affect the propagation delay of the input signal through the inverter string. In the analysis which follows, design equations are developed for n- and p-channel widths, for post-radiation, 125°C conditions. The channel time constant is given by,

$$\tau = C_{load}/gm \quad (2.1)$$

where  $C_{load}$  is the total capacitance at the output of an inverter stage.

The output load capacitance of CMOS inverter is the sum of the n- and p-channel gate-to-drain overlap capacitance and the body-drain junction capacitance plus the capacitance of the next stage.

For a CMOS/SOS device, the junction capacitance is:

$$C_{BD} = C_{BS} = \sqrt{\frac{q k_s \epsilon_o N_B}{2 V_R + \phi_B}} x_j \quad (F/cm) \quad (2.2)$$

where  $\phi_B$  is the junction potential,  $V_R = 0$  @ zero bias,  $x_j = 0.5\mu m$ , and  $N_B$  is the impurity concentration in the body (channel).

# NORTHROP

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Typical post-rad values at 400°C for  $C_{BD}$  are:

P-Channel -  $C_{bd} = 0.5$  pf/cm of channel width

N-channel -  $C_{BD} = 3.0$  pf/cm of channel width

The gate-metal overlap onto the source and drain is designed to be 0.5um.

After processing, the source and drain diffusions will move into the channel approximately 0.5um resulting in a total effective overlap of 1um over the source and the drain. A 1um misalignment increases the overlap to 2um for the worst case. Therefore, the gate-drain overlap capacitances are:

$$C_{GDP} = C_{OX} (1.02 W_p + 2um) (2um),$$

and

$$C_{GDN} = C_{OX} (1.2 W_N + 8um) (2um), \quad (2.3)$$

The terms  $(1.02 W_p + 2um)$  and  $(1.2 W_N + 8um)$  are the result of the overlap related to the edge channel stop regions. The edge channel stops also serve as channel body contacts and are repeated every 100um for the p-channel and every 40um for the n-channel devices. The output capacitance for a device, including drain junction capacitance, is:

$$C_{OUTp} = C_{OX} (1.02 W_p + 2um) (2um) + (0.5pf/um)W_p \quad (2.4)$$

$$C_{OUTN} = C_{OX} (1.2 W_N + 8um) (2um) + (3.0pf/um)W_N \quad (2.5)$$

The sum of the n and p output capacitance for a typical inverter, taking into account that  $W_N = 0.485 W_p$  (See Equation 2.10) for post-radiation 125 C conditions, and using the sum  $W_T = W_p + W_N = 1.485 W_p$ , is given by the following:

$$C_{OUT} = C_{OX} (1.08 W_T + 10um) (2um) + (1.3 \times 10^{-4} pf/um) W_T (pf) \quad (2.6)$$

for  $W_p \geq 100um$  and  $W_N \geq 40um$ .

For those cases where the channel widths are less than above, the actual and overlap capacitance is calculated and added to the circuit output node for simulation.

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The input capacitance is a combination of the gate oxide capacitance and the additional capacitance associated with the channel stop regions, termed CEND or end capacitance. Therefore the input capacitance for the n and p channel devices is the following:

$$C_{INP} = C_{OX} L_g (1.02W_p + 2\mu m) \quad (2.7)$$

$$C_{INN} = C_{OX} L_g (1.2 W_N + 8\mu m) \quad (2.8)$$

and the total input capacitance of an inverter is

$$C_{INT} = C_{OX} L_g (1.08W_T + 10\mu m), \quad (2.9)$$

where

$L_g$  = width of metal gate (6 $\mu m$  typ)

$W_T = W_N + W_P$

$W_N = 0.485 W_P$

$C_{OX}$  = capacitance per unit area of the gate insulator.

The ratio of the widths of the n- and p-channel devices is based on a computer simulation using post-radiation 125°C values of threshold and mobility. The basic requirement for the inverter was equal transition times of  $t_{THL}$  and  $t_{TLH} = 10\text{nsec}$ , for the following conditions: 10nsec transition times on the input waveform, an external 10pf load capacitance and the worst case supply voltage = 10v. The simulation demonstrated that the required widths were  $W_p = 900\mu m$  and  $W_N = 435\mu m$ . Thus the ratio of the widths is  $W_N/W_P = 0.485$ . The n and p-channel widths required for different capacitance loads  $C_L$  or for different transition times  $t_T$  can be scaled from the above basic simulation using the following equations:

$$W_P = 900 C_L (\text{pf}) / t_T (\text{ns}) \mu m \quad (2.10)$$

and

$$W_N = 435 C_L (\text{pf}) / t_T (\text{ns}) \mu m \quad (2.11)$$

Additional computer simulations have been used to verify that the above equation can be used for scaling to different capacitance loads and/or transition times.

# NORTHROP

Electronics Division

It should be noted that the ratio of the output to input capacitance for the basic inverter simulation is about 2.6. This represents the capacitance gain per stage for the 10 nanosec transition time conditions.

A more general equation for estimation of n and p-channel widths for different conditions has been derived. First, there is a relationship between the channel time constant  $\tau$  and the transition time given by:

$$\tau_T = F \tau \quad (2.12)$$

where

F is an empirically determined factor which is related to the input transition time overlap capacitance, output capacitance and relative sizes of n- and p-channel devices.

$$\text{and } \tau = C_L / g_m, g_m = \mu C_{OX} (W/L_O) (V_{GS} - V_T) \quad (2.13)$$

and  $V_{GS}$  = maximum gate voltage =  $V_{DD}$

From the post-radiation, 125°C simulation, the more general inverter equations are:

$$W_P = \frac{C_{LOAD}}{\frac{\mu_P C_{OX}}{L_O} \frac{\tau_T}{5.28} (V_{DD} - V_{TP})} \quad (2.14)$$

$$W_N = \frac{C_{LOAD}}{\frac{\mu_P C_{OX}}{L_O} \frac{\tau_T}{6.38} (V_{DD} - V_{TN})} \quad (2.15)$$

The empirical factors F for these conditions are  $F_P = 5.28$  and  $F_N = 6.38$ . These factors will change somewhat as the ratio of  $\mu_p/\mu_n$  and  $V_T/V_{DD}$  are changed; therefore, the above calculation should be considered only as an approximation if the ratio changes.

### 2.1.3 CMOS Layout Design Rules

Having chosen a process sequence and studied present capability plus unique aspects of Silicon-on-Sapphire, a suitable set of mask design rules was presented. The approach taken was to use conservative design rules so as to maximize photomasking yields and electrical performance. This approach does not result in small LSI die size, but reduction of photomask problems is more important in the first layout of new and complex devices. A redesign for producibility would use tighter layout design rules, and would be appropriate after device performance was verified.

The salient design rules for the CMOS LSIC design (MPROM and GPU) are discussed in paragraph 3.1.2.

## 2.2 THE MASK-PROGRAMMABLE READ ONLY MEMORY, MPROM

The program goals required a read only memory suitable for microprogram storage to operate with a general processor. Also required was operation through certain total dose and dose rate environments. These goals directed the design of the MPROM CMOS/SOS LSIC described in the section which follows. The design was successful, as subsequent sections on test results demonstrate. In brief, 114 fully functional MPROMs were subjected to a screen per MIL-STD-883A, Method 5004, Class B. The yield for the 168 hour dynamic burn-in at 125C was 94%. Radiation tests verified that the design and process meet the program goals. A total of 48 parts were subjected to total dose testing, including total dose to failure. Dose rate testing was done on 23 parts, and neutron exposure on 9 parts. Temperature-bias-stress testing ran for 3000 hours on six parts and about 2000 hours on 24 parts.

### 2.2.1 MPROM Design

In this section the circuit design and results of circuit simulation for the mask-programmable, Read-Only Memory are presented and discussed. As background to the design and simulation, this first subsection includes brief descriptions of this LSI part, both functional and operational. The second subsection contains one particular circuit schematic diagram and simulation result. The fourth section describes the expected performance of this CMOS/SOS part.

#### 2.2.1.1 Brief Descriptions of the MPROM

This mask-programmable, Read-Only Memory was designed primarily for microprogram storage. It is also useful for program storage. The design is denoted by the mask set number: 4028. A tabulation of the characteristics and features is given in Figure 2.2-1.

## Characteristics and Features

- o 256 x 4 Organization
- o Random access
 

	Pre-Rad	Post-Rad, 125 C
Read access	90 ns	150 ns
Read cycle	120 ns	210 ns
- o 3-State Output Buffers
  - Drive 20 pf in 30 ns
- o Power
 

Read	90mW at 2.7 MHz, 12V
Deselected	200μW at 12V
- o Complexity 1624 transistors
- o CMOS/SOS technology
- o Bit pattern programmed at metal level
- o Differential detection
- o Data ready output to strobe second tier MPRoMs
- o Single supply: 12V nominal
- o In 40-lead DIP, fits 18-lead DIP w/o test transistors

FIGURE 2.2-1 MASK-PROGRAMMABLE, READ-ONLY MEMORY

### 2.2.1.1.1 Functional Description

The mask-programmable, Read-Only Memory is organized to store 256 words of 4 bits each. A block diagram of the MPRoM is shown as Figure 2.2-2. The desired bit pattern is incorporated into the part during fabrication, at the metal interconnect level. Eight address inputs determine the word to be read. Four 3-state buffers provide the output. For operation of more than one MPRoM on the same 4-bit data bus, the outputs of the parts not addressed are prevented from driving or loading the bus by setting a "chip select" input (CS) at the HIGH level. When this control input is LOW, the part outputs the addressed word. A pair of enable inputs are used to operate the internal decode and read circuitry: either or both  $\overline{EN}_1$  &  $\overline{EN}_2$  must cycle HIGH-LOW with each address change.

A useful feature of this ROM is a data ready output ( $\overline{DR}$ ). It signals when all four data outputs are correct, i. e. when the output can be read. It can be used to strobe the output into a register or it can serve as the enable signal to a second tier of ROM's which are addressed by outputs of a first tier of ROM's. Because the 8-bit address would come from two ROM's, two enable inputs are accepted ( $\overline{EN}_1$  and  $\overline{EN}_2$ ); these could be the  $\overline{DR}$  outputs from those two ROM's. The second tier ROM would not be enabled until both  $\overline{DR}$  inputs were LOW. When not needed, one enable input can be tied LOW ( $\overline{EN}_1$  or  $\overline{EN}_2$ ).

This CMOS/SOS LSI part requires a single  $V_{DD}$  supply voltage, nominally +12V.

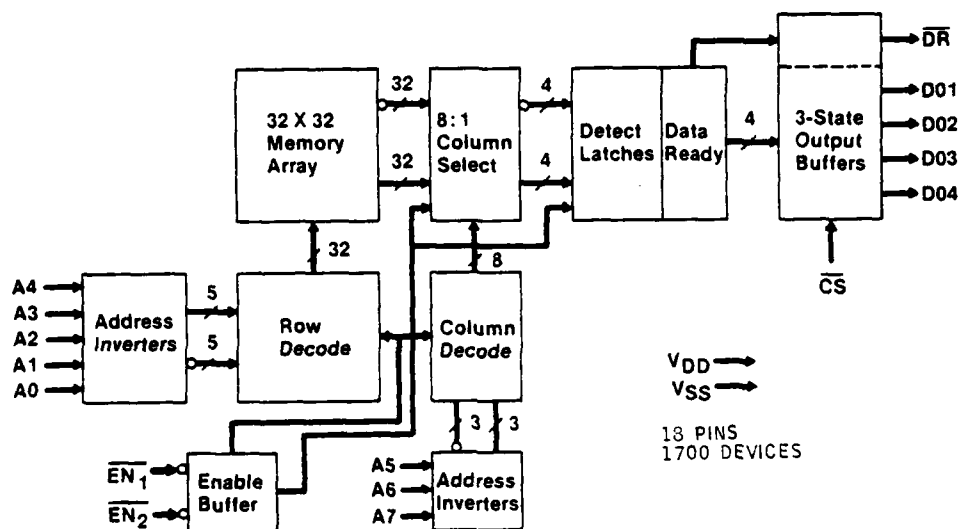


FIGURE 2.2-2 CMOS/SOS ROM, MASK PROGRAMMABLE  
ORGANIZATION FOR 256 WORDS BY 4-BITS

All inputs respond to CMOS levels and all outputs drive at CMOS levels. Eighteen pins are required for the inputs, outputs, power and ground. It is designed to operate with a supply voltage range of 10 to 13V, over the full -55°C to +125°C ambient temperature range. The design ensures operation before and after the required total radiation dose and through the required dose rate.

## 2.2.1.1.2 Operational Description

The internal organization of this 1024-bit ROM is 32 rows by 32 columns. The five least significant address bits (A0 - A4) are decoded to select one of 32 rows; the remaining three address bits (A5 - A7) select one of eight columns for each of the four outputs. The chip select input (CS) can serve as the ninth bit of address, used if more than one ROM outputs to the same 4-bit data bus, to provide more than 256 words. The CS inputs to the 3-state output buffers only. When CS is LOW, the buffers actively drive a data bus with the addressed word. When CS is HIGH, the buffers are forced into a high impedance state, neither driving nor significantly loading the bus, by turning OFF both the n- and p-channel output transistors. The response of the 3-state buffers to this CS input favors applications with two or more ROM's on a common data bus. When selection is transferred from one ROM to another, the internal timing ensures that the overlap time during which both ROM's are in the active state is insignificant, thereby minimizing current surges on the supply lines.

The enable function serves to discharge decoders and to charge differential sense lines and bistable detect latches before responding to a new address. This design provides highly reliable operation with a minimum transistor count and insensitivity to radiation effects, either from threshold shifts, mobility degradation, or photocurrents.

The 1024-bit pattern is programmed during wafer fabrication. It is done at the metal interconnect level. The drain of each transistor in the 32 row by 32 column memory array is connected to either the "ONE" or "ZERO" column sense line by custom design of this portion of the interconnect pattern.

The detailed part specification for the MPR0M, LSIC device number 4028, is included in Appendix B.

#### 2.2.1.2 MPR0M Circuits and Simulations

In order to verify the post-radiation operation of the MPR0M LSIC part in a 125°C environment, computer simulation of the circuitry was carried out using the ISPICE circuit analysis programs. The ISPICE simulations utilize the models and parameters as discussed in 2.1 above. This section will discuss the results of the simulation for the case of photocurrent generation in the detection latch circuit. The other circuit simulations are given in the MP/ROM Design and Simulation Report. See Appendix A. The simulations were all carried out for post-radiation, 125°C operation.

##### 2.2.1.2.1 Data Cell, Column Select, Detect Latch

The decoded row and column address lines are used to select the proper MP/ROM data cell present in the memory array. Figure 2.2-3 and 2.2-4 represent circuits used to select and detect the ROM data bit. The actual bit pattern in the memory array will be established at the metal interconnect level during processing. The other input is the ENA signal generated by the chip enable circuit described above. ENA presets the bit lines to  $V_{DD}$  through p-channel devices, ENA being LOW until the chip is enabled. ENA also precharges the detect latch inputs, D0 and D1, to  $V_{DD}$  setting the latch outputs, Q and  $\bar{Q}$ , to LOW. The timing is such that ENA and the address lines will go HIGH simultaneously. This will turn OFF the precharge transistors and address the proper ROM data bit.

The ROM data cell which is addressed will be selected by the row decode lines, thus turning ON the n-channel data transistor. The selected column address will enable the proper set of select switches in the detect latch input lines. The select switch will thus connect the programmed bit to the data latch. If the selected bit is programmed as a ZERO, the data transistor will discharge the D0 line to  $V_{SS}$ . If a ONE is programmed into the bit, the D1 line will discharge to  $V_{SS}$ .

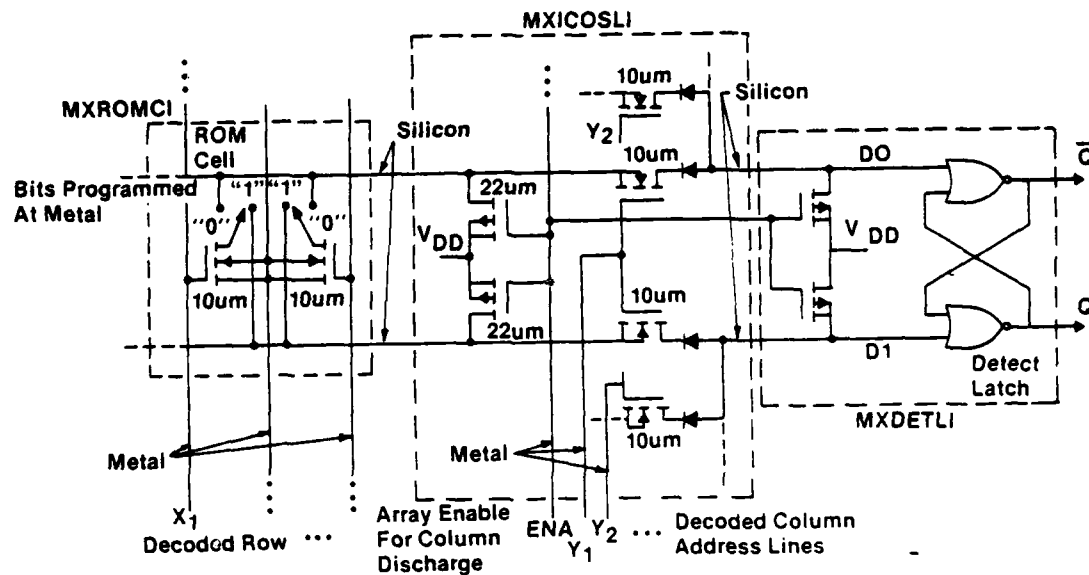


FIGURE 2.2-3 ROM: CELL AND COLUMN

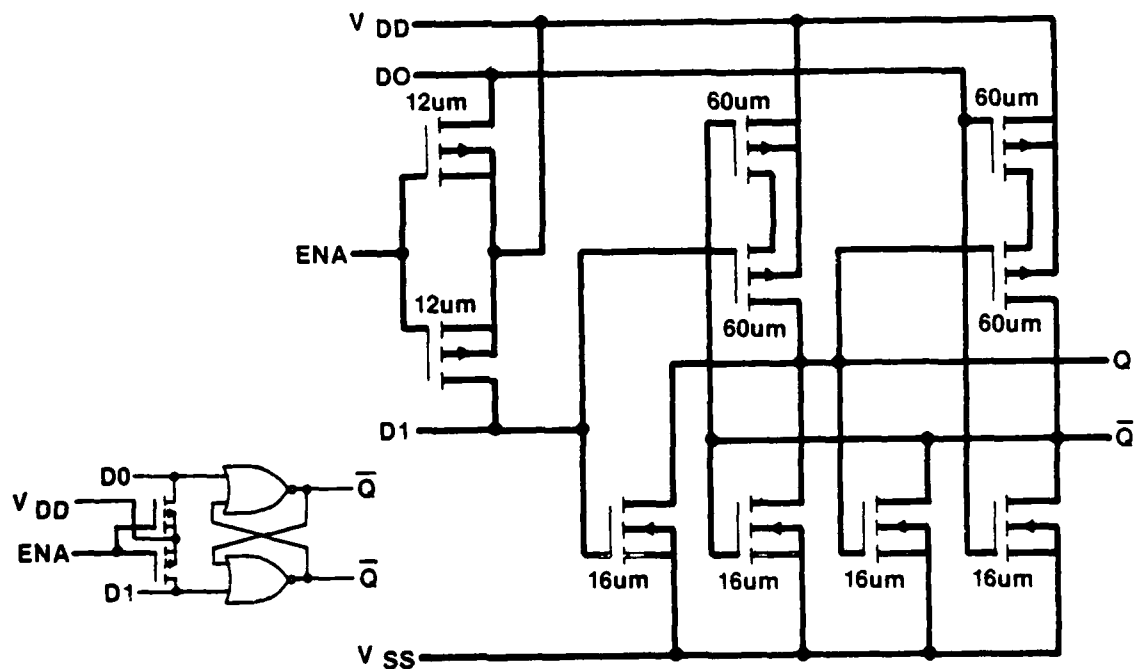


FIGURE 2.2-4 ROM: DETECT LATCH

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Thus, Q will go LOW and then HIGH, respectively. When the chip is deselected the ENA signal will again precharge the D0 and D1 lines to  $V_{DD}$ , establishing the detect latch levels for the succeeding address.

For the MP/ROM array and detect latch circuits, it is necessary to simulate two different cases. First, it is necessary to simulate what is termed the worst-case data bit. The worst case data bit is the bit physically located such that it is influenced by the loading of the remaining 31 bits in a column. This simulation is represented by the circuit in figure 2.2-5. In this case, the effects of the remaining 31 bits in the column are represented as a distributed resistor-capacitor network. The array data transistor is represented by M25; precharge transistors M23 and M35, detect precharge transistors M24 and M36, and column select switches are represented by M37, D2, M26 and D1. Resistors R3 through R6 and capacitors C5 to C8 represent the column loading. Figure 2.2-6 shows the "worst-case" simulation with row address X1 as the driving function and Q as the output. The data bit is programmed as a ZERO. ENA is set for the simulation to coincide with the X1 driving function. The result is that the "worst-case" data bit has a 44 nanosec propagation time from address select to data out through the detect latch.

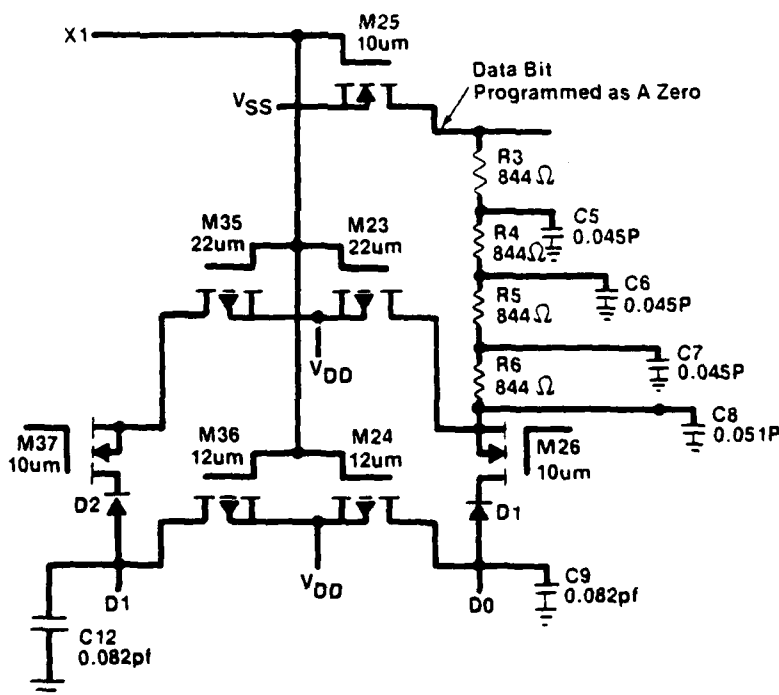
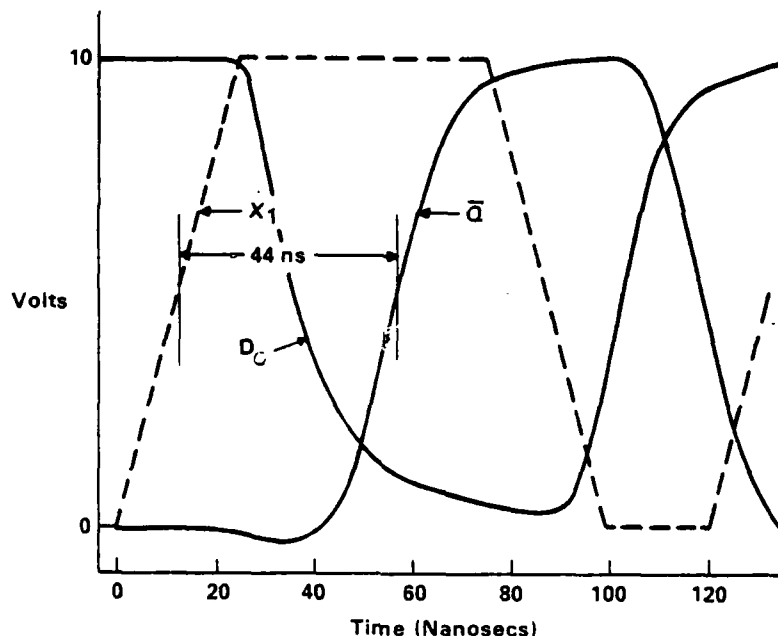


FIGURE 2.2-5 ROM: SIMULATION CIRCUIT, WORST-CASE BIT



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FIGURE 2.2-6 ROM SIMULATION OF RAM ARRAY, WORST-CASE BIT  
POST-RAD, 125°C

The other case simulated is the effect of a photocurrent generator upon the data cell and detect latch. The timing in the circuit is such that the output of the detect latch is established by which sense line goes LOW first (i.e. discharged by the data cell). Thus, any photocurrents generated, although causing voltage swings, must not disrupt the established timing. Figure 2.2-7 shows the circuit used to simulate photocurrent effects. In this case, the bit is programmed as a ONE, thus when addressed the D1 line to the detect latch will be discharged. Resistor R7 represents the path from the addressed bit to the column select switch. A photocurrent generator is represented by an n-channel transistor supplying 53 $\mu$ a at 10 volt bias (M38). This simulates a wide pulse GAMMA transient level of 10 times the spec.

The current source is connected to the node representing the column select switches, which is in the D0 sense line. The current generator is used to represent the photocurrent induced in the 31 deselected bits of the addressed column. D0 will have the tendency to be discharged by the photocurrent. The simulation in Figure 2.2-8 is similar to that shown in Figure 2.2-6, with the effects of photocurrent added. With the programmed bit set at ONE, D1 is discharged and Q is set to ONE. The effect of the photocurrent generator is seen in the signal D0, which initially is discharged, however the relative timing between D0 and D1 required by the detect latch is preserved. Thus Q goes HIGH, Q remains LOW as required.

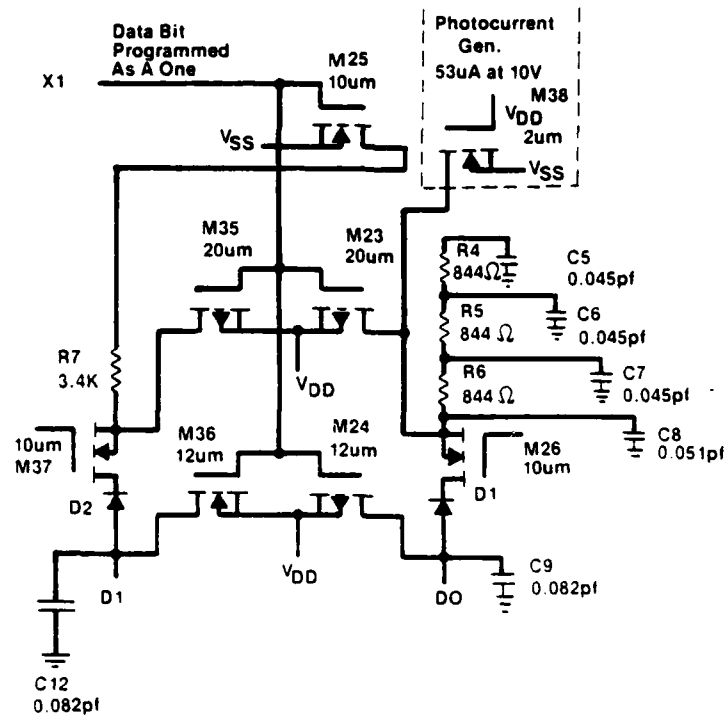


FIGURE 2.2-7 ROM: SIMULATION CIRCUIT, PHOTOCURRENT

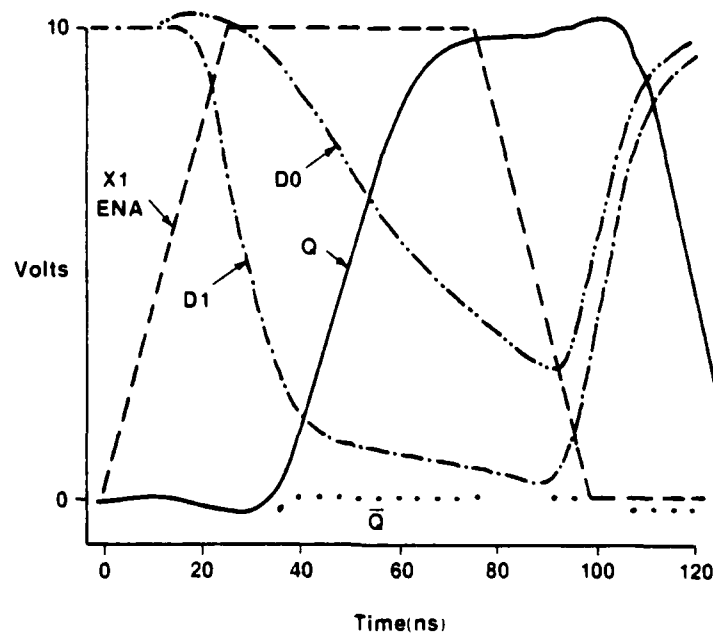


FIGURE 2.2-8 ROM SIMULATION OF ROM ARRAY, WITH PHOTOCURRENT POST-RAD, 125°C

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By this simulation, the dual-line, differential detection circuit is shown to function correctly with the worst-case photocurrent. The timing is not disrupted; the circuit detects as desired. Use of the dual-line, differential detection rather than a simpler single-line detection scheme does require more layout area. And the timing design, which requires a disable pulse between addresses, is more complex than a simple purely static circuit. But the excellent immunity of this circuitry and timing scheme to high dose rate effects validates the need for such a design. It meets the required radiation performance with good margin, as has been shown in radiation tests performed on actual MPRM devices.

#### 2.2.1.2.2 MPRM Test Pattern

The MX ACT L MPRM was designed and fabricated with the fixed data pattern shown in Figure 2.2-9. This pattern provides worst-case loading of all columns, maximum variations in data pattern in each column, and equal row loading for all addresses. This pattern allows the MPRM to be fully characterized for pattern sensitivity to loading, etc.

In measuring worst-case access times, the addresses are cycled and the longest address time is recorded. This can be done for either a selected output bit, the data ready signal, or the entire ROM array.

In the organization of the MPRM test pattern, individual 32-bit columns were set up with 31 "1's" and 1 "0" (and vice versa) to provide worst-case photocurrent generation in the transient environment.

The Life Test Waveform Generator for the MPROM is a dedicated exercisor capable of driving up to eight device boards, each with seven sockets. The Waveform Generator is shown in figure 3.3-9B. It contains front panel LED displays to indicate any deviations from normal for the power supply voltage. It was used for all MPROM burn-in and temperature-bias-stress (TBS) testing of the MPROM.

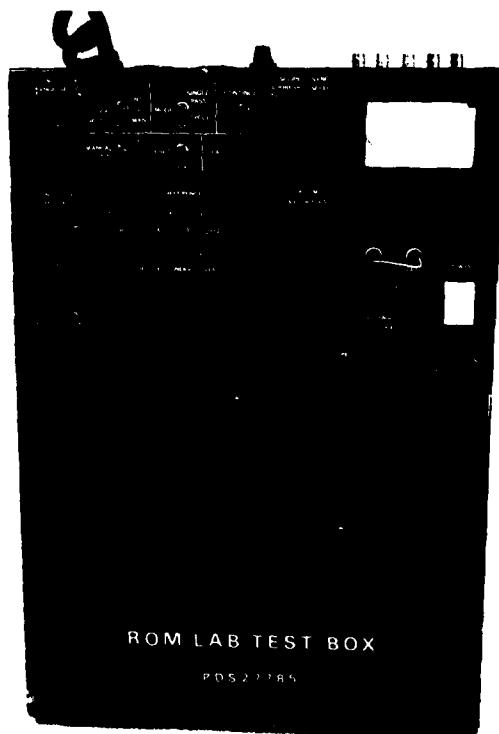


FIGURE 2.2-9A LAB TEST SET FOR THE MPROM 4028 CMOS/SOS MASK-PROGRAMMABLE READ ONLY MEMORY

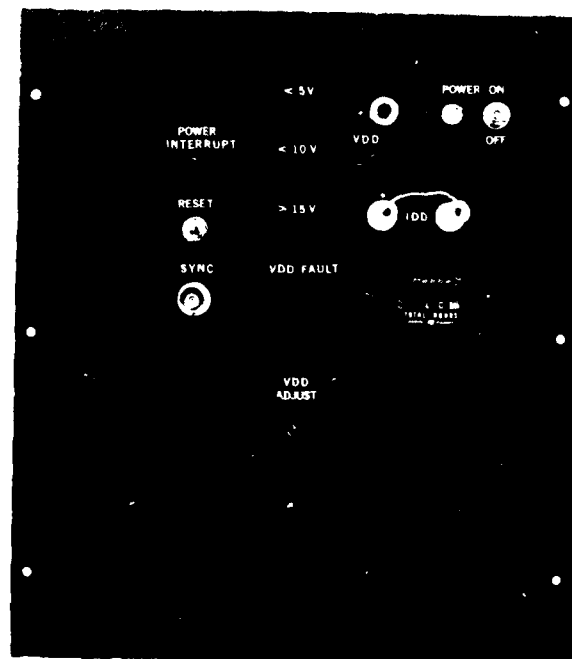


FIGURE 2.2-9B LIFE TEST WAVEFORM GENERATOR AND POWER SUPPLY FOR THE MPROM 4028 CMOS/SOS MASK-PROGRAMMABLE READ ONLY MEMORY

# ACT 1 TEST ROM

256 X 4 ROM PATTERN

	D00				D01				D02				D03			
	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
2	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
3	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
4	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
5	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
6	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
7	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
8	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
9	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
10	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
11	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
12	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
13	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
14	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
15	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
16	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
17	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
18	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
19	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
20	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
21	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
22	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
23	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
24	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
25	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
26	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
27	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
28	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
29	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
30	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
31	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

ROW ADDRESSES  $A_0$  THRU  $A_4$

$\bar{A}_0$   $A_0$   $\bar{A}_1$   $A_1$   $\bar{A}_2$   $A_2$   $\bar{A}_3$   $A_3$   $\bar{A}_4$

$\bar{A}_5 = \text{EVEN}, A_5 = \text{ODD}$

$\bar{A}_6$   $A_6$   $\bar{A}_6$   $A_6$   
 $\bar{A}_7$   $A_7$

FIGURE 2.2-9 ACT 1 MPROM PATTERN

### 2.2.2 MPR0M Fabrication and Wafer Test

Several lots were processed to verify the mask set and performance of the MPR0M. These also verified certain process choices. After verification of design, six lots were run to provide the necessary parts for screen and subsequent tests and stresses. These were completed in the period December 1976 through February 1977 and parts were introduced into the MIL-STD-883, Method 5004, Class B screen.

Of the 36 wafers started into process according to the proper process sequence, 25 reached wafer test, for a wafer throughput of 69%. Electrical wafer tests on the Macrodata MD-154 automatic tester included parametric tests as well as a functional test of all 1024 bits of stored data pattern. Results were 208 fully functional dice at wafer probe, for a yield of over 11% (there are 74 die sites on each wafer, hence 1850 potential dice on the 25 wafers). For this 148 by 202 mil die size, and with the MPR0M so early on the learning curve, the yield is judged to be quite good.

### 2.2.3 MPR0M Test Equipment

In order to test the MPR0M in a thorough and cost-effective manner, both automatic and laboratory test methods were used. A test sequence for wafer test and another for package test were programmed for the Macrodata MD-154 automatic tester. A description of this high speed test system is given in section 3.1.7.1 of this report.

The ROM Lab Test Set is shown in figure 2.2-9A. It was designed to permit diagnostic and special characterization testing of the MPR0M by the design engineer independent of the MD-154. It contains all necessary waveforms and power supply for operation of the LSIC part. Counters and front panel controls generate desired address and control patterns. Timing of the waveforms and magnitude of the supply voltage are adjustable over a wide range. Cycle time is adjustable, ranging from fast enough for operation at the expected 25C pre-rad speed to slow enough for driving parts remote over several feet of cable, into a temperature chamber or to a wafer probe station. A reference PROM (fuze programmable) is included in the test set. It contains the pattern used in the MPR0M and serves as a reference, using a comparator to check the MPR0M under test against this reference PROM.

The Life Test Waveform Generator for the MPR0M is a dedicated exercisor capable of driving up to eight device boards, each with seven sockets. The Waveform Generator is shown in figure 3.3-9B. It contains front panel LED displays to indicate any deviations from normal for the power supply voltage. It was used for all MPR0M burn-in and temperature-bias-stress (TBS) testing of the MPR0M.

## 2.2.4 MPROM Screen Test

Good dice identified at wafer probe, as discussed in section 2.2.2, are assembled into packages and subjected to the MIL-STD-883B, Method 5004, Class B screen procedure. Because each die on the wafer has a unique die number, and because wafer and lot identity are preserved, complete die traceability is maintained for these parts. Section 1.1 describes traceability more completely.

The assembly and screen sequence is shown fully by the trip ticket in figure 2.2-10, by a flow chart in the PSM section 3.1 and by a brief list below:

- Serialize packages
- Die mount and wire bond
- Prelid visual inspection
- Lidding, marking and lead form and shear
- Interim electrical test
- Stabilization bake
- Temperature cycle
- Centrifuge
- Hermeticity
- Optional electrical test
- Burn-in for 168 hours at 125C
- Final electrical test
- External visual inspection

MPROM parts were screened in four lots. A total of 188 good dice were submitted to assembly. There were some losses in assembly, prelid visual, interim electrical test, centrifuge and hermeticity. The total parts passing optional electrical test before burn-in was 127, for an assembly-mechanical screen yield of 68%. Parts submitted to burn-in were 119, with 8 parts removed for urgent total dose tests. After burn-in, 114 parts passed final electrical, for a burn-in yield of 96%. All yields are felt to be good considering that assembly and screen activities for these LSI SOS devices were early on the learning curve. By the fourth screen lot, yield for assembly-mechanical screen had reached 79%.

These screened MPROM parts next went to stress tests as mentioned in the opening paragraph of section 2.2 and as described in sections 2.2.5, 2.2.6 and 2.2.7.

# NORTHROP

Electronics Division

MX PROGRAM					Lot No. _____	
Release Date _____		Responsible Engineer _____			Phone No. _____	
Sta.	Qty.	Operation	Spec. No.	Oper.	Date	
106		Serialize pkgs	—			
107		Die mount — DuPont epoxy No. 5504	A010			
108		Wire bond — ultrasonic	W006			
109		Record S/N's (ref lot, wafer & chip nos.)	—			
—		Production Control				
110		Precap visual inspection	OCPD 9074			
—		Production Control				
111		Lidding	5005			
112		Mark pkgs	M001			
113		Lead shear & form	M002			
114		Load interstation carriers (use velofoam)	—			
—		Production Control				
115		Interim elec test (+25°C only)	ETS			
—		With histogram tape, print out to engineer				
—		Production Control				
116		Stabilization bake 24 ± 1 hr @ 150°C	OCPD 9012			
117		Temperature cycle	OCPD 9010			
118		Centrifuge	OCPD 9013			
—		Record failures by SN's on reverse side				
119		Leak test — helium	Y021			
—		Record failures by SN's on reverse side				
120		Leak test — gross	Y011			
—		Record failures by SN's on reverse side				
121		Load electrical test carriers (velofoam)				

PRODUCTION CONTROL		
122	Interim electrical test with histogram tape	ETS
123	Deliver printout to engineer for burn-in selection	
—	Production Control	
124	Burn-in	OCPD 9015 Append.25
—	Production Control	
125	Final electrical test 25°C with histogram tape	ETS
126	Final electrical test 55°C with histogram tape	ETS
127	Final electrical test 125°C with histogram tape — deliver printout to engineer	ETS
—	Production Control	
128	External visual inspection	OCPD 9069
129	O&RA Buy-off/mark & dot	OCPD 9069
130	Production Control	

Note: ATL 9046 "Assembly Handling Practices" applies throughout

Special Instructions: Record all failures by sta. & S/N on reverse side of this trip ticket.

FIGURE 2.2-10 MX ACT 1 SCREEN TRIP TICKET

## 2.2.5 MPROM LSIC Environmental/Reliability Test Results

During the ACT 1 program, thirty (30) MPROM parts were subjected to long term temperature bias stress (TBS) testing, to establish long term reliability and stability of the part. The electrical conditions included both static and dynamic bias, with a supply voltage of 13 volts for most cases. The temperature was 125C for most of the testing, with an exception of 150C for one set of six (6) parts. In addition, eighteen of these parts were subjected to an additional long term TBS test.

In all, 94,848 device-hours were accumulated. In particular, these were:

set	parts	hours	temp	conditions	lot no.	dates
1.	6	3008	150C	12V, Static	3043	Sep 76-Feb 77
2.	6	2700	125C	13V, Dynamic	3169	Jan-May 77
3.	6	1700	125C	13V, Dynamic	3175, 6	Feb-May 77
4.	6	1700	125C	13V, Static	3169, 75, 6	Mar-Jun 77
5.	6	1000	125C	13V, Static	3169, 75, 6	Mar-Jun 77
6.	18	1900	125C	10V, St & Dy	above	Sep-Nov 77

Some typical results are shown in figures which follow. Figure 2.2-11 shows the stability of access time for set 1 above, over 3008 hours at 150C. The access time for the slowest output of the four, for the slowest bit, is shown as TDO. The longest delay time for the Data Ready output is shown as TDR with dashed lines. Figure 2.2-12 shows the same data plotted separately for each of the six (6) parts, in contrast to the average and range at each time of measurement, for the data output access time only. The stability of threshold voltage for the p- and n-channel test transistors is shown in figure 2.2-13. Data for sets 3 and 4 is shown in figures 2.2-14, -15, -16, and -17, with both DO access time and threshold voltages vs hours out to 1700. Figure 2.2-18 shows the same data as 2.2-16, but is plotted for each part separately, to show individual part behavior. In most of these figures for access time, an expanded scale is used, magnifying the changes that were observed. The repeatability of the Macrodata 154 automatic tester was about  $\pm 2$  nanoseconds.

The data shown indicates reasonable stability for these developmental devices. Over all six groups tested, with 94,848 device-hours at or above 125C, there were two failures and several parts which showed shifts in access time beyond  $\pm 10$  nanoseconds. But these were the exception; Most of the parts showed good stability.

In a continuation of the ACT 1 program, after all activity on the MPROM had been completed, some modifications to the process were made. Of special note is the change in nitride deposition, from the APCVD used on all earlier work to the LPCVD, for uniformity and repeatability (see section 3.3.2.2). Also, an anneal after gate oxide deposition was omitted, with indications of improved stability. Although these modifications were developed while emphasis was on the MNOS/SOS memory parts, the resulting process is suitable for CMOS/SOS parts such as the MPROM, see section 3.3.4 "CMOS/SOS Process Sequence" with references to 3.3.3.

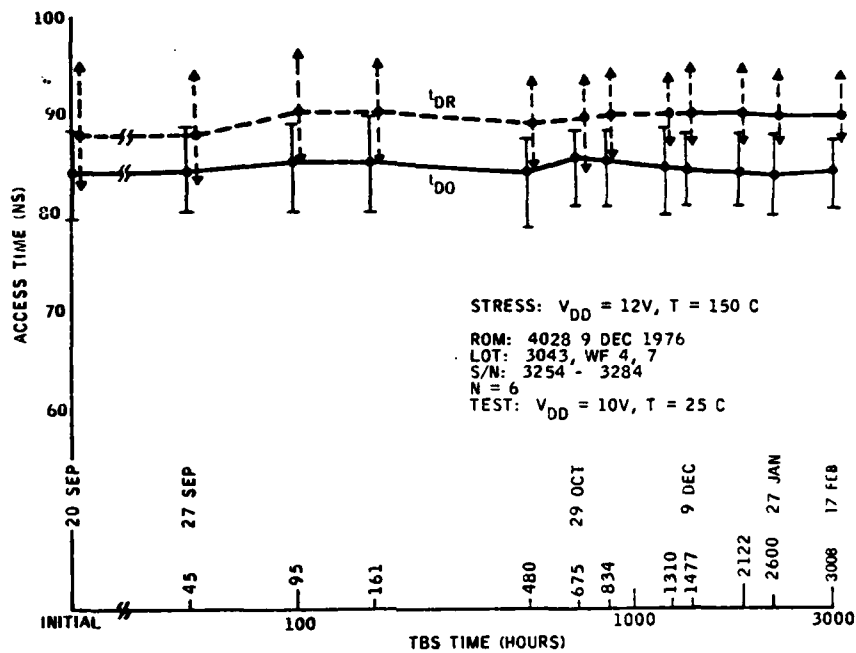


FIGURE 2.2-11 ROM: ACCESS TIME AFTER STATIC TBS

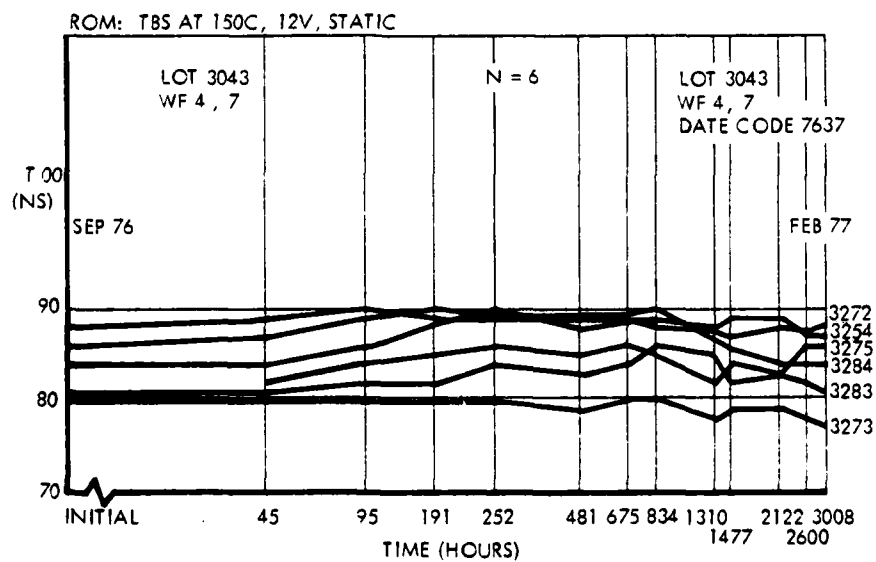


FIGURE 2.2-12 ROM: TBS AT 150C, 12V, STATIC

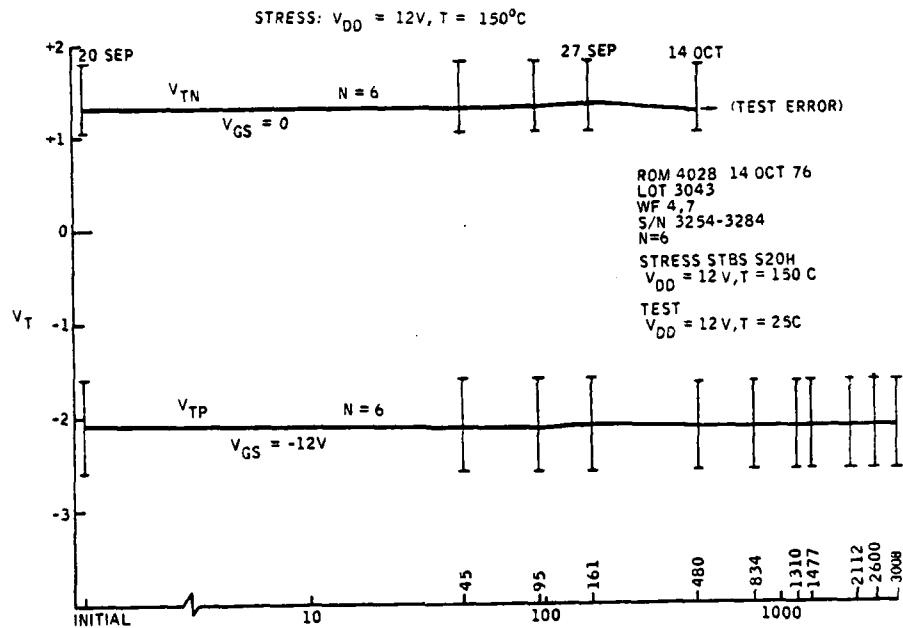


FIGURE 2.2-13 ROM:  $V_{TN}$  AND  $V_{TP}$  AFTER STATIC TBS

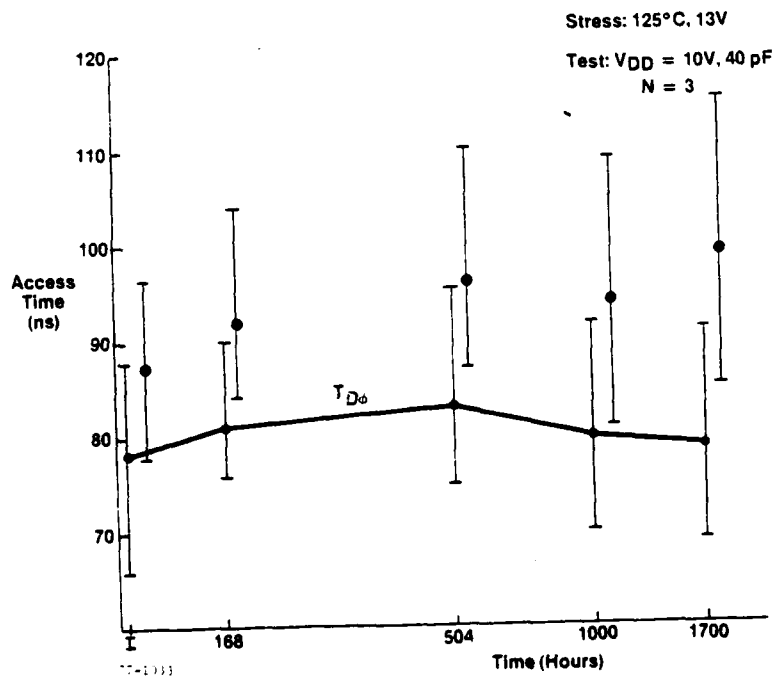
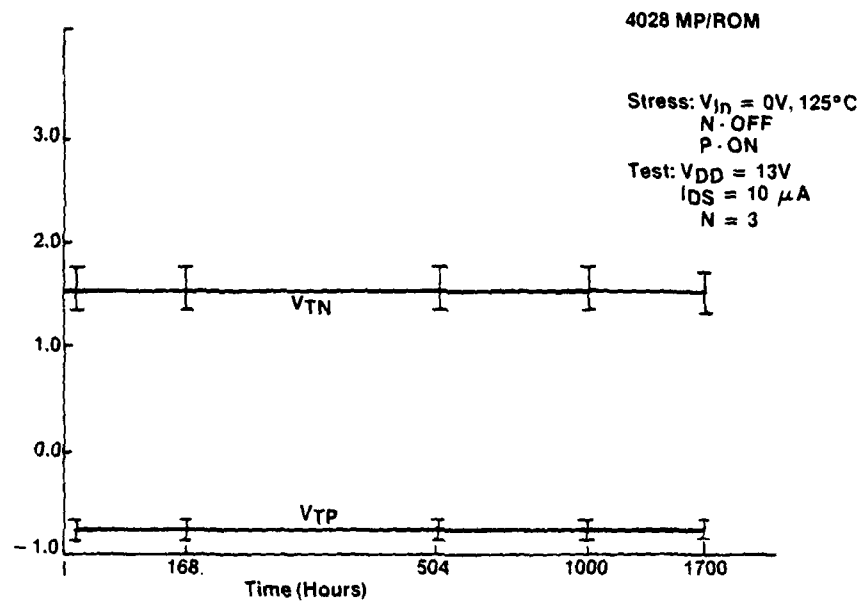
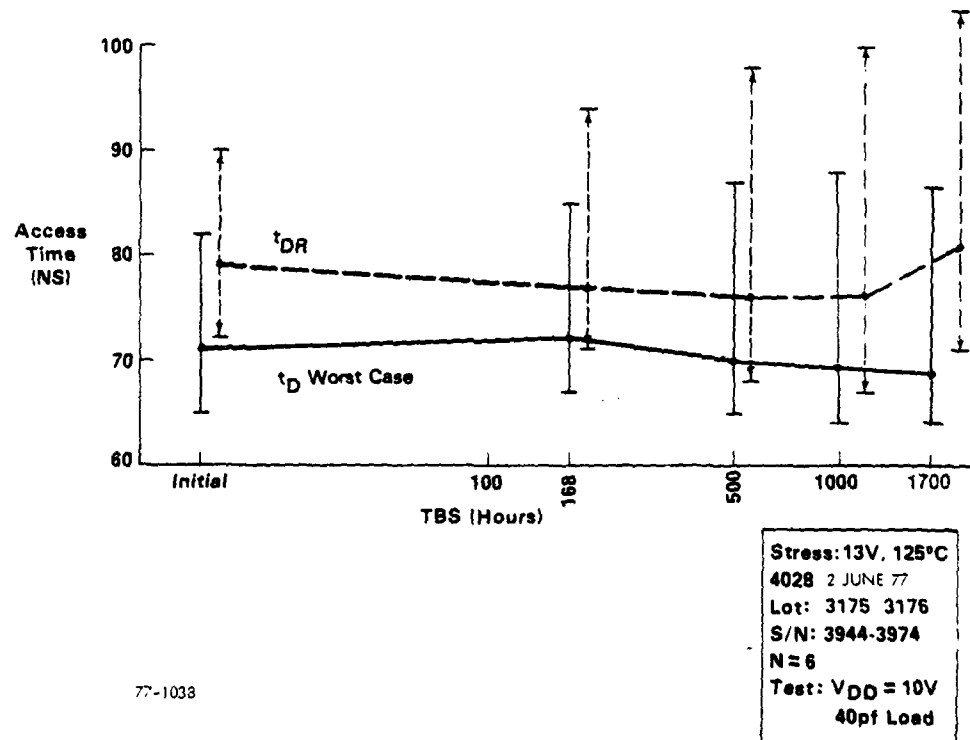


FIGURE 2.2-14 ACCESS TIME VS STATIC TBS ( $\overline{CS} = 0$ )



77-1034

FIGURE 2.2-15  $V_T$  VS STATIC TBS ( $\overline{CS} = 0$ )



77-1038

FIGURE 2.2-16 ROM: ACCESS TIME AFTER DYNAMIC TBS

52348

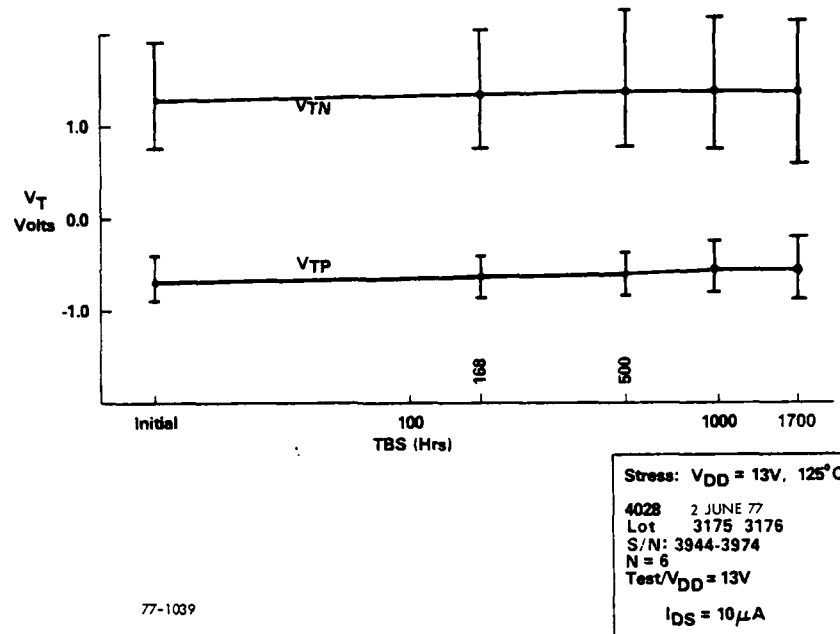


FIGURE 2.2-17 ROM:  $V_{TN}$  AND  $V_{TP}$  AFTER DYNAMIC TBS

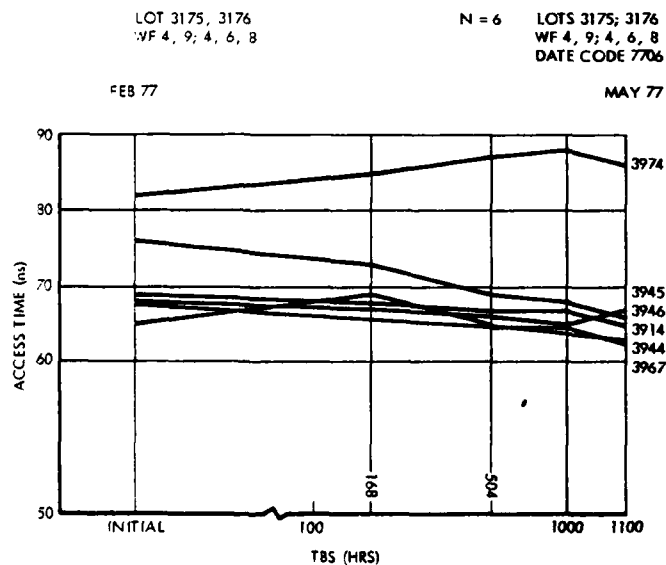


FIGURE 2.2-18 ROM: TBS AT  $125^{\circ}C$ ,  $13V$ , DYNAMIC

Some CMOS/SOS 4007 (triple inverter, revised mask set 4005) lots were run with process variations. Included was the chosen LPCVD nitride and omission of anneals after gate oxide. Devices processed in this manner were subjected to a TBS of 150C, static bias, for 1000 hours. Exceedingly stable n- and p-channel threshold voltage performance resulted, as shown in figure 2.2-19. MPR0M parts processed according to this modified sequence are expected to have the same excellent stability, even better than that shown in earlier access time vs hours TBS figures.

#### 2.2.6 MPROM LSIC Radiation Test

A total of 48 MPR0M parts were subjected to total dose radiation testing. These parts continued to operate beyond the required total dose, with little change in functional characteristics.

Test results have been described in detail in the design verification report. A good summary is given in figure 2.2-20. It shows the result of the second total-dose-to-failure testing. Parts from three lots were tested. The figure shows worst-case access time (on expanded scale) vs total dose. The enable pulse width was widened somewhat over the original specification value. All parts operated beyond a total dose of "6", with the expected increases in access time. Four of the six parts operated beyond "10" although the access times were shifting more markedly. Performance is clearly acceptable beyond "4.5" for these hardened CMOS/SOS MPR0M parts.

#### 2.2.7 MPROM Design Verification and Development Tests

The MPR0M, mask 4028, was subjected to a series of tests to verify the device design and to characterize the ac and environmental performance of the CMOS process. These tests were separated into two major categories, the Design Verification Tests and the Development Tests. The tests incorporated in these two categories are summarized below.

##### 2.2.7.1 Development Tests

The purpose of these tests was to supplement the design verification, screen, nuclear and environmental tests with data that was required to assure the performance goals of the MX ACT 1 Mask Programmable Read Only Memory, MPR0M/LSIC. The tests detailed in this report were done utilizing the MPR0M laboratory test fixture and the automatic LSIC test system. The measurements were taken at 25C unless otherwise noted. In all cases, the operating conditions of the device under test (DUT) were varied so as to cover what was considered to be worst-case conditions.

For each test conducted, a sufficient number of parts were measured to assure that a satisfactory data base was established. For room temperature tests,

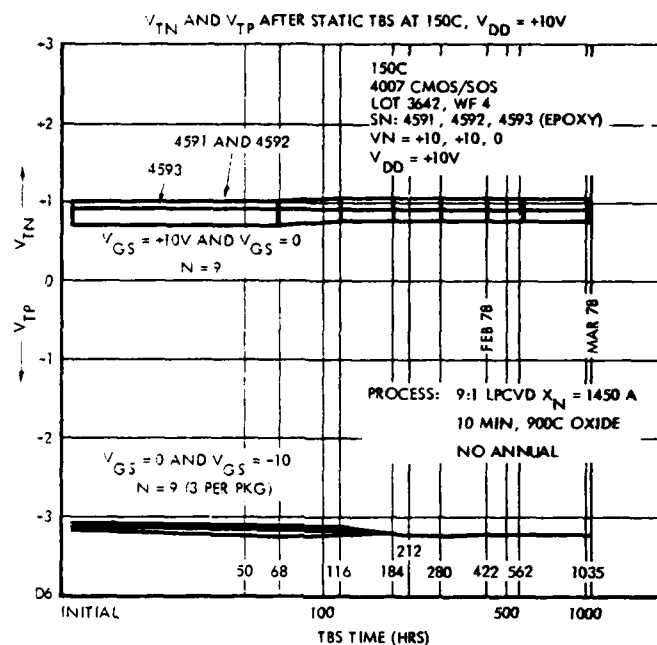


FIGURE 2.2-19  $V_{TN}$  AND  $V_{TP}$  AFTER STATIC TBS AT 150C,  $V_{DD} = +10V$

## FORMAL RAD TEST, SCREENED PARTS

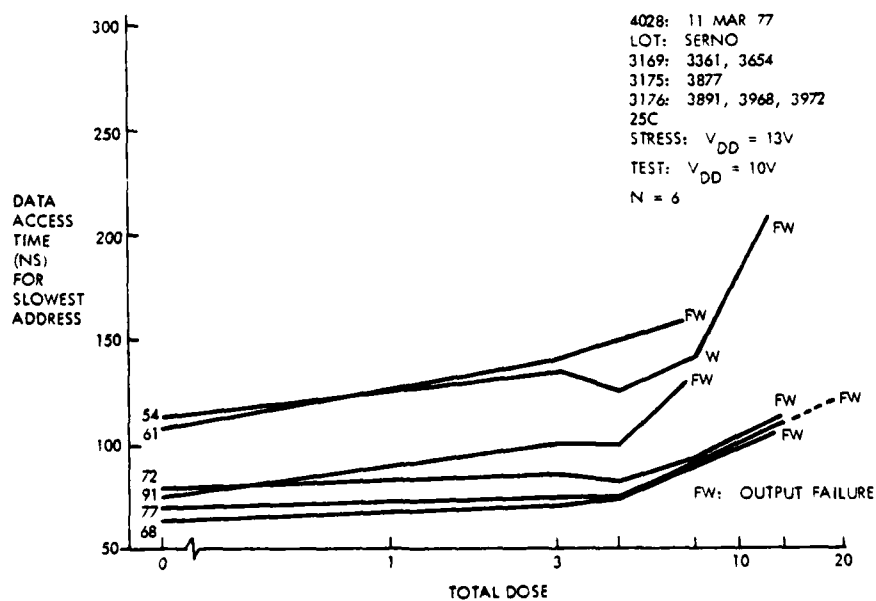


FIGURE 2.2-20 ROM: DATA ACCESS TIME VS. TOTAL DOSE TO FAILURE

pre-rad, either 9 or 10 parts were tested. It was determined that for the development tests a subset of these 10 parts would be exposed to a Co60 dose and their parameters remeasured. A group of 4 parts was selected for this purpose.

A listing of the tests conducted under this test plan is given below. The numbers in parenthesis refer to the appropriate section of the MPROM Development Test Report, see Appendix A.

- a) Pattern Sensitivity: A test designed to measure any dependence of the access time upon the addressing pattern (3.0).
- b) CMOS Level Threshold Voltages: A series of measurement designed to evaluate both the HIGH and LOW state input noise margin, or threshold levels, for the MPROM. Data was obtained both pre and post Rad (Si) (4.0).
- c) Clock/Control Timing: Variations in access time as the enable pulse width and address set-up times were varied has been evaluated for both pre and post Rad (Si) (5.0).
- d) Output Transition Time: A series of measurements were made, pre and post Rad (Si) to evaluate the effects of output capacitive loading upon the output transition time as a function of supply voltage level (6.0).
- e) Output Enable Delay Time: A test designed to measure the delay time from output enable (CS) transition to a valid output logic level. Pre and post Rad (Si) data was obtained (7.0).
- f) Output Disable Delay Time: A test designed to measure the delay time from output enable (CS) to transition to valid output logic level. Pre and post Rad (Si) data was obtained. (7.0).

#### 2.2.7.1 Design Verification Tests

The purpose of these tests is to verify the design and operating characteristics of the 256 X 4 mask programmable CMOS/SOS Read Only Memory (ROM). The data entailed both laboratory testing and automatic testing of the LSI by both Westinghouse and Northrop. The report provided a detailed summary of the tests called for by the SOW and of several additional tests used to extend the characterization of the MPROM. That report is included in an Appendix to this report.

The purpose of the Design Verification Tests was to provide detail data for applications of the MPROM. For each parameter of the MPROM considered, a sufficient number of parts were tested to provide a satisfactory data base, the number of parts being determined by the particular test. The tests are broken down into seven main categories, the numbers in parenthesis refer to the corresponding section of the Design Verification Test Report, see Appendix.

- a) Static Tests (3.0) - a series of tests to evaluate the static or standby mode of operation of the MPROM. Basic tests are for standby power dissipa-

tion and loading effects. This sequence includes:

Standby Power Supply Current	(3.1)
Input Leakage Current	(3.2)
Output Leakage Current	(3.3)
I/O Capacitance	(3.4)

- b) Functional Tests (4.0) - a test sequence to verify proper dynamic circuit logic operation and to measure dynamic power dissipation. This sequence included:

Circuit Verification Test	(4.1)
Dynamic Power Dissipation	(4.2)

- c) Operating Margin Evaluation (5.0) - a series of tests which are used to evaluate the dynamic operating characteristics over a range of temperatures, output loading, supply voltage and read patterns. These tests are designed to detail the operating envelope of the MPROM. Included in this test are:

Read Access Time	(5.2)
Temperature Bias Stress	(5.3)
Output Loading	(5.4)
Power Supply Sensitivity	(5.5)
Pattern Sensitivity	(5.6)

- d) Nuclear Effects (7.0) - testing to verify the radiation hardness of the LSIC. The tests conducted were:

Total Dose - Co60	(7.1)
Transient Dose - FXR	(7.2)

- e) Process Verification (8.0) - tests to evaluate the mechanical integrity for the final MPROM, both in terms of die integrity and package integrity. Evaluation of the following were conducted:

Scanning Electron Microscope	(8.1)
Die Shear	(8.2)
Bond Strength	(8.3)

- f) Input Protection Network Evaluation (9.0) - a sequence of tests to determine the protection afforded each input terminal for the LSIC. These tests included:

Characterization	(9.1)
Pulse Width	(9.2)

- g) Additional Tests (10.0) - further characterization of the output buffer stage was conducted to complete the basic parameter study of the MPROM. In particular, the tests conducted were:

Output Characterization	(10.1)
Output Pulse Tests	(10.2)

Where called upon, the data was obtained over a range of supply voltages and ambient temperatures. The particular ranges and values used were dependent upon the test being conducted. The result of the Design Verification Test Program for the MPROM is a definition of the basic operating envelope of the LSIC.

## 2.2.8 Summary of MPROM Activity

A radiation hardened, high speed mask programmable read only memory (MPROM) has been successfully designed, fabricated, screened and stressed.

This device (Westinghouse mask number 4028) was one of the first hardened CMOS/SOS LSI parts with a substantial amount of reliability screening and stress testing. Figure 2.2-21 summarizes these quantities.

- 0 A TOTAL OF 114 SCREENED, FULLY FUNCTIONAL ROMs WERE PRODUCED. YIELD FOR SCREEN BURN-IN WAS 96%.
- 0 FORMAL TBS TESTS RUN FOR 2000 TO 3000 HOURS HAVE ACCUMULATED 95,000 DEVICE-HOURS
- 0 RADIATION TESTS COMPLETE: TOTAL DOSE (48 PARTS)  
AND GOALS MET TOTAL DOSE TO FAILURE  
NEUTRON (9 PARTS)  
DOSE RATE (23 PARTS)
- 0 DEVELOPMENT TEST MEMO COMPLETE
- 0 DESIGN VERIFICATION MEMO COMPLETE

AS OF AUGUST 1977

## MPROM STATUS FIGURE 2.2-22

The complexity is 1024 bits of mask programmed memory, with one transistor per bit plus about 600 p- and n-channel MOSFETs in the peripheral decoder, detector and driver circuitry. The total is 1624 MOS field effect transistors on a die 148 by 202 mils. The layout used line widths judged to be conservative in 1975 when this program began. A revised layout to line widths now in use would provide a die of half the area. A redesign to twice the capacity, to 2048 bits, would be easily feasible and would still be smaller than the present die size.

The design effort in 1976 utilized circuit simulations to ensure that the differential detection latch could not be upset by high dose rates. A single sided detection circuit could not ensure this performance. Dose rate testing has verified the design approach.

With over one hundred parts through screen, having passed all radiation tests and demonstrated good stability, with 95,000 device hours, this MPROM is judged to be a mature development part. It is ready for small scale production. With a design revision it would be appropriate for full scale production, aimed at supplying program storage requirements in advanced military systems.

## 2.3 THE GENERAL PROCESSOR UNIT, GPU

The program goals required a general processor which would provide the throughput necessary for the MX application. Features such as two-bit-at-a-time multiply were judged to be essential, as well as the usual arithmetic and logic functions, shifts and complement. The layout was desired to be appropriate to a multi-chip assembly, with the shortest paths between elements for shift and carry signals, permitting maximum speed of operation. The characteristics and features of the resulting design effort by Northrop and Westinghouse are shown in figure 2.3-1. A simplified block diagram showing data paths is given in figure 2.3-2.

This highly complex, hardened CMOS/SOS LSIC was successfully designed and fabricated with a resulting die size of 232 by 238 mils. Parts were obtained which executed correctly the lengthy truth table of test instructions and outputs. Interregister cycle times were typically about 120ns. Power consumption was measured at 70mW for operation at the intended 2.7MHz clock rate. Radiation tests showed good performance through a total dose of "3". Figure 2.3-3 summarizes the status of the GPU development effort.

Due to finding limitations, screening and stress testing of the GPU parts was omitted. However, it should be noted that the GPU was designed with the same layout groundrules, identical transistor geometries, many of the same circuits, and the same CMOS/SOS process as the MPROM.

The function of the GPU is described in great detail in a Northrop report numbered A3420-76-63, which is included in Appendix A. The report is titled "ACT I GPU FUNCTIONAL DESCRIPTION".

The design is fully described in the Westinghouse "Report of Design and Simulation, CMOS/SOS, General Processor Unit, Part Number 4027" dated 16 June 1976. It is included in an Appendix to this report. In the paragraphs which follow, brief descriptions are given of the function, the design, and test results.

### 2.3.1 GPU Functional Description

The General Processor Unit (GPU) is a 4-bit slice of a Central Processor Unit (CPU) architecture appropriate to the system requirement. A block diagram of the GPU is shown as Figure 2.3-4 and an explanatory list of GPU Signal Definitions is shown as Figure 2.3-5. The GPU includes four registers, all clocked by the LOW-to-HIGH transition of CL, the system synchronous clock. These registers are: a dual accumulator A1 & A2, an operand OPR and a multiplier MQR register. Associated with each register, and interconnected with many other blocks as well, is a multiplexer; an A MUX driven by the dual A register, a B MUX driven by the OPR, and an MQ MUX driven by the MQR. These provide selection between direct, complement, or shifted signals, or force a ZERO

## CHARACTERISTICS AND FEATURES

- o Four-Bit Slice of General Processor
  - o Dual Accumulator Registers
  - o Data clocked into all registers Synchronously On L-H Transition
  - o Interregister Cycle Time
  - o CMOS/SOS Technology
  - o Two-Bit-At-A-Time Multiply
  - o Lateral Outputs Located Across From Respective Inputs, Drive 10 pf
  - o Four Outputs From ALC And Accumulator Enhance
- |        |         |          |                               |
|--------|---------|----------|-------------------------------|
|        | Pre-Rad | Post-Rad |                               |
| 4-Bit  | <100 ns | <150 ns  | Applicability And Testability |
| 32-Bit | 240 ns  | 360 ns   |                               |
- o Three-State, Four-Bit I/O Port
  - o Drives 25 pf in 20 ns
  - o Power 75 mWatt 2.5 MHz, 12V
  - o Complexity 1150 Transistors
  - o Single Supply: 12V Nominal
  - o 46 Pins Plus 2 Pins For Test Transistors

FIGURE 2.3-1 THE GENERAL PROCESSOR UNIT

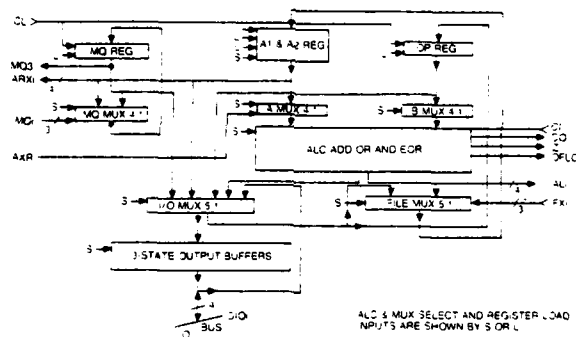
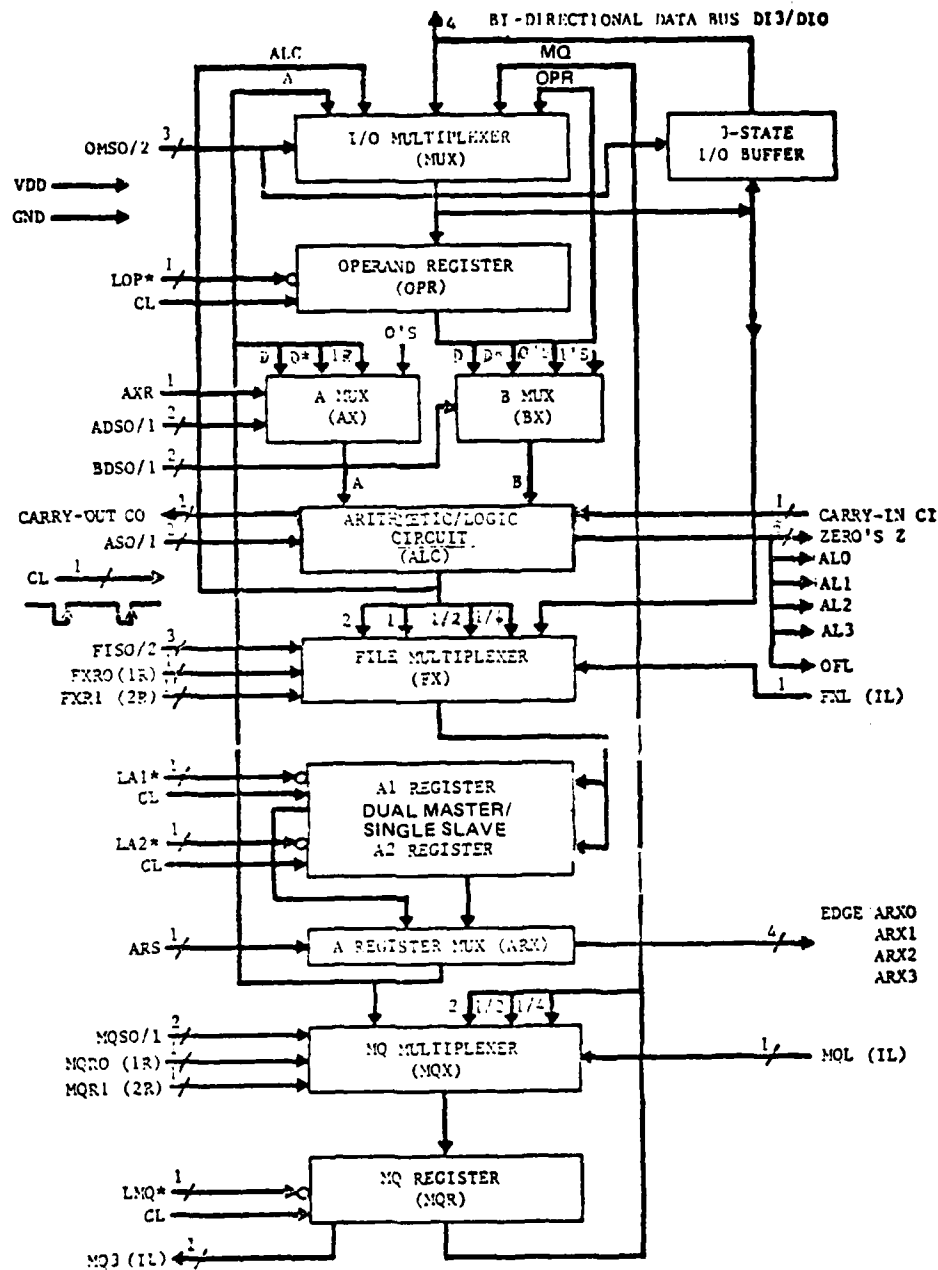


FIGURE 2.3-2 GPU DATA FLOW DIAGRAM

52350

- o Wafer test, latest lot: 46 functional dice, from 8 wafers
- o Two wafers assembled, 15 dice
- o Package test: 12 functional DIPS
  - 5.8 to 9 MHz clock rates measured
  - 172 to 111 ns CLOCK PERIOD
- o Four functional samples delivered to Northrop
- o Design verification data complete

FIGURE 2.3-3 GPU: STATUS



D = DATA  
D\* = INVERTED DATA

FIGURE 2.3-4 4 BIT GENERAL PROCESSOR UNIT BLOCK DIAGRAM  
(2-BIT-AT-A-TIME MULTIPLY COMPATIBLE)  
46 PINS UTILIZED

52351

ADS	ALC A-data input select. Selects the file, inverted files, file right-shifted one place, or all zero's for the A-input to the ALC.
AL0, AL1, AL2, AL3	ALU output port.
ARS	Select accumulator 1, or accumulator 2.
ARX0, ARX1, ARX2, ARX3	Accumulator multiplexer outputs, 0 is LSB
AS	ALC mode select, enables the various modes of operation of the ALC.
AXR	Left edge input required for right shifting the A-input to the ALC.
BDS	ALC B-data input select. Selects the operand, inverted operand, all one's or all zero's for the B-input to the ALC.
CI	Carry input to the ALC.
CL	Clock.
CO	Carry output of the ALC.
DIO(0-3)	3-state input/output data, 0 is LSB
FIS	File input select. Selects the source of the file input: the ALC direct, left shifted, or right shifted, or the I/O multiplexer.
FXRO, FXR1, FXL	Two left and one right edge inputs required to shift the ALC outputs into either file register.
LA1*, LA2*	Load accumulator 1 or 2 respectively.
LOP*	Load operand register.
MQ3	Left edge output signal required for left shifting the multiply-quotient register.
LMQ*	Enables loading of the multiply quotient register.
MQRO, MQR1, MQL	Two left and one right edge inputs required to shift the multiply quotient register.
MQS	Multiply-quotient multiplexer select. Selects the multiply quotient register left shifted one place, right shifted one place, right shifted two places or the file as the input to the multiply-quotient register.
OMS	Output multiplexer select, enables one of the five inputs to the 3-state output gate, to the operand register, and to the file input multiplexer. Also selects the appropriate state of the 3-state output gate.
Z	Indicates that ALC output is all zero's.
OFL	Arithmetic Overflow

FIGURE 2.3-5 GPU SIGNAL DEFINITION

or ONE. A major block in the GPU is the Arithmetic-Logic-Circuit (ALC), which performs Add, AND, OR, and Exclusive OR. The output of the ALC drives a fourth mux, the File MUX FX, which provides direct or shifted outputs.

Appropriate mux selections of the data paths between the four registers and the ALC provide all necessary arithmetic and logic operations including 2-bit-at-time multiply. By means of buffered outputs from the registers and ALC and corresponding inputs to the mux's and ALC, data is transferred to and from adjacent GPU 4-bit slices of the CPU. These paths permit all operations with any multiple-of-four-bit word length. Speed of the arithmetic operations is dependent upon word length because carry must propagate from the first GPU to the last. Logic operations run at a speed which is independent of word length.

The fifth mux, I/O MUX, selects the 4-bit data path to be outputted from the GPU via the 3-state output buffers to a 4-bit bi-directional data bus. The I/O MUX also causes deselect of the 3-state output buffer and admits input data from that same 4-bit data bus.

This CMOS/SOS LSI part requires a single  $V_{DD}$  supply voltage, nominally +12V. All inputs respond to CMOS levels and all outputs drive at CMOS levels. Forty-six (46) pins are required for the inputs, outputs, power and ground. It is designed to operate with a supply voltage range of 10 to 13V, over the full -55°C to +125°C ambient temperature range. The design ensures operation before and after the required total radiation dose and through the required dose rate.

The GPU is capable of being cascaded to construct longer word lengths. It has the necessary storage capacity and data paths to accommodate 2-bit-at-time multiply, non-restoring divide, and floating-point algorithms from a series of micro-programmed inputs. Timing is fully synchronous with single-phase clocking. All control inputs and data inputs and outputs change on the rise of the system clock (CL).

In the paragraphs which follow, additional description is given of the registers, the data path control by means of the multiplexers, and the arithmetic-logic circuit (ALC). The section which follows these paragraphs discusses the circuit design and simulation.

#### 2.3.1.1 Registers

The four registers operate as standard master/slave bistable circuits. The condition of the slave units changes on the rise of the CL, provided the register has been enabled.

2.3.1.1.1 The Operand Register: This register normally holds the operand from memory during the execution of an instruction. The control for loading the operand register is a single wire, called LOP\*. When LOP\* is false and

CL rises, the data present on the I/O multiplexer output is clocked into the operand register. One of the five data sources, as specified by the I/O multiplexer coding, can be selected as input data to the operand register.

**2.3.1.1.2 Accumulators A1 and A2:** These two working registers, are loaded from the file multiplexer outputs under the control of two separate control wires. These two control functions are called LA1\* and LA2\*. When these inverted load controls are low, the respective register is changed on the rise of CL.

**2.3.1.1.3 The Multiply Quotient Register:** The MQR is used to hold the multiplier during multiply, the lower half of the double-length dividend during divide, or the lower half of double-precision numbers during double-precision shift operations. This register is loaded from the MQ multiplexer outputs when the inverted load MQ register control signal is low.

#### 2.3.1.2 Data Path Control

Data paths are coded through six multiplexers and an ALC. Fifteen bits of control are required to effect data selection through the multiplexers and to control the ALC.

**2.3.1.2.1 I/O Multiplexer:** This multiplexer selects one of five inputs to be routed to the operand register, the three-state I/O buffer, and the file multiplexer. These control bits specify the input selection and the three-state buffer control. The MSB control the three-state I/O buffer. The other two bits select the output of the I/O mux, Accum mux, OPR, or the ALC.

**2.3.1.2.2 The Accumulator Multiplexer:** This ARX selects one of two working registers (A1 or A2) to be routed to the ALC A input mux and to the MQ mux. A single bit controls this selection.

**2.3.1.2.3 The A Multiplexer:** The A Mux selects one of four inputs to the A part of the ALC. The selectable inputs are all zeros or data from the A register: direct, complemented, or shifted right one bit.

**2.3.1.2.4 The B Multiplexer:** The B Mux selects one of four inputs to the B port of the ALC. The selectable inputs are: all zeros, all ones or data from the OPR: direct or complimented.

**2.3.1.2.5 The File Multiplexer:** The FX selects one of five inputs to be routed to one of the two file registers (i.e., A1 or A2). The selection is controlled by a three-bit field and is specified as follows: The inputs are the I/O mux or the ALC output: direct, shifted left one bit (i.e., X2), shifted right one bit ( $\div 2$ ) or two bits ( $\div 4$ ).

2.3.1.2.6 The MQ Multiplexer: The MQX selects one of four inputs to the multiplier/quotient register. The inputs are the output of the Accum or of the MQR shifted left one bit, right one bit, or right two bits.

## 2.3.1.2 ALC Cell

The ALC cell performs four functions on the data at the A and B ports: the logical bit functions AND, OR, exclusive OR, and the arithmetic function ADD. Both equal zero (Z) and overflow (OFLO) outputs are mechanized to effect detecting these conditions.

The flow of information within the ALC is depicted in Figure 2.3-6. The inputs at each of the four stages feed the first "exclusive OR" to form the modulo 2 sum of each stage. The output of the first exclusive OR is then summed with the input carry to produce the desired sum output. The logical bit functions or the sum, as selected by the control, are outputted through a final OR stage. The logic implementation of the ALC in the actual LSI is shown in figure 2.3-7.

## 2.3.2 GPU Circuit Design and Simulation

In order to ensure the post-radiation operation of the GPU part in a 125C environment, computer simulation of the circuitry was carried out using the ISPIICE circuit analysis programs. The ISPIICE simulations utilized the models and parameters as discussed in the CMOS design section 2.1. This section will discuss the results of those simulations for several circuits of the GPU. The simulations in this section are all for post-radiation, 125C operation, with  $V_{DD}$  equal to 10V. Any exceptions to this will be noted in the text. Additional simulations are reported in the GPU Design and Simulation Report.

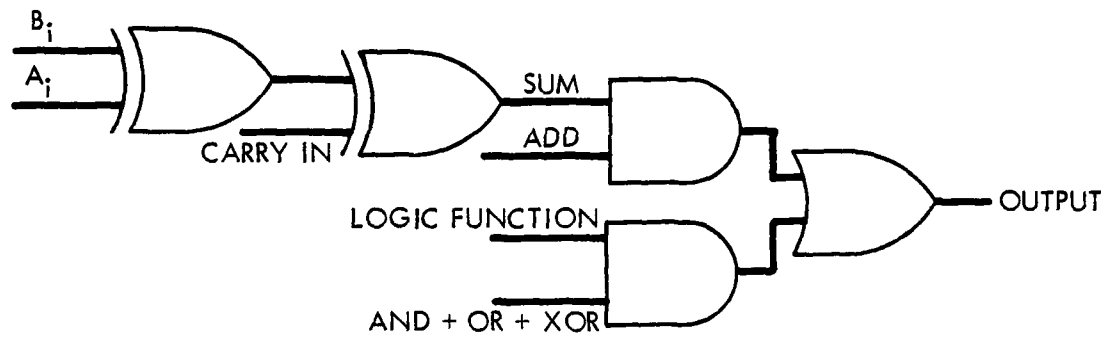


FIGURE 2.3-6 ALC CELL DATA FLOW

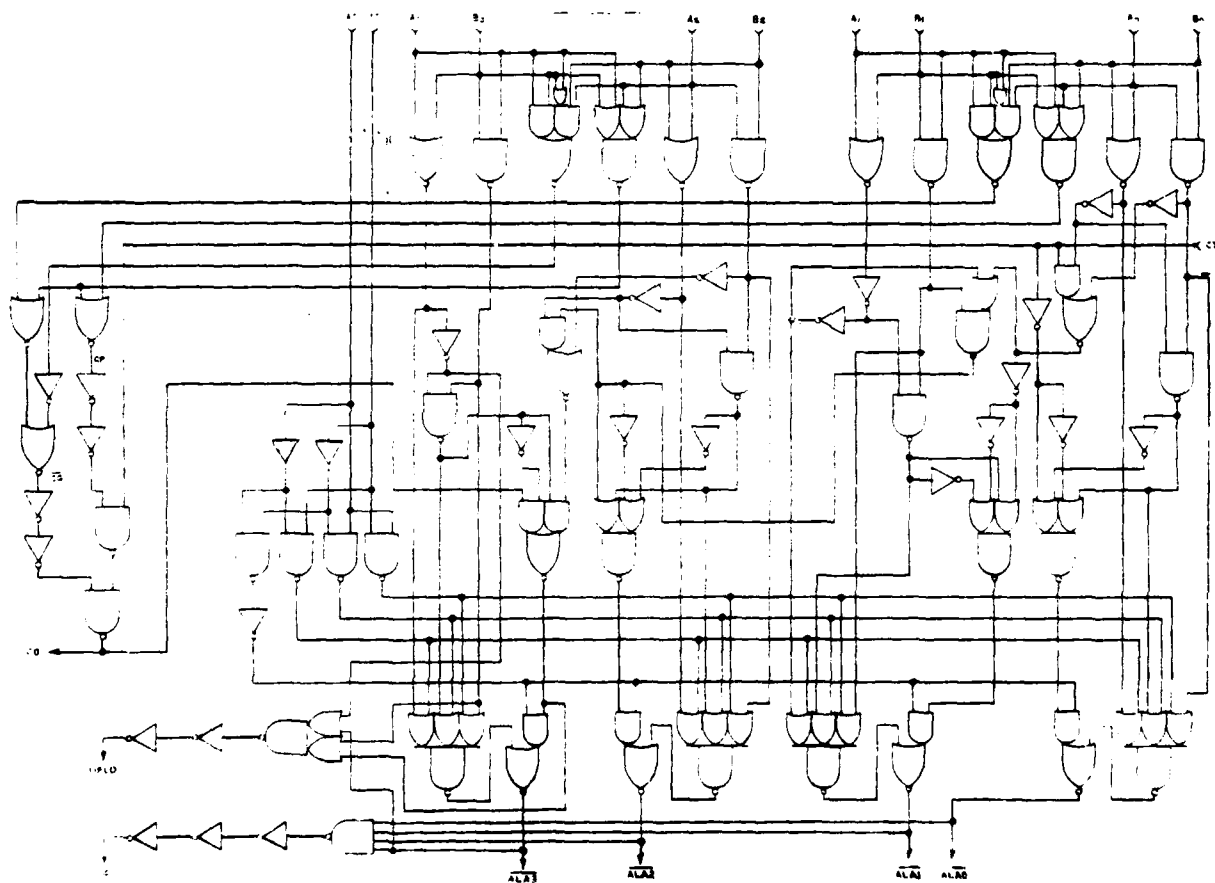


FIGURE 2.3-7 LSI GPU MASK NO. 4027 ALC

## 2.3.2.1 Registers

The registers are implemented using two latch circuits in series operating as master and slave. The latch circuit uses two inverters in series with transmission switch feedback and data input.

The master is designed with minimum size transistors at the input to minimize the input capacitance. Each succeeding inverter stage through the master and slave increases in size with the output of the slave capable of driving 1.0 pf. The clock control and additional buffering may differ for each register.

The master and slave, as shown in Figure 2.3-8, were simulated together to find the worst-case propagation delay for the slave output (Q) with respect to the slave clock (SCL) and the data setup time of the master. As shown in Figure 2.3-9, the delay for the slave output is 25 nanoseconds (ns) and the setup time of the master, from data in to the output node, is 24ns.

**2.3.2.1.1 Operand Register:** Logic schematic of this cell is shown in Figure 2.3-10. Loading of the register is dependent on the state of the Load Operand (LOP) input which is active low. This input controls the clock to the master. The slave clock is buffered to equalize the delay.

The output load, presented by the input capacitance of the I/O Multiplexer and B Data Multiplexer (B MUX), exceeds the 1.0 pf drive capability of the slave output. A two stage buffer was added. The typical propagation delay for each inverter stage when designed for a 10ns transistion, as these were, is 9ns.

**2.3.2.1.2 A1 and A2 Registers:** These A registers (Figure 2.3-11) are configured as one cell using two master circuits and a single slave circuit per bit. The slave has two input transmission switches which are controlled by the state of A Register Select (ARS). By using a NOR gate in one circuit and a NAND gate in the other, the transmission switches turn off and on in unison, thereby reducing the risk of data upset.

To prevent overloading of the slave latch output (AR), four stages of buffering were required with loads being connected on a priority basis.

## 2.3.2.2 Multiplexers

Multiplexing is accomplished by transmission switches with appropriate control and complement control signals. The same size of the transmission switch is used in all multiplexers, with output buffering added.

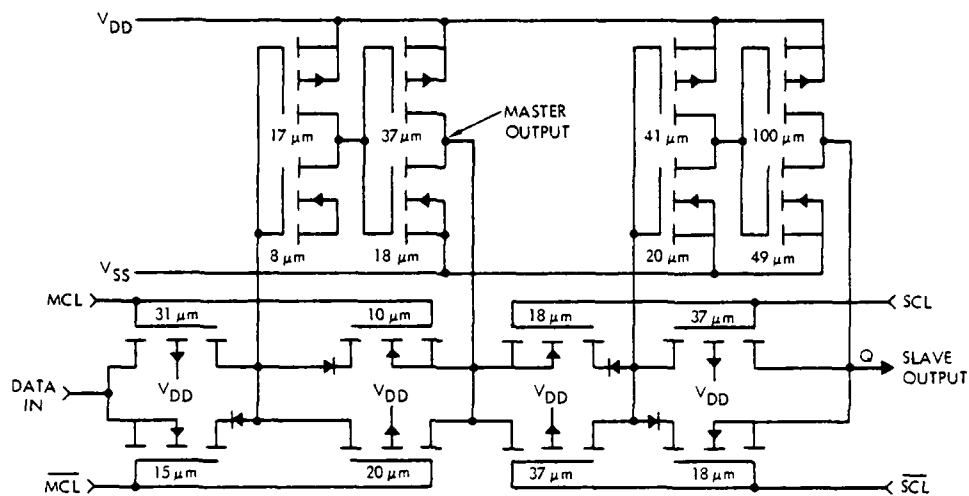


FIGURE 2.3-8

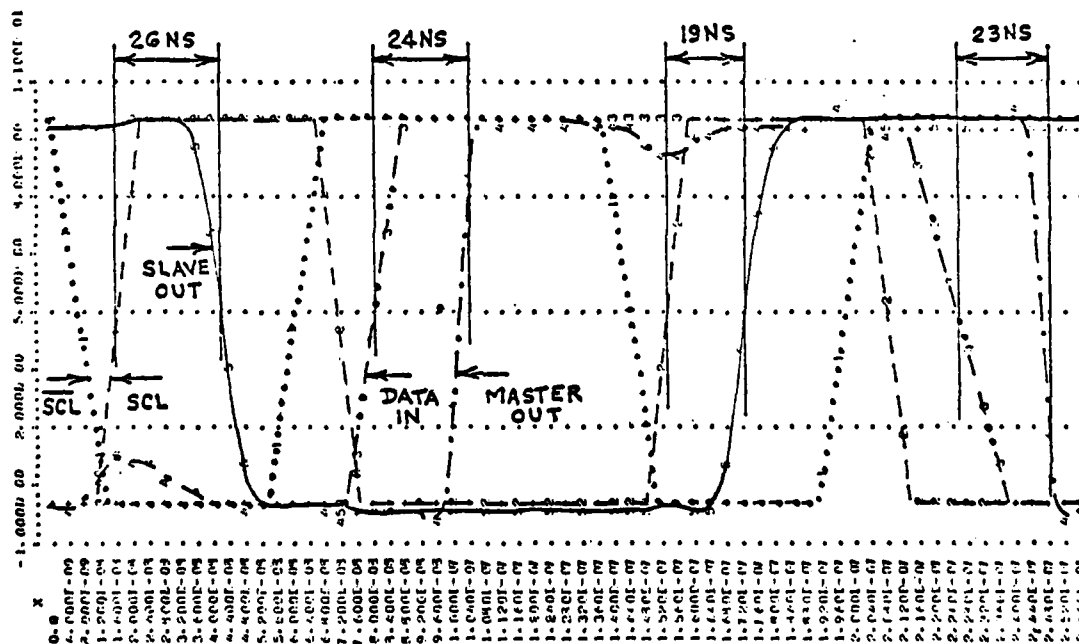


FIGURE 2.3-9

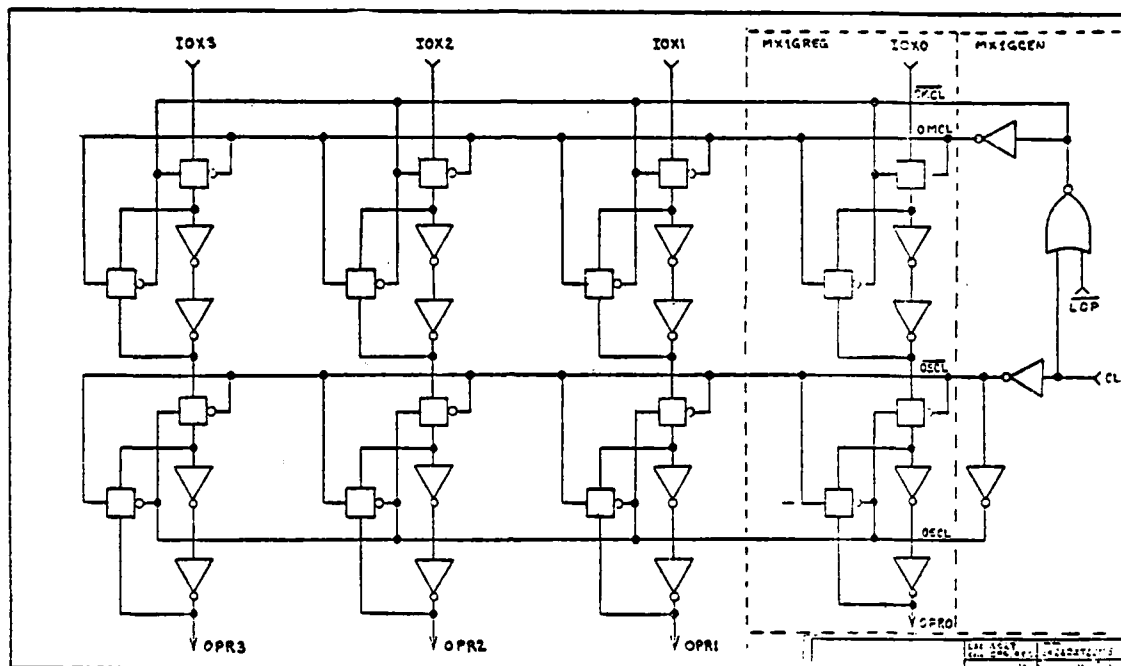


FIGURE 2.3-10

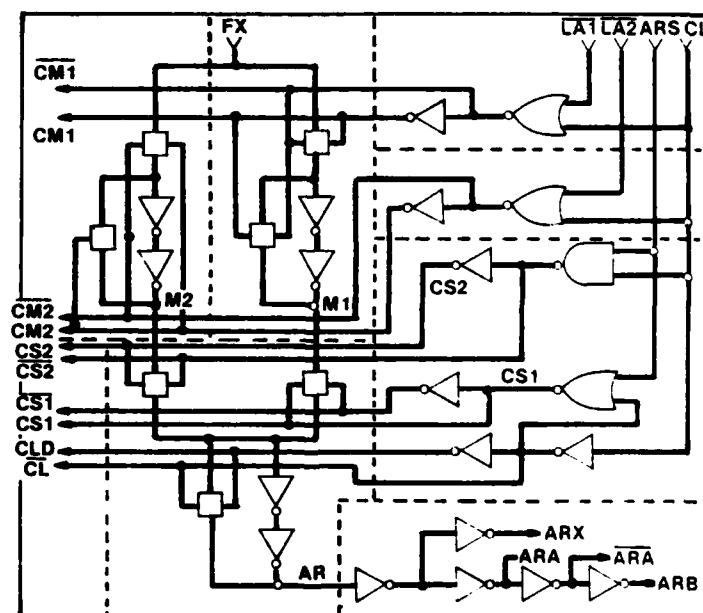


FIGURE 2.3-11 GPU: A REGISTERS LOGIC

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The I/O multiplexer is used for selecting the data to be put on the DATA BUS via the 3-state I/O buffer as well as providing the input data path for the GPU when the I/O buffer is in the high impedance state. Logic schematic representation of this circuit is shown in Figure 2.3-12.

Since this is a 5:1 MUS, it is necessary to use three-input NAND gates for the mode select decode. A simulation of this circuit shows a propagation delay of 42ns. A simulation of data through the transmission switches and the buffers shows a propagation delay of 26ns from the ALC input to the buffer output IOX.

#### 2.3.2.3 Arithmetic Logic Circuit (ALC)

A Logic diagram of the ALC is shown in Figure 2.3-7. This gives an overall view of how the functional blocks are interconnected. Circuit descriptions are covered in the paragraphs to follow.

2.3.2.3.1 Carry Out: For intermediate GPU's, the data path of interest is C in to C out (CI to CO). Using the circuitry of Figure 2.3-13, a delay of 20ns results. This simulation included 8.0pf for the parasitic capacitance of the two packages and printed circuit board as well as the input (CI) load capacitance and protect network series resistance in the next GPU. Driving these capacitances at this speed requires the transistors to be very large. This made it necessary to buffer the carry generate (CG) and the carry propagate (CP) signals. Simulations show a delay of 28ns from CG to CO and 26ns from CP to CO.

2.3.2.3.2 ALC Summary: For a 4-bit operation, the interregister signal path is as shown in figure 2.3-14. For a 32-bit add operation, as illustrated in Figure 2.3-15, the primary speed factor limiting is carry propagation. The lookahead gating computes the carry generate/propagate status for the four bits of each GPU and combines it with the incoming carry-in from the preceeding GPU. An exception is in the first GPU (LSB's), whose carry-in is a micro instruction. This delay in the first GPU, of 65ns, is the sum of the AO to CG and CG to CO delays. The generate/propagate status logic sets up in all GPU's in parallel, therefore, the CI to CO of the remaining GPU's is only 20ns.

In the last GPU, the path of interest is from carry-in (CI) to the most significant sum output (AL3), with the A and B bits already settled and combined. This includes the internal ripple carry and a-d logic delay of 54ns and the buffering delay of 30ns for 10pf load and a transistion time of 20ns.

The sum of these delays for a 32-bit (8-GPU) add is 268ns, from AB data into the ALC to MSB sum output from the ALC. This is a major part of the time required for an 8-GPU inter-register cycle.

For a logical operation (AND, OR, or EOR), the total number of bits of GPU's is immaterial; the total delay is within each GPU and the delays in all GPU's are accomplished in parallel. The worst-case delay for a logical operation is 82ns, from AB input data to ALA output.

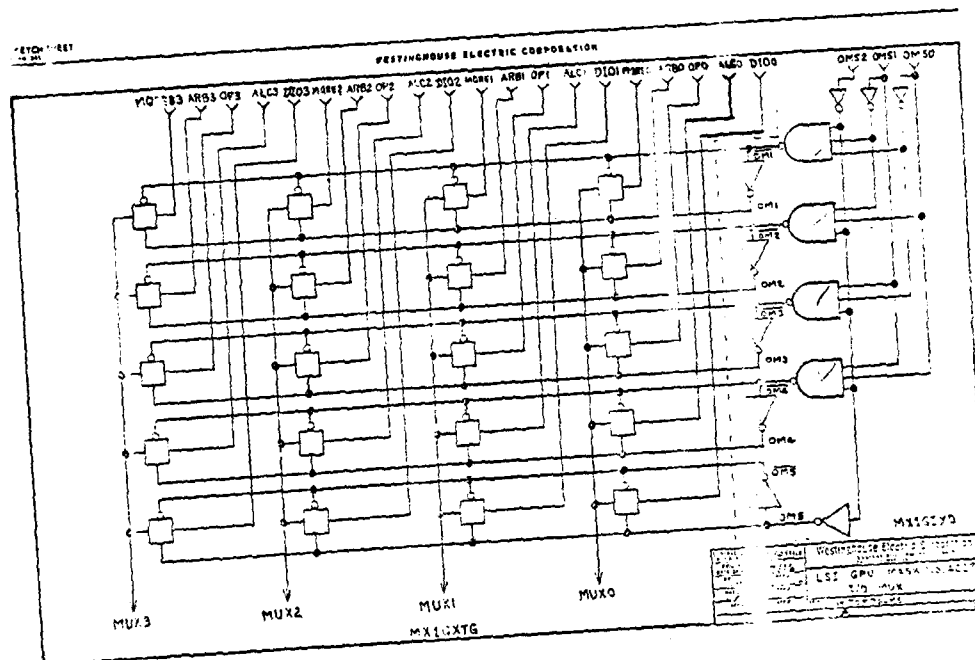


FIGURE 2.3-12

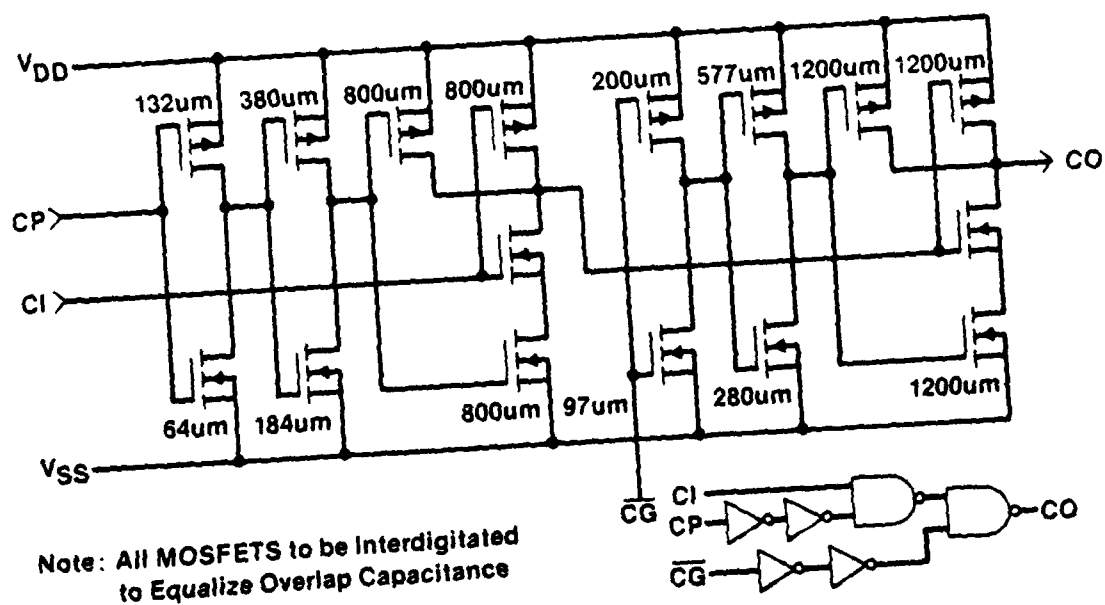


FIGURE 2.3-13 GPU: CARRY IN-CARRY OUT

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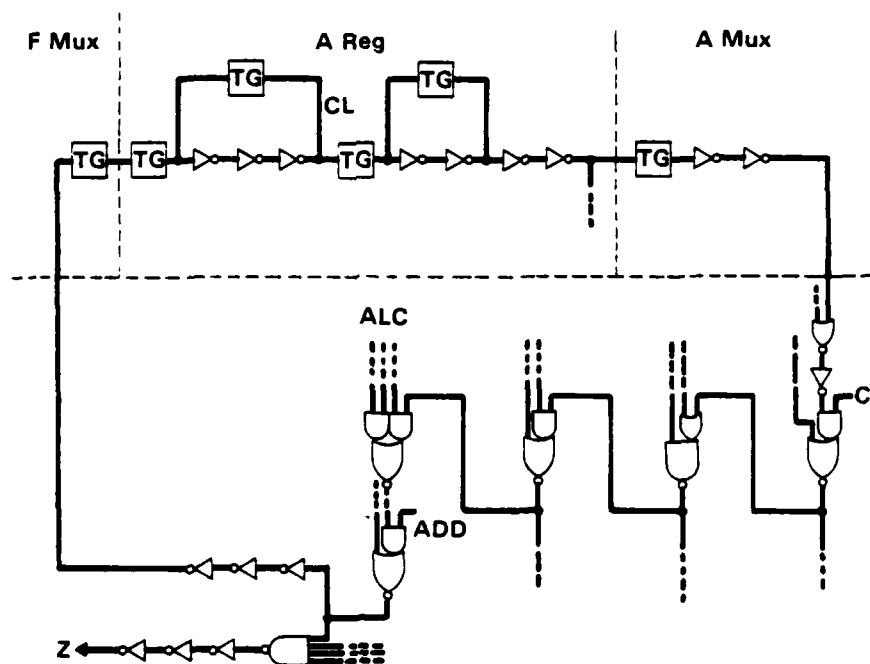
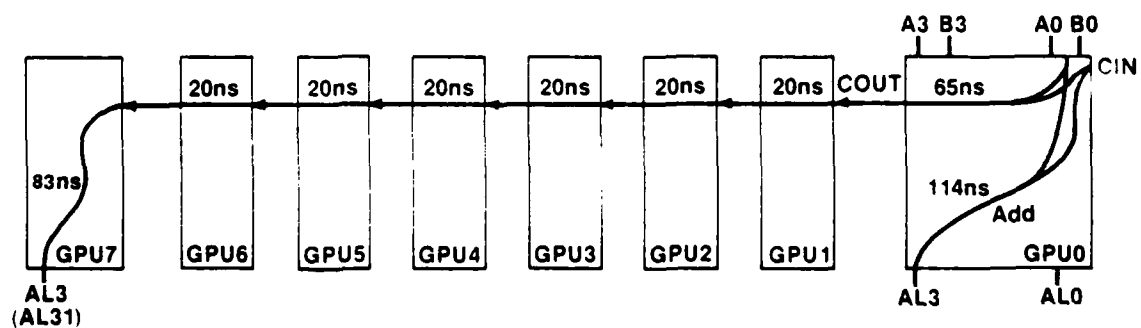


FIGURE 2.3-14 GPU: INTERREGISTER SIGNAL PATH - 18 TRANSITIONS  
ZERO DETECT SIGNAL PATH - 17 TRANSITIONS



Delay From ALC Inputs to ALC Buffered "Edge" Outputs  
AO & BO Inputs to AL31 Buffered Output, Full Carry: 268ns  
A & B Inputs to AL Buffered Outputs, EOR: 112ns

FIGURE 2.3-15 GPU: SUMMARY OF ALC PATH DELAYS FOR 32-BIT OPERATION

### 2.3.3 GPU Test Results

The first lot of GPU's completed after design verification yielded 46 functional dice at wafer probe, from 8 wafers tested.

The wafer test yield is 16%, which is quite good for these very complex 232 by 238 mil dice. From two wafers, 15 dice were assembled.

#### 2.3.3.1 Test Methods

The packaged parts were tested according to a Truth Table of 92 steps; 12 parts proved to be fully functional. The Truth Table is subdivided into five sequences of between 16 and 25 steps each. Figure 2.3-16 shows the cells of the GPU which are checked by each sequence. The detailed bit pattern is included in the GPU Specification, included in the Appendix to this report. Separable sequences are possible for this GPU because, as has been shown in Figure 2.3-2, the four-bit outputs from the ALC and the A register are available in addition to the four-bit I/O bus. This feature greatly enhances the testability of this GPU.

#### 2.3.3.2 Test Equipment

Wafer test and package functional test was done on the Macrodata automatic tester. The Truth Table was programmed into the Macrodata data buffer memory and could be run at system clock rate. Characterization testing and some functional tests were done on a GPU Lab Test Set, especially designed for this part, for manually switched tests. The GPU Lab Test Set is shown in figure 2.3-17. It includes an internal clock with adjustable frequency, pulse width, and delay. Toggle switches are provided for all control signals. LED displays show output states, used when the part is operated in a push-to-step clock mode.

	Registers			Multiplexers				Arith-Logic Circuit								3-State I/O Buffer
	A	OPR	MQ	I/O	A	B	FILE	MQ	OR	AND	XOR	ADD	CO	Z	OFL	
Seq 1	✓	✓		✓												✓
Seq 2					✓	✓			✓						✓	
Seq 3							✓									
Seq 4									✓	✓	✓	✓	✓		✓	
Seq 5			✓					✓								

FIGURE 2.3-16 GPU: TRUTH TABLE FUNCTIONAL TEST

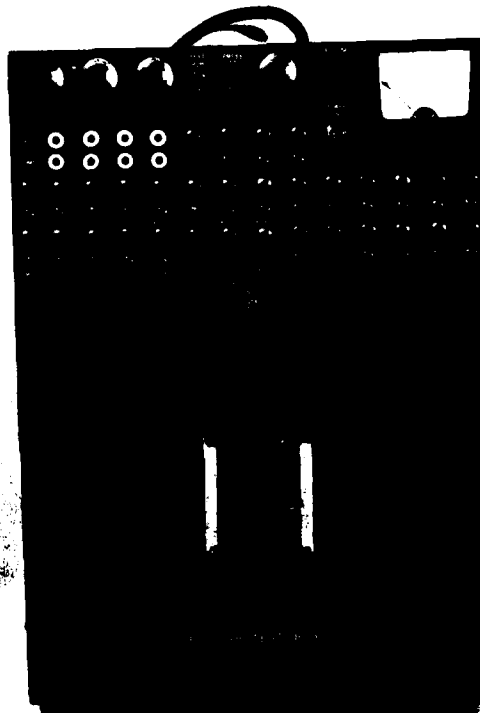


FIGURE 2.3-17 LAB TEST SET FOR THE GPU 4027  
CMOM/S05 GENERAL PROCESSOR UNIT

# NORTHROP

Electronics Division

## 2.3.3.3 Power Consumption

The packaged parts were tested thoroughly and characterized. Power Consumption was measured as a function of clock frequency and supply voltage, with the results shown in figure 2.3-18. At the intended clock rate of 2.7 MHz, power consumption at the nominal 12 volt supply is just under 75 mW.

## 2.3.3.4 Dynamic Performance, Pre-and Post-Rad

A good test of operating speed is the cycle time for an interregister operation. The part is set up in an interactive sequence, with a scope used to monitor the overflow or all zeros output, thereby checking for correct operation. The frequency is increased until an error results, then backed off. Operation at this maximum frequency is rechecked with another pattern, from a static start condition. Figure 2.3-19 shows the results for such a test of four parts, with supply voltage set to the spec minimum of 10V, as a function of total dose. Pre-rad, the cycle times ranged from 74 to 87 ns (13.5 to 11.5 MHz clock rate). Post-rad, at a dose of "1". The cycle times ranged 76 to 105 ns, and at a dose of "3" the cycle times were between 110 and 130 ns, with one part at 200 ns (5.0 MHz clock rate). This atypical part is not included in the range bars and averages at doses of "1" and "3".

The three typical parts were tested at other supply voltages in the specified operating range of 10 to 13 V and at lower voltages as well. The results are shown in figure 2.3-20. The design minimum supply voltage is shown to be quite safe in that even a volt or two below that value the part continues to function with only a moderate increase in cycle time.

Some propagation delays within the GPU are plotted in Figure 2.3-21 vs total dose. They lie within or below the range for simulation results computed for post-rad transistor parameters, which are shown by range bars beside the ordinate. These delays were measured from the clock edge to the 3-state output DIO via the MQ Register and to the Z output via the ALC.

Propagation delays within the GPU appear to be less sensitive to radiation for parts from another lot. Delay times were measured from the B MUX select signal transition to certain outputs, in particular to the data bus DIOi, to the all zero output Z, and to the outputs from the ALC (ALi). Results for pre-rad and post-rad are shown in figure 2.3-22. They show only modest increases at a total dose of "6".

## 2.3.3.5 GPU Summary

Design and fabrication of the GPU LSIC were successful. Fully functional parts were produced and characterized for electrical performance and radiation effects. Results meet or exceeded the design simulations and program goals.

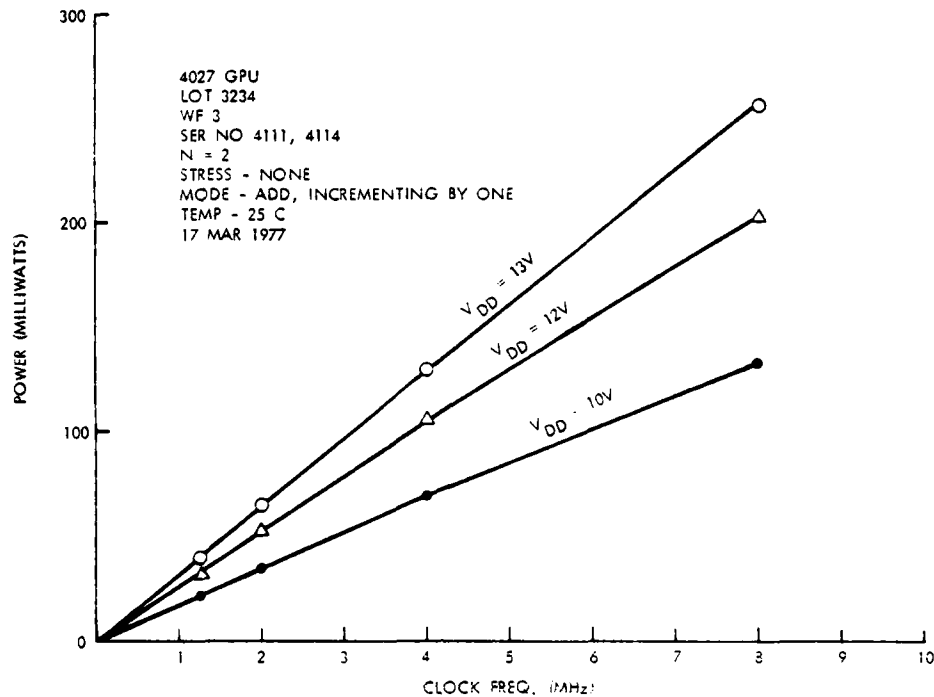


FIGURE 2.3-18 4027 GPU DYNAMIC POWER CONSUMPTION

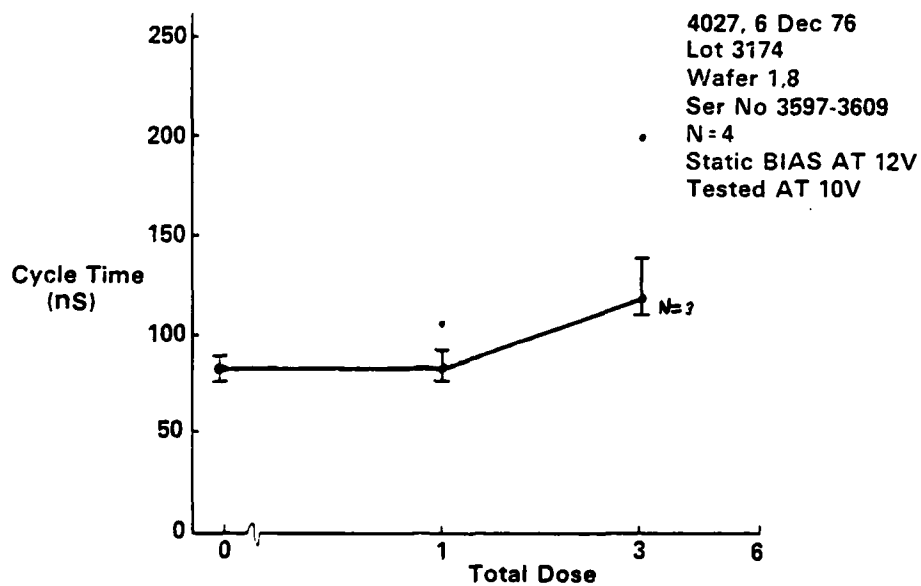


FIGURE 2.3-19 4027 GPU: CYCLE TIME VS TOTAL DOSE  
(ACCUM BY 1 AND ACCUM BY -1)

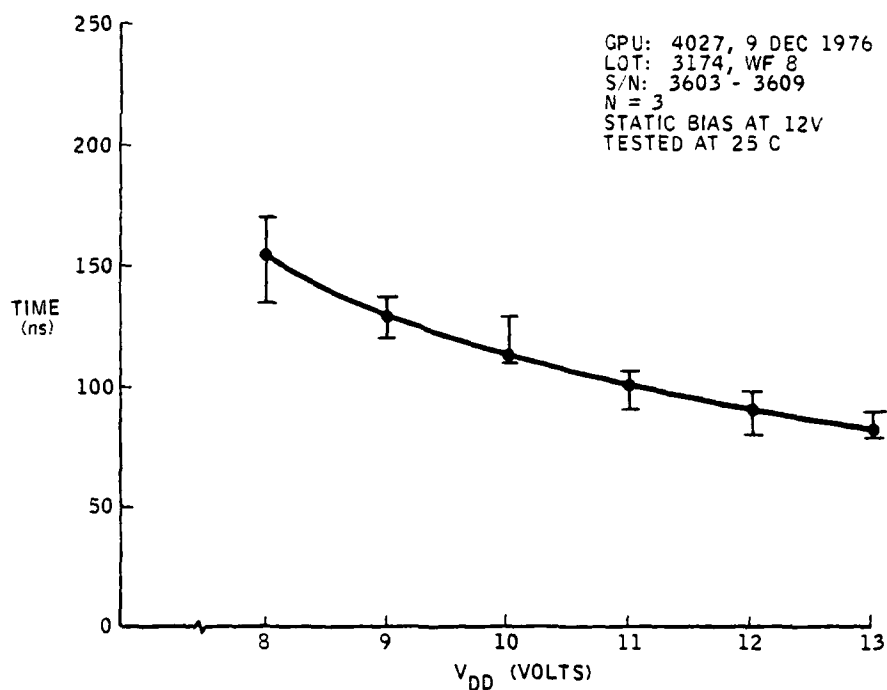


FIGURE 2.3-20 GPU: CYCLE TIME VS  $V_{DD}$  (POST-RAD)

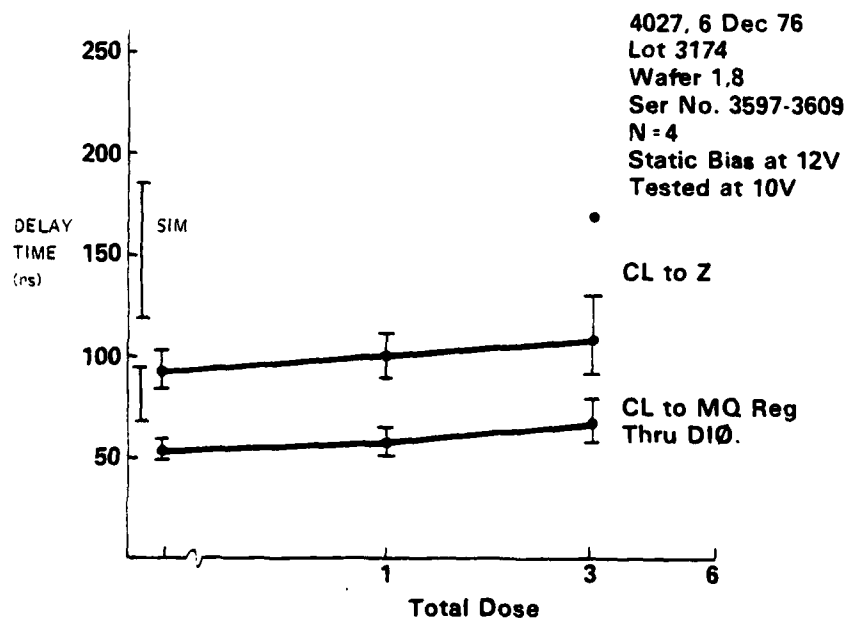
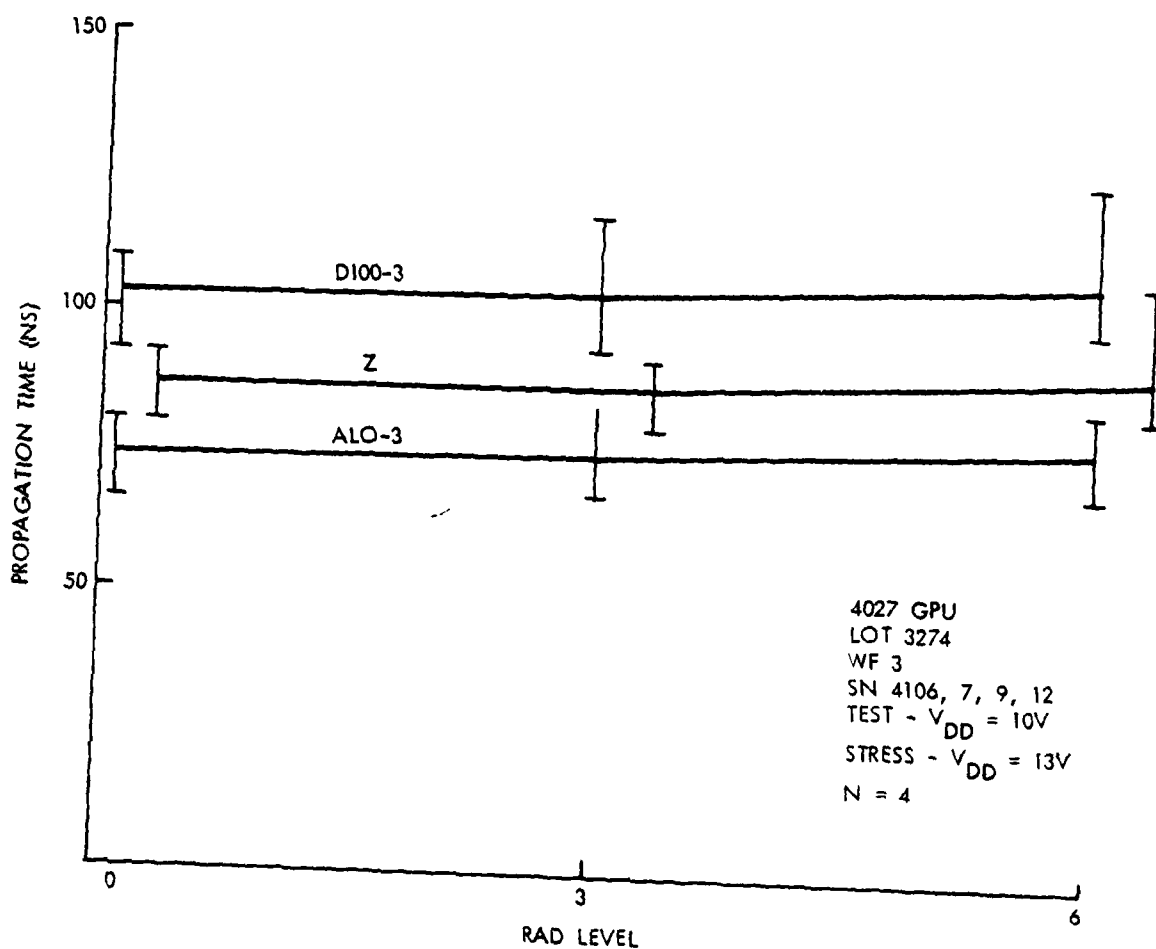


FIGURE 2.3-21 4027 GPU: CL TO MZ AND CL TO Z DELAY VS. DOSE  
 (L TO H AND H TO L)



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FIGURE 2.3-22 4027 GPU SELECTED PROPAGATION DELAYS  
 (FROM BMUX SEL) VS RADIATION, STATIC BIAS

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## 2.4 INPUT/OUTPUT PROTECTION NETWORKS\*

During the course of developing the complex CMOS/SOS logic and MNOS/SOS memory circuits for the MX ACT I program, a reliable input protection network was needed which would withstand usual static discharges that occur during electronic module construction and maintenance. It was desired that these new MOSFET parts could be handled at the die and packaged part level with no more precautions than those commonly used with bipolar parts. Further, these parts were hardened to tolerate nuclear radiation effects, and superior protection must be provided against internally generated EMP transient voltages that might develop with low source impedances. The major emphasis of verification tests was done with all operating potentials on the parts, 12V for CMOS and up to 30 V for MNOS parts. The transition between adiabatic and quasi-adiabatic region occurs near 90 ns, so most of the measurements were made between 100 ns and 1  $\mu$ s. Transient RC zap tests and human equivalents also have time constants in this time domain. Since transients run both ways on interconnecting wiring, tests included both inputs and outputs.

Tests were done on hundreds of inputs and several dozen outputs on the four LSI devices. These devices are large die, 25 to 40  $\text{mm}^2$  (40K to 60K  $\text{mil}^2$ ), so eighteen or more protective networks each about 0.05  $\text{mm}^2$  use only about 0.9  $\text{mm}^2$  or 3 percent of the chip area. The level of protection increases with allocation of more power dissipating area. The chosen approach keeps high-voltage surges at the perimeter of the die, permits inspection with conventional input resistive and leakage current measurements, withstands repeated overvoltage surges without degradation, if kept 20 percent under the failure threshold.

### 2.4.1 Pulse-Test Network

A test jig was constructed to interface the LSI component with a charged transmission line pulser. The design matched the RG-58 50-ohm coaxial cable which determined the pulse-width at about 3.0 ns/ft. A Simulation Physics Pulser Model 25 was used to form the single-input pulse. A 20-ohm current-limiting resistor was added between the LSI terminal and the output of the pulser. This avoided damaging the pulse-forming network

\* For more detail see: "C-MOS/SOS LSI Input/Output Protection Networks," B.T.Ahlport, J.R.Cricchi, D.A.Barth, IEEE Trans. on Elect. Dev., Vol ED-25, No. 8, pp 933-938, Aug 1978. A copy is included in the Appendix to this report.

by reducing somewhat the surge currents that developed when the input resistor ionized into a low conductive path. A low-impedance noninductive divider sampled 0.100 of the LSI input voltage. The LSI input current was simultaneously measured with a CT-2 current probe. The network was constructed over a ground plane, and less than 2.5-in lead dress was used to contact one LSI input or output. Voltage transitions were achieved within 10 ns. LSI power was supplied through limiting resistors, but capacitively stiffened at the zero insertion socket terminals.

Typical waveforms are shown for a +580-V 100-ns-wide input pulse. In figure 2.4-1 node resistor heating first reduces the current until the high-temperature heating causes the current to hook up at the end of the pulse.

Ten repeated low-duty cycle pulses will not change these wave shapes, but just one pulse with 10 percent more input voltage will destroy the input resistor since the low source resistance of 21-ohm does not limit thermal runaway.

#### 2.4.2 Input-Protection Circuit

The thin gate dielectric is usually the weakest region in MOSFET circuits. Depending on process/fabrication/layout details, this region may destructively break down at the gate edges with potentials as low as 40 to 60 V in nominal 800-to-1200-Å-thick silicon dioxide gate insulators. The Westinghouse house designs use diffusion-aligned edgeless gate layouts with a thin 80-Å silicon dioxide layer, then a 1300-Å silicon nitride layer, forming an equivalent gate of 900-Å  $\text{SiO}_2$ . C-V measurements have shown the onset of nitride conductivity at 75 V, with destructive breakdown or threshold shifts requiring even higher gradients. Destructive breakdown typically occurs between 100 and 120 V.

The input circuit design prohibits such large potentials from reaching the MOSFET, and shifts the failure mechanism to the input series resistor. This element can readily be inspected both with a pre-lid visual and packaged electrical screen, and is fabricated with easily controlled and verifiable processes, giving improved quality assurance. The input is built with a double-L attenuator topology, shown in figure 2.4-2. The power density in the p+ diffused resistor  $R_1$  sets the failure threshold.  $R_2$  and  $R_3$  are n+ diffused with half the sheet resistivity of the input, and do not degrade. The clamp diodes are small geometry, about 140-um junction periphery, are ion implanted for breakdown near 18 V with a dynamic bulk resistance of 180-ohm. They are sized not to be the weakest element, the input resistor is the circuit fuse.

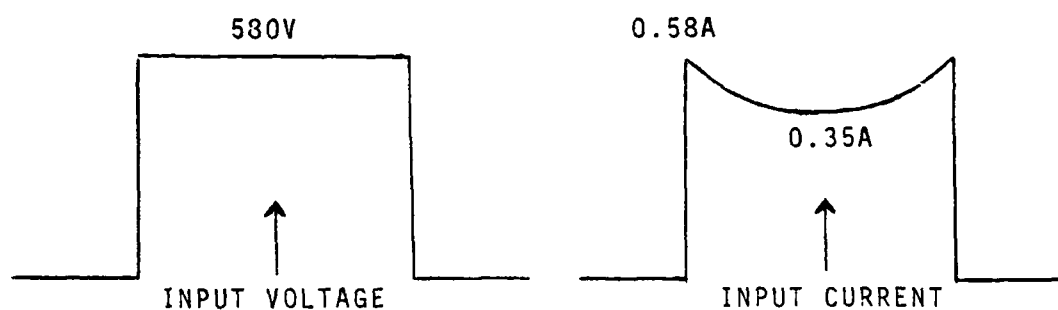


FIGURE 2.4-1 INPUT WAVEFORMS

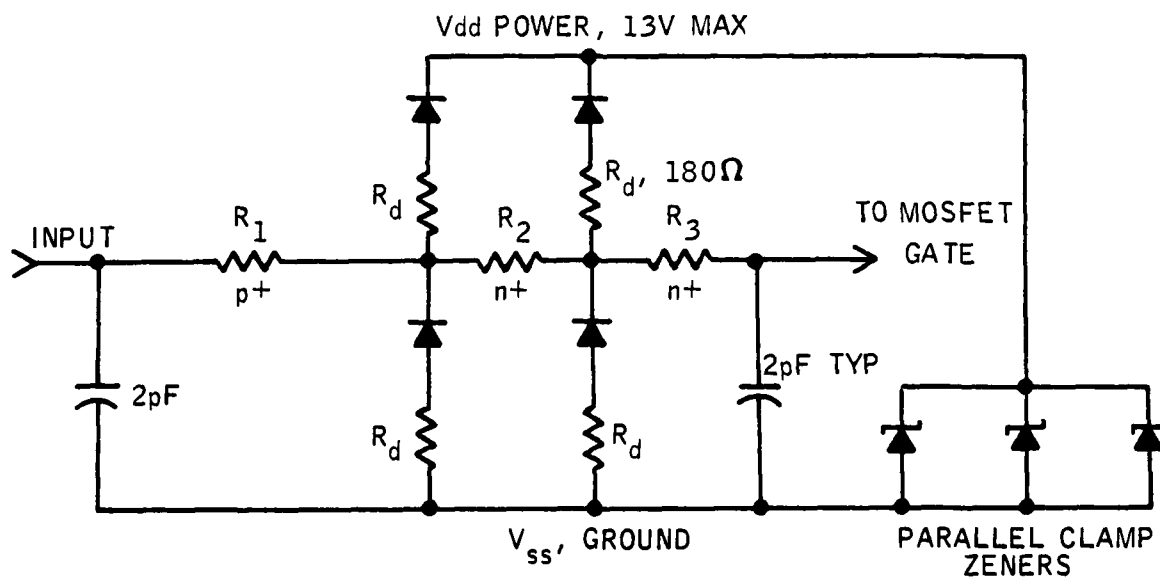


FIGURE 2.4-2 INPUT ATTENUATOR TOPOLOGY

The double attenuator provides a delay to the gate while the first L section clamp diode turns on. The performance is almost symmetrical with input polarities. The metal runs are sized to carry the surges and shunt photocurrents from intense ionizing radiation. The first node reduces a 580-V 100-ns pulse to typically 70 V (worst case 100 V) past the supply voltage. The smaller second attenuator then reduces the gate to body stress to 32 V (48-V worst case). Worst case assumes a diode resistance of 225-ohm. Initially 600 mA of surge current flows, but this drops about 40 percent as  $R_1$  heats. Thus if the input surge comes from a higher impedance, as 1500-ohm in a handling static discharge, the forcing voltage is dropped externally another 900 V, on a pulse of 1500 V for 100 ns is required to cause serious damage.

## 2.4.3 Input-Protection Layout

The layout of the input-protect network is shown in figure 2.4-3. An earlier input-protection layout is shown in figure 2.4-4. The original layout exemplifies several conditions which should be avoided. The small contact at the top of the resistor caused localized heating which induced failure before the rest of the resistor degraded. A conductor path crossed the input resistor at 90 percent of the input potential, and the heated silicon underneath developed a premature arc through to this second signal line. The improved design widened the resistor to 25  $\mu$ m in the crossover region, and crossed at the 50-percent voltage point. No failures have occurred in this wider crossover region. The input resistor  $R_1$  was lengthened and the contact region was widened with a large 0.6 square contact window. A wider short aluminum path connects to the input pad. These changes improved the voltage failure level 1.9 times.

The original input layout, used on the ROM, needed 0.041 mm<sup>2</sup>, the improved layout used 0.054 mm<sup>2</sup>.

Resistor  $R_1$  is sized at 15  $\mu$ m wide so variations in edge etching will not contribute more than 10 percent to the resistance value or local power density. The resistor length is 320  $\mu$ m which gives protection up to 320 V for pulses 1  $\mu$ s wide, or 580 V for pulses 100 ns wide. The p sheet resistivity is about 40-ohm/square.  $R_1$  is 850-ohm  $\pm$ 20 percent,  $R_2$  is about 300-ohm, and  $R_3$  is the sum of internal cross-unders to the remote gate electrode, typically under 200-ohm.

Failure occurs when high temperatures develop an increasingly negative temperature coefficient and the thermal ionization arcs along the center of the resistor, allowing the current to increase several fold. The arc extinguishes at the end of the pulse. Thereafter,  $R_1$  is a fused open circuit. This surge may cause a secondary failure with a thin filament through the junction of the forward-biased clamp diode and a larger destroyed region frequently occurs at corners in the reverse breakdown clamp diode. If the pulse is 10 percent below resistor failure, repeated low-duty cycle single pulses do not degrade the resistance nor increase

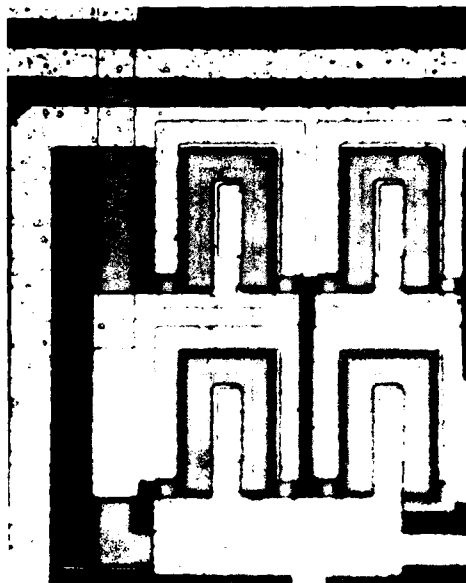


FIGURE 2.4-3 ORIGINAL INPUT PROTECTION LAYOUT

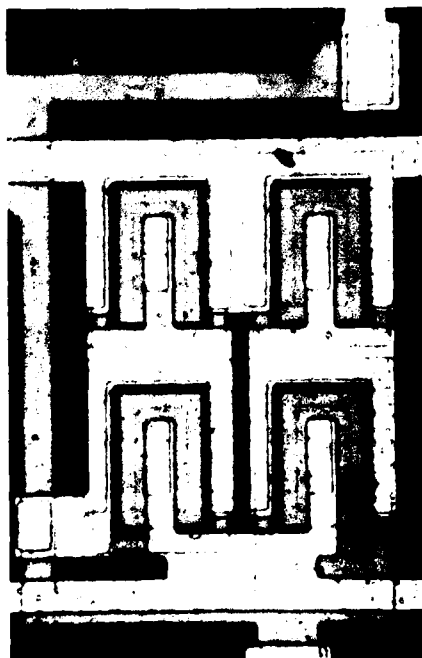


FIGURE 2.4-4 IMPROVED INPUT PROTECTION LAYOUT

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the input nanoampere leakage of the back-biased diodes. If the resistor is not widened at the crossover, the failure threshold will be somewhat lower, since the resistor will heat the silox near  $500^{\circ}\text{C}$  where the aluminum reacts chemically to reduce the silox and develop a catastrophic arc-through.

A typical failure of the original input design after a +325-V, 100-ns-wide pulse is shown in figure 2.4-5 where the input resistor of ROM address 5 has burned open, the tiny heating filament degrading the forward-biased diode cannot be seen, but two corner burnouts of the reverse-biased diode are obvious. No visible degradation ever occurs in the second attenuator stage. For a square pulse, 1  $\mu\text{s}$  wide, the failure current density is about  $3 \times 10^6 \text{ A/cm}^2$  and the energy density is about  $1.3 \text{ J/cm}^2$ , and the power density is  $1.3 \times 10^6 \text{ W/cm}^2$ .

#### 2.4.4 Failure Criteria

Significant degradation was used as the failure criteria. Since LSI devices have many functional characteristics, and degradation of narrow cross-unders in the test samples would cause multiple failures, a thorough parametric and logic test was made between each of the step stress levels. Most of the steps were recorded on high-speed film using a dual trace so the true power could be integrated visually from the E and I waveforms. The Pacific Western Mustang LSI Tester made 200 to 300 parametric measurements on each LSI, between each voltage test group. Step increases near the failure level were about 10 percent in voltage, and ten repeated pulses were made in each test group. An optimum sequence of inputs was determined from the layout, so that multiple input/output failure level data were obtained from the same LSI. Impending negative resistance thermally induced run away frequently was avoided, and the same input could be retested at another pulsewidth.

All input and output high-impedance three-state leakage currents were measured with 10-nA resolution for logic 0 and 1 levels. Degradation criteria were obvious since leakages remained satisfactory and below 100-nA, or jumped over 100-uA when degraded. Input resistances were measured, and changed only a couple percent before a catastrophic opening. Output current source or sink currents changed little until catastrophic failures. Internal logic changes were not found except as related to an input opening. Total power supply currents also did not change until large increases occurred from junction fusing or burnout.

#### 2.4.5 Input Failure Levels

The failure voltage as a function of low-duty-cycle pulse-width is shown in figure 2.4-6 for the earlier 6013 PSM, and for the improved 6023 PSM.

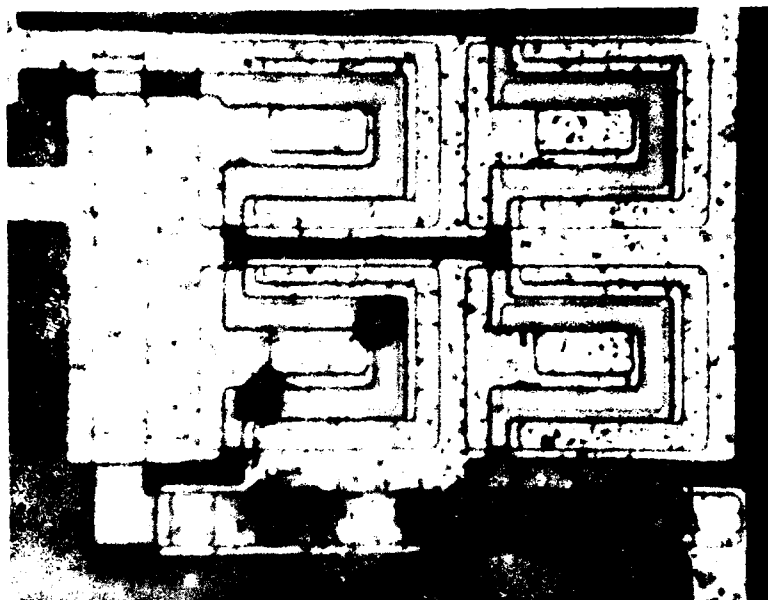


FIGURE 2.4-5 ROM INPUT NETWORK, POST FAILURE

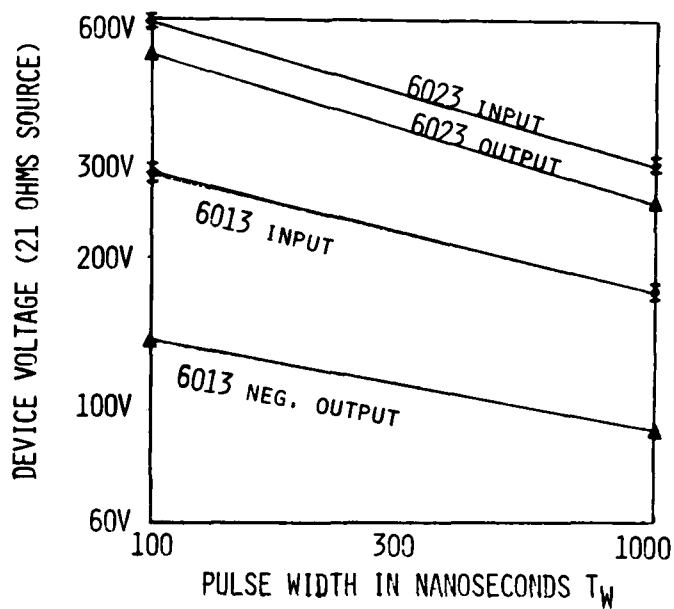


FIGURE 2.4-6 INPUT-OUTPUT PROTECT VOLTAGES

Many measurements on identical geometries gave consistent failure thresholds with about a 20-percent spread.

The resistor energy density for failure will be constant for very short pulses where negligible thermal conduction can occur. This adiabatic region occurs with pulses shorter than about 90 ns. For longer pulses, a quasi-adiabatic region occurs with failure energy increasing with the square root of pulsewidth, see break in figure 2.4-7. At very long pulse widths, constant power equilibrium will occur with energy increasing with the first power of pulsewidth. The instantaneous integral of applied voltage and current was measured and the energy failure threshold for single pulses between 40-ns to 1-us are shown for the two designs in figure 2.4-7.

#### 2.4.6 Capacitive Discharge Tests

A test circuit was made with a capacitor charged to a high potential, then switched to an input through 1500-ohm. The 100 pF with 1000 V or 50 uJ, voltage zap test was performed with no degradation on the improved input. The capacity was increased to 140 pF with 1000-V peak applied to the 1500-ohm source. Here the input resistor just started to degrade, rising about 1 percent in resistance with each zap. The failure level for capacitive discharges is broad, since large increases in the input resistor can occur before a failure in device access time results. Charging 140 pF to 2000 V did not fail the input network or degrade gate or diode reverse leakage currents. The heated input resistor dropped in resistance far below power match to the 1500-ohm source, and most of the increasing input voltage and energy is absorbed in the external source. Several 2000-V pulses increased the input resistor 25 percent. No arcs developed between the close 11-um spacing of the input pad and  $V_{DD}$  bus with a 0.8-um silox passivation overcoat. Tests on non-silox circuits developed destructive arcs at 270 V or  $2.5 \times 10^7$  V/m.

#### 2.4.7 Power Supply Clamping

Multiple parallel breakdown diodes clamp the supply lines from excessive transients when the power supply is not a low impedance. All tests described had nominal power on all supply lines with sufficient local energy storage to limit supply variations to less than 1 V during the transient pulse. Tests were also run to simulate static handling with all supply pins floating, except for the grounded  $V_{SS}$  connection. The excursions of the floating  $V_{DD}$  line were clamped well enough that no destructive breakdown occurred in the internal circuitry and the  $V_{DD}$  line rose to 25 V through the 20-ohm dynamic breakdown impedance when the input pulse was 580 V at 100 ns, the threshold of burnout of the input limiting resistor.

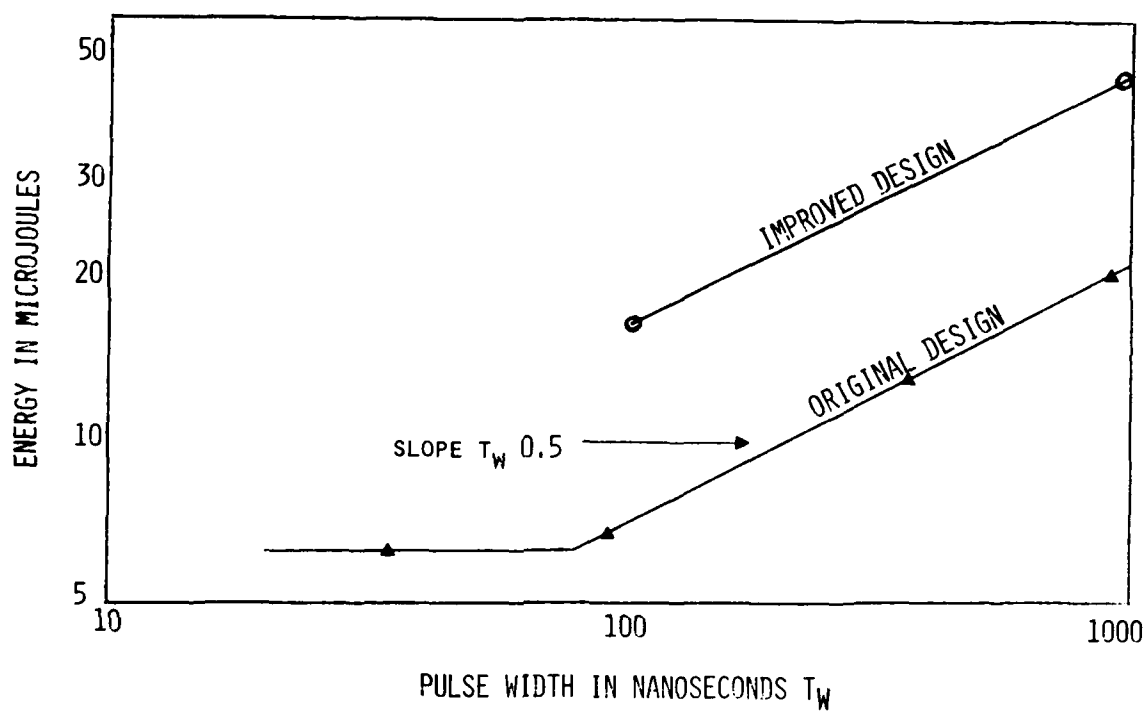


FIGURE 2.4-7 CMOS/SOS INPUT-PROTECT ENERGY



FIGURE 2.4-8 OUTPUT-PROTECT LAYOUT, POST FAILURE

## 2.4.8 Metallization Burnout

The metallization widths are sized to carry the input surge currents and survive high ionization pulse currents without failure. The aluminum is a nominal 1.0  $\mu\text{m}$  thick, with 0.9  $\mu\text{m}$  as a minimum. The silox island step edges are graded to avoid step thinning. A special test structure has been designed with passivated 1.0- $\mu\text{m}$ -thick aluminum conductors in 5-, 6-, and 8- $\mu\text{m}$  widths serpentine over 100 steps of 0.8- $\mu\text{m}$  silox plus 0.5- $\mu\text{m}$  silicon on a 330- $\mu\text{m}$ -thick sapphire substrate. Rectangular pulse tests were made with 100-ns and 1- $\mu\text{s}$  widths. The three linewidths failed at about the same current density  $J$ . Metallization burnout has been related to current density by  $J = kt^{-1/2}$ . With  $k = 2 \times 10^4 \text{ A} \cdot \text{cm}^{-2} \cdot \text{s}^{1/2}$  an 8- $\mu\text{m}$  minimum linewidth will handle up to 1.4 A or a current density of  $200 \times 10^5 \text{ A} \cdot \text{cm}^{-2}$  for a 1- $\mu\text{s}$  pulse. The steady-state current density is kept less than  $2 \times 10^5 \text{ A} \cdot \text{cm}^{-2}$ .

## 2.4.9 Output Protection

The historic approach to output protection is to do nothing. Since output devices have p-n junctions that break down at reasonable voltages and conduct static currents, there has been little historic problem from higher impedance static discharges, compared to the input-gate protection. Adding series-current limiting from the output driver to the package pin detracts from the fast rise-time characteristics when driving capacitive bus structures, so series resistance would usually be minimized.

A computer subsystem might have outputs and inputs interconnected on a bus with a low characteristic impedance for short pulsewidths. Our tests have shown failure of the output drain junctions with only 90-V pulses, 1  $\mu\text{s}$  wide. Thus the output FET's are more susceptible to failure than the inputs described above. A balanced design requires some output protection.

The clamping action of the drain-body diodes in the output buffer transistors is poor, since the short-channel regions have considerable lateral bulk resistance. Improved protection is obtained by adding low-bulk resistance reverse-biased clamp diodes shunting the output surge currents to  $V_{DD}$  or  $V_{SS}$ . The capacitive loading of these diodes is quite negligible, and they are sized so that the more easily controlled series output resistor  $R_L$  is the weakest element.

Since the output drain junctions can reverse breakdown (worst case) or forward bias to the power lines, a double-L attenuator design is achieved by placing a limiting resistor  $R_L$  from the output to diode clamps returned to the  $V_{SS}$  and  $V_{DD}$  supplies. Since the output bus has much higher capacitance than the input gate, the resistance must be lower. Then a second resistor

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$R_2$  of much lower power dissipation, connects to the output drains. The failure voltage of  $R_1$  is directly proportional to length, so the resistor must be large. A lower resistivity  $n^+$  diffusion (33-ohm/square) was used to thin the width and give a longer aspect ratio for the output resistor, which is 252  $\mu\text{m}$  long, 70  $\mu\text{m}$  wide. The output layout is shown in figure 2.4-8.  $R_1$  is 120-ohm,  $R_2$  is 100-ohm, and each diode that clamps to the supplies is formed with two parallel diodes of the same design as the input. Failure occurs in  $R_1$  with a 100-ns 580-V pulse applied to the output, a 220-V peak appears across the two clamp diodes, and the FET drain junctions survive and still can be switched into high impedance with leakages less than 100 nA. The most significant penalty for this output protection into a 50-pF output bus is 10 ns of added delay.

## SECTION 3

## MEMORY SUBSYSTEM (MNOS/SOS) PARTS

On this program four MNOS memory parts were designed and fabricated. All were directed at nonvolatile memory applications. All were designed using p-channel and n-channel transistors. Memory is obtained by the MNOS (Metal Nitride Oxide Semiconductor) transistor structure. All were fabricated using MNOS/SOS technology (using silicon film on sapphire wafers). The circuitry, structure and technology were chosen as the most suitable for low-power, non-volatile memory and radiation hardness as required for the intended missile guidance computer application.

The first part was designed on a previous program for the same technical purpose, an MNOS/SOS nonvolatile memory test vehicle. It was modified and served well to achieve the goals of this program. The Westinghouse mask set number is 6003. Processing of early lots was complete with test results in June 1975. Fabrication with process variations continued.

The second part to be designed was a fast-write TSM test vehicle. The Westinghouse mask set number is 6006. It included a 32-by-4 memory array with partial decoders sufficient to address four rows and two columns. Also included are row and column address input buffers, a row line driver, data input and output buffers and the column detect latch. The design and layout were complete by the end of June 1975. Fabrication of several lots resulted in obtaining fast write performance with write pulse widths down to 1.0  $\mu$ s in October 1975.

A parallel effort on the fast-write TSM was a breadboard designed to simulate the TSM test vehicle operation. It used MNOS/SOS memory test transistors from the 6003 PSM test vehicle for the two-transistor memory cell. Other MOS transistors, bipolar transistors and integrated circuits provided the timing, drive and sensing. The completed breadboard showed a 2 volt memory window for differential detection after a 1.0  $\mu$ s write pulse width.

Test results from these PSM and TSM test vehicles and from the TSM breadboard provided the base for definition and recommendation at Part Design Review I Meeting, (PDRI), 20-21 October 1975, of the LSIC memory parts to be designed.

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The third and fourth MNOS parts to be designed were the LSIC memory devices. These parts are the 256-word by 4-bit wide Permanent Store Memory (PSM), mask set number 6013 and the 512-word by 1-bit Temporary Store Memory, mask set number 6012. Design was begun on these after the Concept Review Meeting, 26 February 1976. Designs, simulations and layout were well underway by the Part Design Review II Meeting (PDRII), 3 June 1976. Design had progressed sufficiently by PDRII for the presentation to include characteristics, features, block and timing diagrams, circuits and simulations, approximate transistor counts, and estimated die sizes.

Layout on the PSM was complete by late September 1976. Processing, diagnostic testing and some mask iteration/correction was complete by December 1976. A good quantity of PSM parts was processed and screened in the February to May 1976 period. Reasonable wafer test and package test yields were obtained for this 237-by-260 mil die.

After PDRII, some additional simulations were run on the TSM detection circuitry. Several circuit problems were discovered which required increases in the sizes of most cells. By 3 August 1976, the conclusion was reached that the die size for this 256-word by 2-bit organization would be too large for mask-making and reasonable yield. Request was made for approval to change the organization of the TSM. After several meetings and much additional study, simulation and trial layouts, approval was granted on 8 September to design the TSM as a 512-word by one-bit memory. Layout of this version was completed in late November. Processing, diagnostic testing, some mask iteration/correction and final processing was complete by May 1977.

In September, 1977, the program resumed with emphasis on design modifications to improve the performance of the two, nonvolatile memory parts, PSM and TSM, and on process refinement to increase reproducibility and yield.

Process evaluation had indicated directions for improvement. A series of process experiments led to some modifications in the MNOS/SOS process. These were initiated early in 1978, resulting in improved yield and performance for the PSM and TSM.

Modification of design to improve the performance of the PSM was completed in December 1977. Many lots of PSM were fabricated, tested and screened by January 1979. Results were good yield, excellent stability and increased hardness.

Modification of the TSM for improved detection, reduced power and better internal timing was completed in February 1978. Fabrication of lots with the modified mask set was supported, beginning in April, by another contract. Good test results were achieved in December 1978 and January 1979.

In the subsections which follow, details of analysis, simulations, design, layout, process and test will be given or reference will be made to previous reports, included as appendices.

## 3.1 THE PERMANENT STORE MEMORY PSM, EAROM

In order to achieve the program goals an innovative approach was taken in the design of the PSM. The goals to be achieved were:

- 1 Kilobit nonvolatile memory storage capability
- Clear/write cycle time of 200  $\mu$ s
- Read cycle time of 1  $\mu$ s.
- Access time of 370ns after total dose exposure of "3"
- 3 year retention after  $10^4$  reversals
- Endurance of  $10^8$  reversals
- Low power >500 mW

### 3.1.1 Technology and Design Approach

The approach to Decode/Driver Devices and Circuits consisted of:

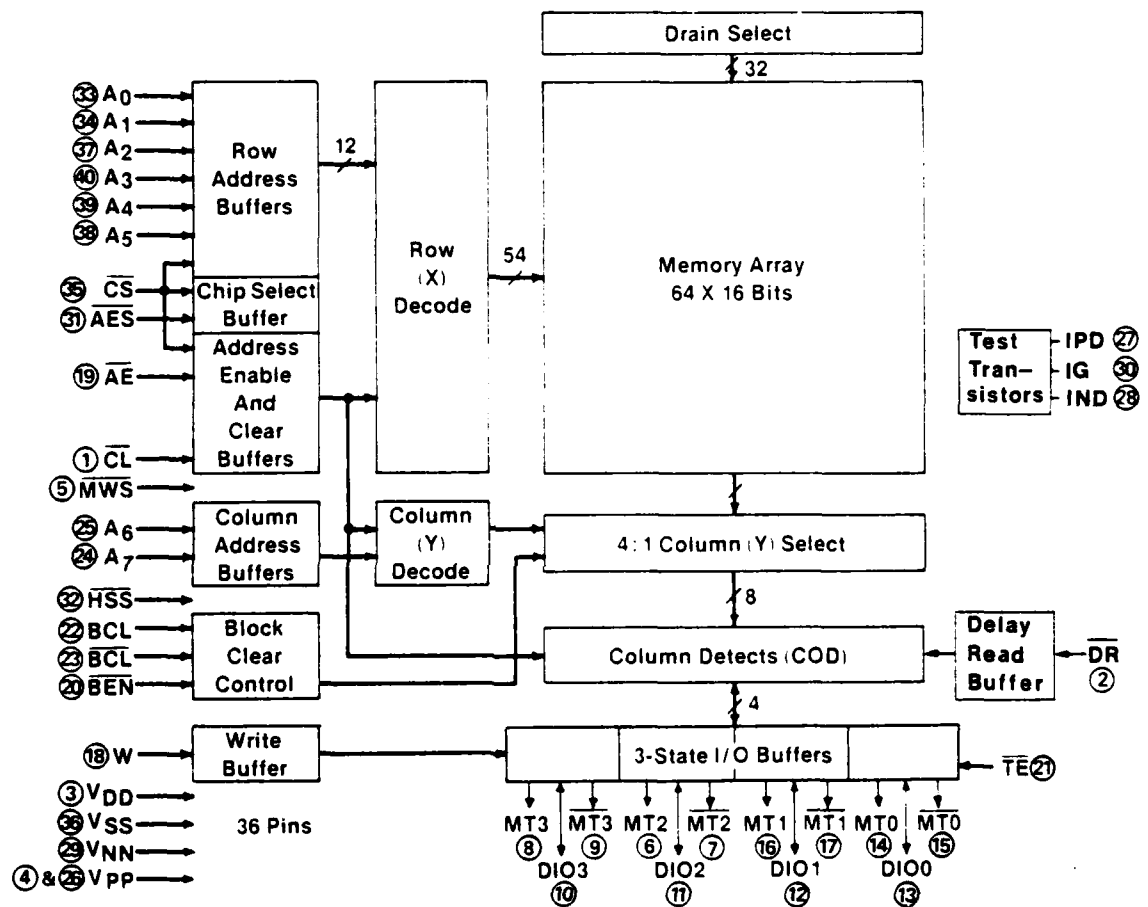
- N Channel depletion mode SOS device
- Constant current load elements
- Complementary push-pull drivers
- Low power decode tree
- Photo current compensation
- Radiation hard negative bias regime
- Minimum device/contact count
- CMOS compatible input/output

Features of the PSM include:

- N-depletion and P-enhancement mode devices
- Three stage buffers - lower input capacitance, improved speed
- Positive drive on N-depletion mode devices - size/speed improvements
- Improved decode circuitry to eliminate pattern sensitivity
- 2 FET storage cell
- Y-selection prior to COD - lowers power dissipation
- Test feature to determine  $\Delta V_T$  of each storage cell
- Non inverting tri-state I/O ports
- Alternating positive and negative write security block clear
- Single layer metal

In addition, the technology baseline chosen was a combination of p-enhancement and n-depletion mode transistors (PEMT and NDMT), fabricated in MNOS/SOS.

The first step in the engineering process of the PSM was to generate a block diagram which would accomplish all the functions necessary to meet the program goals for the PSM (figure 3.1). Additional functions such as on-chip decoding, CMOS compatible inputs, timing circuits, and 3-state I/O buffers were included for ease of system use.



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FIGURE 3.1 6013 PERMANENT STORE MEMORY BLOCK DIAGRAM

This technology and design approach represents state-of-the-art processing and circuit design capable of meeting or exceeding the high performance goals of the ACT program for the PSM.

### 3.1.2 Layout Design Rules

Once a technology choice was made, a suitable set of mask design rules was generated. The approach taken was to use conservative design rules to maximize photomasking yields and electrical performance. The one drawback of this approach was that the size of the LSI die would grow, but initial yield was considered most important in this parts development program.

The salient design rules for the PSM are summarized below:

#### MEMORY DESIGN RULES

- Gate and contact window for the gate must stay  $5\text{ }\mu\text{m}$  inside the silicon island where the metal gate electrode enters the transistor.
- Single-level metal with diffused cross-unders in the SOS film.
- Bonding pads will be  $5\times 8$  mils to permit rebonding in hybrid package assembly.
- Bonding pad to scribe lane spacing is 3 mils.
- Power busses external to the bonding pads will be permitted to facilitate the design of input protect networks. The minimum spacing of a bus to scribe lane is 3 mils.
- Scribe lanes are  $\geq 10$  mils wide to permit either laser scribing or diamond saw separation.
- Number each chip on the wafer.

To insure high reliability of the part, detailed design of the interconnect system was performed. The design criteria for interconnection current density is a maximum current density of  $10^5\text{ amp/cm}^2$ , calculated at the minimum aluminum thickness allowed. In a single metal aluminum interconnection system the deposition thickness is  $10\text{K}\text{\AA}$ , however a minimum thickness of  $5\text{K}\text{\AA}$  over steps is allowed. The current density is calculated at the minimum thickness of  $5\text{K}\text{\AA}$ . The line width design equation is  $W = (2 \times 10^{-3}) I_M \mu\text{m}$  (microns), where  $I_M$  is the maximum current carried by the metal line. For example, if the line carries a maximum of 5 ma, then a  $10\text{-}\mu\text{m}$  wide line is required to meet the current density design criteria. A  $40\text{-}\mu\text{m}$  wide line can carry 20 ma with no reliability problems. SEM inspection techniques are used to guarantee the minimum aluminum thickness.

TABLE 3.1 LAYOUT/DESIGN RULES  
DIMENSIONS AFTER PROCESSING (IN MICRONS)

	<u>CMOS</u>	<u>TSM</u>	<u>PSM</u>
Minimum N <sup>+</sup> -P <sup>+</sup> Space Along Silicon Edge	12	12	12
Gate Width 10V	4	5	
20V	-	9 (HVNEMT)	7 (PEMT)
30V	-	11 (HVNEMT)	9 (PEMT)
Boron Overlap of HVNEMT 20V		4	
30V		5	
Gate Metal Overlap of Gate Protect	1	1	1
Metal: Gate Width	6	7	8
Min. Interconnect Width	8	8	8
Min. Metal-Metal Space	8	8	8
Minimum Contact Window	6x6	6x6	6x6
Maximum Body Contact Spacing N-channel	40	40	40
P-channel	100	100	100

These design rules lend themselves to final masks which will have ease of alignment to ensure high photoengraving yields. The basic alignment tolerance designed into the masks is  $\pm 2$  microns with the one exception being the metal alignment to the gate of  $\pm 1$  micron. These alignment tolerances are readily achieved with present-day photolithography equipment. In addition layouts are drawn as they appear after processing. The software capability of the Calma automated graphic system accounts for any sizing which may be necessary during the mask-making sequence to compensate for image size changes which occur during processing.

Therefore, using conservative design rules and level to level alignment tolerances, high performance, advanced LSI circuits can be processed with a high degree of manufacturability.

### 3.1.3 Test Pattern and Test Vehicle Design

Initial evaluation of a new technology approach, circuit design, and mask design rules is normally performed on a test vehicle prior to design and fabrication of the final LSI circuit. The objectives of the ACT test vehicles are these:

- Provide structures to actively monitor processes and process variations.
- Provide devices that allow correlation of process parameters with both memory and nonmemory transistor characteristics.
- Provide discrete devices to evaluate effects of process parameters (improvements) upon thermal stability and radiation hardness.

In addition to these objectives, some test vehicles contain actual circuit elements which are to be used on the final LSI circuit. These circuits are usually configured to simulate actual operation of the final LSI circuit so that performance predictions may be made. This type of test vehicle is usually defined as an "advanced test vehicle".

#### 3.1.3.1 6013T Test Pattern

In order to meet the process and electrical evaluation objectives of the ACT program, the 6013 basic test pattern was designed, fabricated and tested. This test pattern with its interconnect pattern shown in figure 3.2 contains process evaluation test structures as well as individual FETs to evaluate electrical device parameters. Since the 6023T is a modification of the 6013T and contains 6013T structures as well as some additional ones, details of the test pattern structures will be given in the 6023T description.

#### 3.1.3.2 6023T Test Pattern

The 6023T test pattern interconnect is shown in figure 3.3. Note that a regular pad arrangement was incorporated in this structure. This was done to facilitate hand or automated testing of the various sections. The 6023T contains both process and electrical evaluation structures.

3.1.3.2.1 Process Evaluation Structures: These structures are used for both in-line test and final evaluation after processing is complete. The structures include:

TABLE 3.3 SCMOSFET PARAMETERS

STRING INPUT ORDER	KEYWORD	DESCRIPTION	DEFAULT VALUE	MEASUREMENT UNIT
1	VTO	Zero-bias threshold voltage	0	Volts
2	PHI	Surface potential	0.5	Volts
3	UO	Zero-bias surface mobility	200	cm <sup>2</sup> /v-sec
4	NB	Substrate doping concentration	1.E+15	cm <sup>-3</sup>
5	RD*	Drain ohmic resistance multiplied by unit channel width	0	Ω-cm
6	RS*	Source ohmic resistance multiplied by unit channel width	0	Ω-cm
7	CO	Oxide capacitance	1.E-8	F/cm <sup>2</sup>
8	C1**	Gate-source overlap capacitance/unit channel width	0	F/cm
9	C2**	Gate-drain overlap capacitance/unit channel width	0	F/cm
10	CBD**	Bulk-drain zero-bias capacitance/unit channel width	0	F/cm
11	CBS**	Bulk-source zero bias capacitance/unit channel width	0	F/cm
12	PB	Bulk junction potential	1	Volts
13	IS	Bulk junction saturation current	1.E-14	Amps
14	KN	Normal field mobility coefficient	0	Volts <sup>-MN</sup>
15	MN	Normal field mobility exponent	0	---
16	KL	Lateral field mobility parameter	0	---
17	ECRIT	Velocity limiting lateral field	∞	Volts/cm
18	BETA	Transconductance	1.E-6	Amps/V <sup>2</sup>
19	GAMMA	Bulk threshold parameter	0	(V) <sup>1/2</sup>
20	LAMBDA	Channel length modulation parameter	0	cm/V <sup>1/2</sup>
	NI	Intrinsic carrier concentration	0	cm <sup>-3</sup>
	ALPHA	Impact ionization parameter	0	cm <sup>-1</sup>
	BETASX	Avalanche critical field	2.2E+06	V/cm
	TINS	Insulator thickness	1.E-05	cm

\* This parameter is divided internally by the device width.

\*\* This parameter is multiplied internally by the device width.

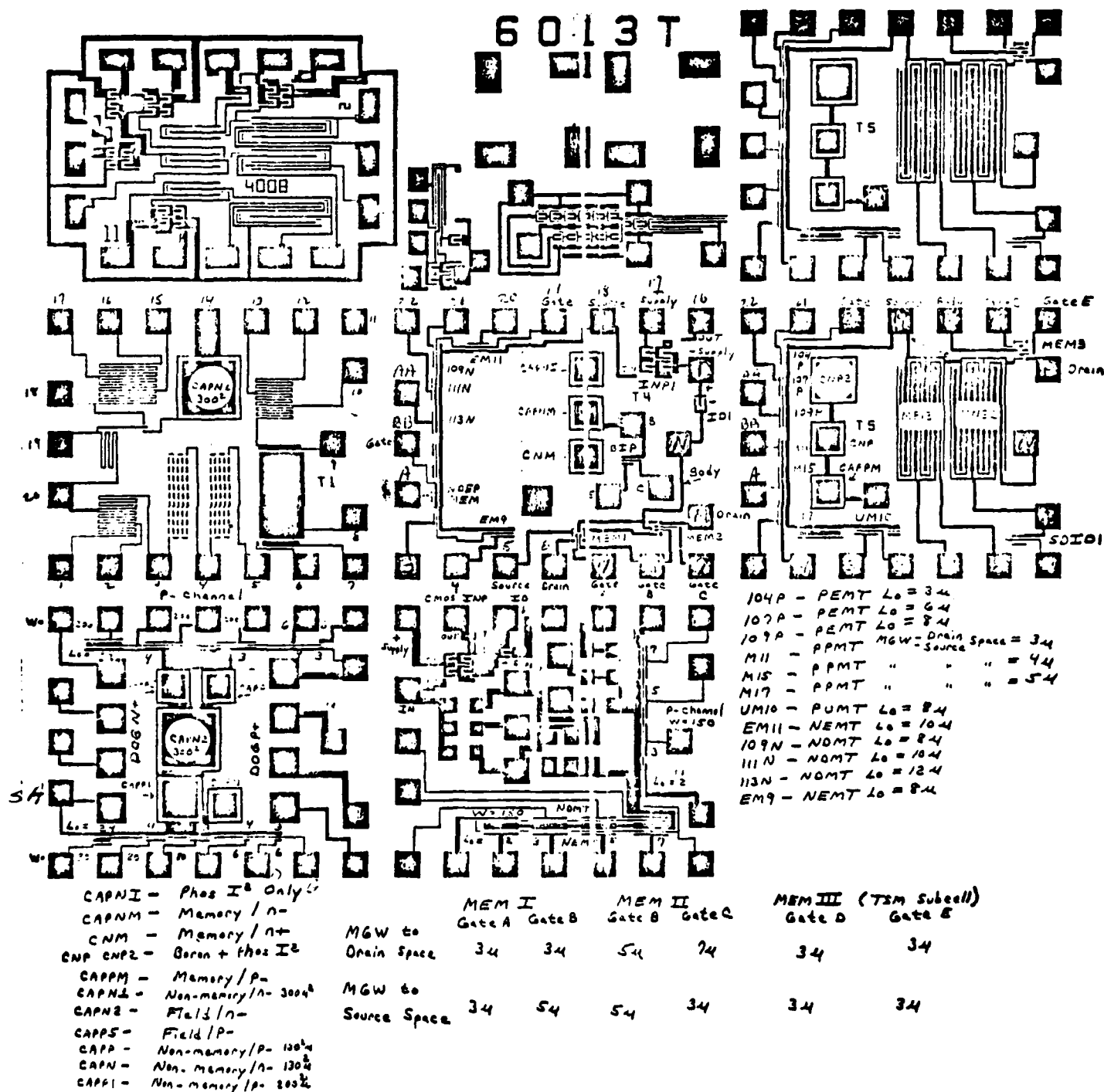


FIGURE 3.2 TEST PATTERN 6013T

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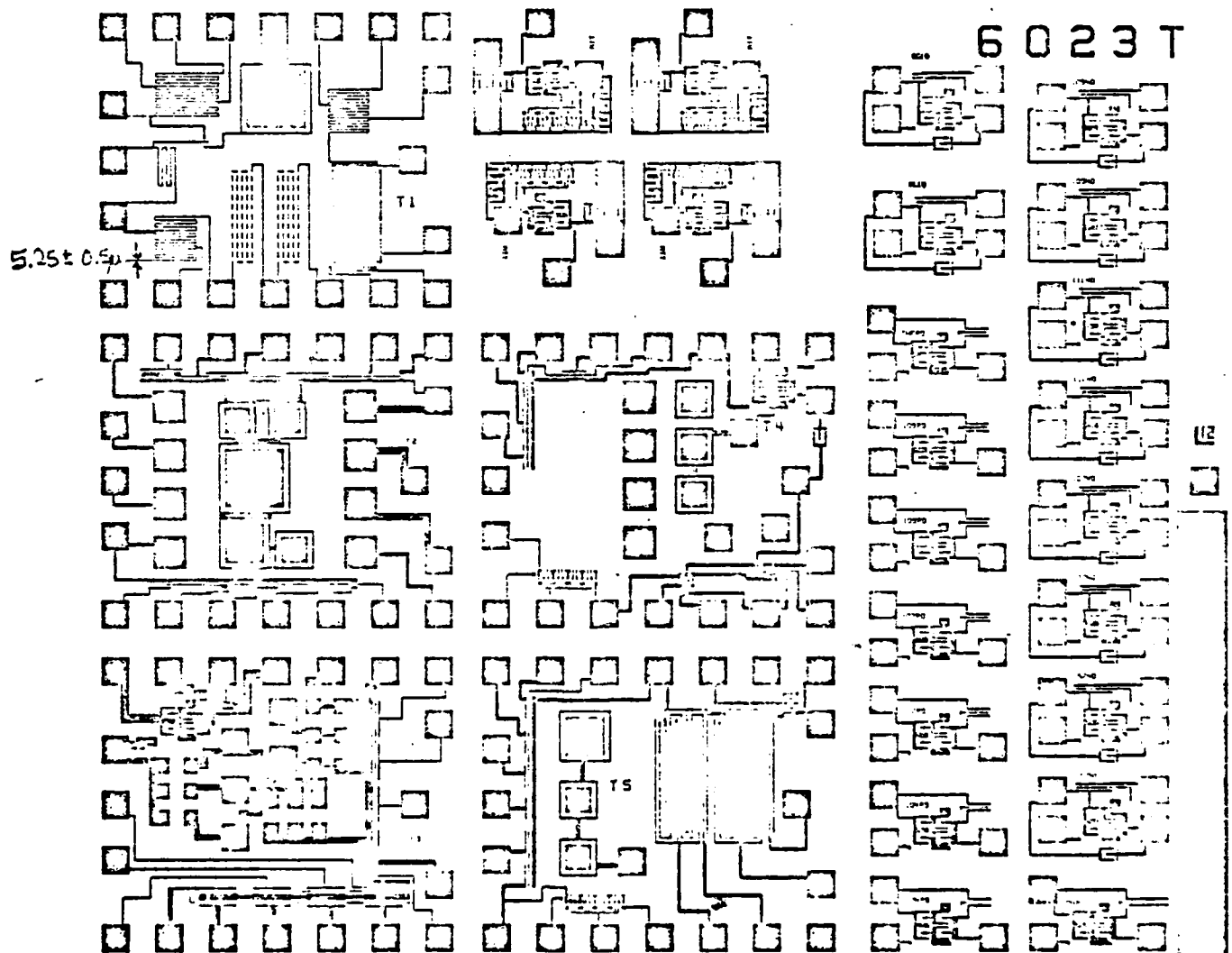


FIGURE 3.3 TEST PATTERN 6023T

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- CV Capacitors: Nonmemory; P-Implant, N-Implant,  
P-/N-Implant, N Substrate  
Memory; P-Implant, N Substrate  
N+ diffusion,  
Thick Field; P-Implant
- Dogbones: N+, P+, P- Implant
- Resistance Measurements: Long N+ Si Island  
N+, P+ Resistor strings with 100  
min. size contacts.  
N+, P+ Pulse Test Resistors
- Metal Step Coverage: Island Edge  
Gate Window Edge  
CW over Silicon Island  
Island - Field - Gate FETS
- Resolution Patterns

3.1.3.2.2 Electrical Evaluation Structures: These structures, which in general are individual FETs of various types, are used to monitor the electrical parameters of the devices. The effects of process variations on these parameters can, therefore, be monitored. The feedback from these types of tests can be used to stabilize the process at a point which will yield devices capable of optimal electrical performance. Using these individual devices such characteristics as radiation hardness and temperature bias stability can be determined. The devices included on the 6023T include:

- Structures w/o Input Protect Network
  - N enhancement mode FET - L = 3, 4, 5, 6, 8, 10, 25  $\mu\text{m}$
  - P enhancement mode FET - L = 3, 4, 6, 8  $\mu\text{m}$
  - N depletion mode FET - L = 3, 4, 6, 8, 10, 12  $\mu\text{m}$
  - P depletion mode FET - L = 4, 5, 25  $\mu\text{m}$
  - P memory FET, Drain-Source Protected (DSP)
  - P memory array subcell (DSP)
  - N memory FET (DSP)
  - P memory FET (non DSP)
- Structures with Input Protect Network
  - P enhancement mode FET - L = 4, 7, 9  $\mu\text{m}$
  - N depletion mode FET - L = 7, 9, 11  $\mu\text{m}$
  - P memory array subcell (DSP)
- Individual input protect network
- Input protect single diode structure

### 3.1.3.3 6003 Advanced Vehicle

A 64 x 4 MNOS/SOS memory test vehicle, shown in figure 3.4 and designated 6003, has been designed to predict operation of a 1-kilobit array to be used for long term program storage in a radiation environment. ISPICE, an interactive computer-aided design program, was used to verify operation of all peripheral circuitry as well as predict operation of the array itself.

A complete description of the circuits contained in the 6003 and the design and simulation of these circuits is contained in CDRL Item 1001. Analysis and Simulation Report for MNOS/SOS Test Vehicles dated 19 November 1975.

3.1.3.3.1 Design Summary: Basic as well as advanced test vehicles were designed for process and electrical evaluation of the technology choice for the ACT PSM. Using these test vehicles, process optimization in the areas of yield and electrical performance can be realized. Once optimized, these test vehicles are then used to monitor process stability. The 6003 was designed in such a manner as to yield an accurate prediction of electrical and functional performance of the final PSM LSIC.

### 3.1.4 Test Results for Test Patterns and Test Vehicle

Following fabrication of the memory test vehicle lots, each was evaluated by measuring electrical and process parameters. The results of these tests were fed back so that process improvements could be incorporated in later lots to yield an optimum device and interconnect structure. Individual devices from 6013T/6023T lots were subjected to total dose and temperature bias stress tests. Individual memory FETS were subjected to endurance/retention tests.

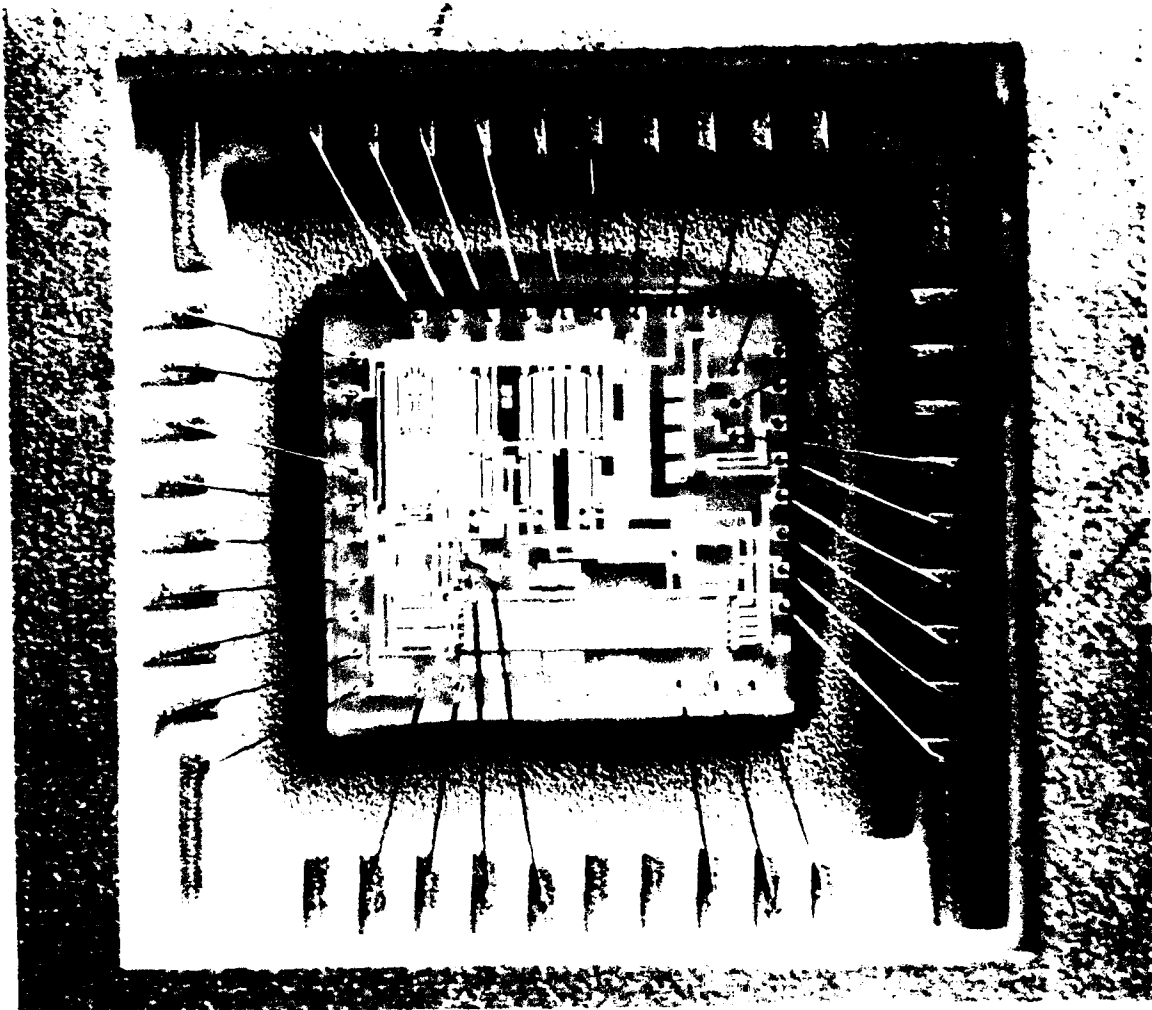
#### 3.1.4.1 6013T and 6023T Test Results

Test results of 6013T and 6023T devices relating to process improvement and refinement is covered in a separate section of this report.

In addition, radiation test of 6013/6023T devices will be covered in the Radiation Tests Section and temperature bias testing will be covered in the Environmental/Reliability Section.

Memory device endurance/retention tests will be covered in the Endurance/Retention Tests Section.

The above mentioned sections will cover results of Test Vehicles as well as the PSM LSIC as, in general, test vehicles were processed on the same wafers as the LSIC.



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FIGURE 3.4 PSM TEST VEHICLE 6003 PACKAGE

## 3.1.4.2 6003 Test Results

The 6003 Permanent Store Memory (PSM) Test Vehicle has been designed and fabricated. This report conveys test procedures and results to date on the PSM test vehicle in the areas of both electrical and radiation hardness characterization.

A complete description of the 6003 test results is contained in CDRL item 1002, Test Results Report MNOS/SOS 6003 Permanent Store Memory Test Vehicle dated October 1975.

Not included in that report are temperature bias stress results which will be included here. Figure 3.5 shows access time vs TBS for a period of 150 hours at 150 C. Variations in access time are less than 10% at any data point. Likewise, figure 3.6 shows read power vs TBS stress and indicates changes of less than 5%.

Both parametric and functional testing of the 6003 Permanent Store Memory Test Vehicle has verified low-power, high-speed operation with an overall chip access time of 250 nanoseconds. The sensitivity of the 6003 detection circuit is projected to provide proper detection of stored data for a period

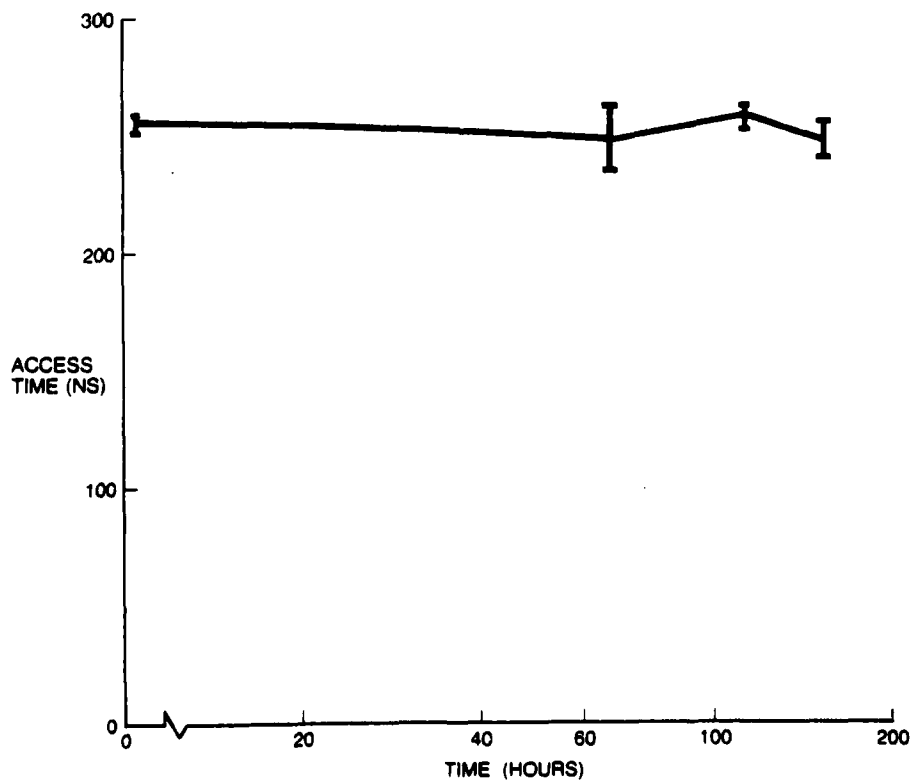


FIGURE 3.5 6003 PSM TEST VEHICLE, TBS @ 150°C, ACCESS TIME

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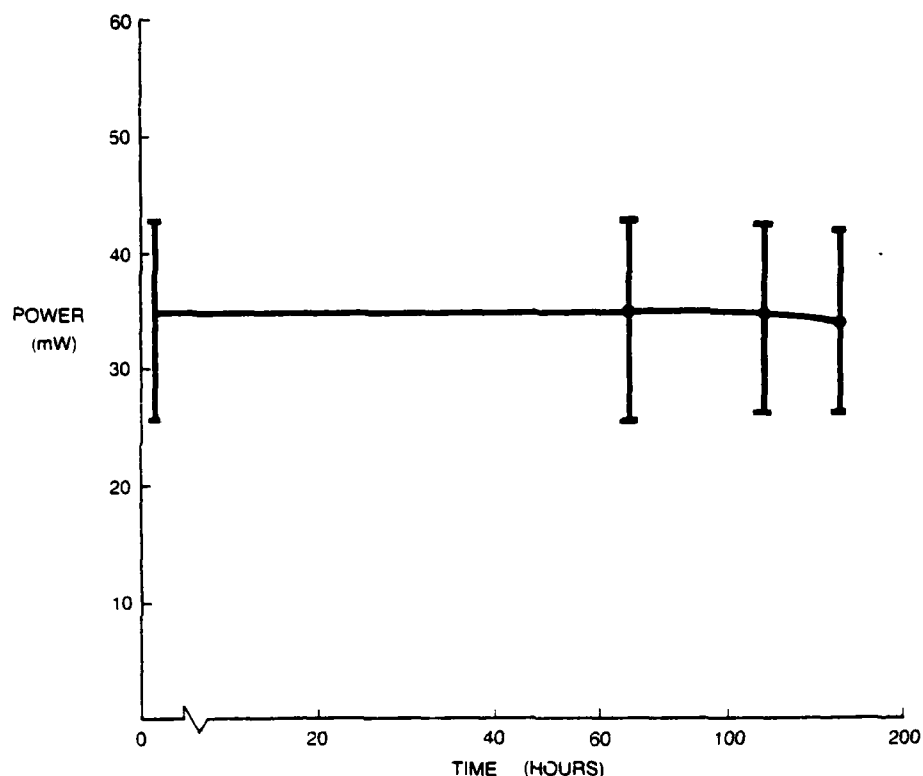


FIGURE 3.6 6003 PSM TEST VEHICLE, TBS @ 150°C, READ POWER

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of 10 years after  $10^{10}$  reversal cycles. The 6003 has been subjected to maximum specified total dose which resulted in only a 10% increase in access time, while maximum gamma dose rates have been applied without upset of any of the peripheral circuitry.

The test results of the 6003 PSM Test Vehicle indicate that all the performance goals of the LSI Permanent Store Memory can be met or surpassed.

### 3.1.4.3 Summary

Utilizing the 6013T, 6023T, and 6003 PSM test vehicles, the process has been verified and optimized, process stability has been demonstrated as well as radiation hardness and temperature bias stability. In addition, the circuit design approach has been proved to yield a high-speed, low-power part capable of meeting all the performance goals of the PSM LSIC.

### 3.1.5 PSM 6013 LSIC Design and Circuit Simulation

After optimizing the process, a large statistical sampling of both process and electrical parameters was made. These parameters were then fed into a MOSFET model which was used for circuit simulation. Once a high degree of confidence in the model was obtained, an automated circuit simulation package incorporating this model and known as ISPACE was then used to simulate functional operation of all circuits which were designed for the PSM LSIC.

### 3.1.5.1 General Description of ISPICE

ISPICE is a highly responsive analytical system that can be controlled and operated by users with little or no data-processing background. The ISPICE capability is implemented with an uncomplicated command language based on normal information requirements and terminology of the engineering discipline. The size of a circuit to be simulated is not limited by the program, and circuits containing over 1000 elements may be simulated in a single operation.

Three basic types of analysis are performed by the program. These are: ac small signal sinusoidal steady-state analysis, in which operating points are automatically calculated from dc analyses and transfer responses; nonlinear dc analysis which yields steady-state operating point, input, and output characteristics; and Nonlinear transient analysis used to determine time responses to arbitrary inputs. The last two types of analyses were used extensively in the design of the PSM LSIC.

I/O for the simulation program is accomplished through a high-speed, time-share terminal. Circuits are coded into circuit files which are stored on the user's disc for retrieval at the time the simulation is run. Output data of circuit voltages and currents may be output in tabular form or plotted in a format specified by the user.

Several circuit element models have been developed for and by National CSS and are available on ISPICE. A list of the elements are shown in table 3.2.

TABLE 3.2 ISPICE ELEMENTS

<u>COMPONENTS</u>	<u>DEVICES</u>
• RESISTORS	• DIODES (JUNCTION, SCHOTTKY, ZENER)
• CAPACITORS	• BIPOLAR JUNCTION TRANSISTORS (BJT)
• INDUCTORS	• BIPOLAR INTEGRATED TRANSISTORS (BIT)
• MUTUAL INDUCTORS	• JUNCTION FIELD-EFFECT TRANSISTORS (JFET)
• INDEPENDENT VOLTAGE SOURCES	• MOS FIELD-EFFECT TRANSISTORS (MOSFET)
• INDEPENDENT CURRENT SOURCES	• SHORT-CHANNEL MOS FIELD-EFFECT TRANSISTORS
• VOLTAGE-CONTROLLED CURRENT SOURCES	
• NONLINEAR VOLTAGE-CONTROLLED CURRENT SOURCES (WITH TRANSDUCTANCE DESCRIBED BY A POLYNOMIAL FUNCTION)	

**3.1.5.1.1 MOSFET Model:** Since the technology approach for the PSM LSIC was MNOS/SOS, the MOSFET models are of particular interest. Since channel length geometries as small as 4  $\mu\text{m}$  were used, the model should take into account short channel effects.

A short channel MOS model for both P and N type devices in which device parameters are based on processing and geometry in addition to empirical parameters is included in the ISPICE program. This MOSFET model includes representation of channel length modulation; variation of mobility with gate and drain voltage; voltage-dependent capacitors which model gate-to-bulk, gate-to-drain, and gate-to-source capacitances; effects of the substrate diodes; subthreshold current flow; substrate current flow; and "kink effect". This represents a "state-of-the-art" MOSFET model capable of accurate simulation of low power, short channel, MNOS/SOS devices. The program input format is shown in figure 3.7. A table of MOS parameters is pictured in table 3.3. These parameters may be tailored by the designer to represent both process and electrical characteristics of the technology being used in the design. A schematic of the model elements is shown in figure 3.8.

## MODEL SPECIFICATION

The device parameters of a Short Channel MOSFET are based on processing and geometry in addition to empirical parameters as they are in the MOSFET model. However, the SCMOSFET model differs from the MOSFET in its treatment of channel length modulation and variation of mobility with bias.

### Program Input Format

The general format for the SCMOSFET model is as follows:

```
Mxxxxxxx nd ng ns nb modelname w l OFF
MODEL modelname { NSCM } (parameter list)
                  { PSCM }
```

where:

nd	drain node
ng	gate node
ns	source node
nb	substrate node
w	width of gate in cm
l	length of gate in cm
NSCM	N-channel device
PSCM	P-channel device

FIGURE 3.7 ISPICE INPUT FORMAT

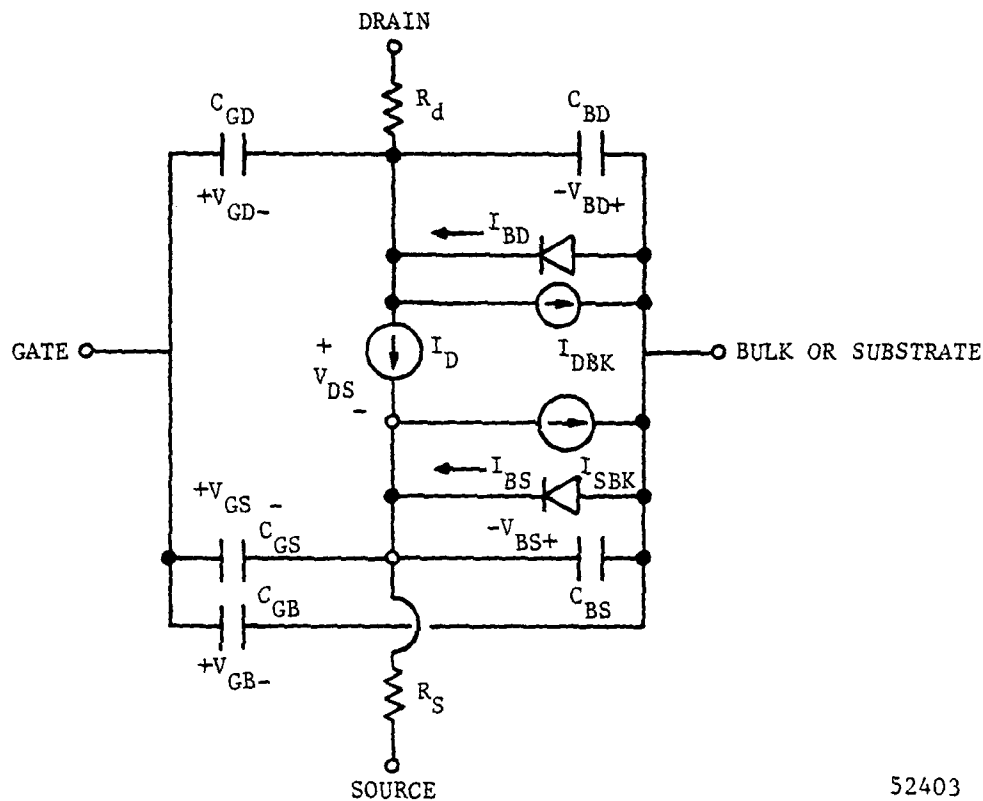


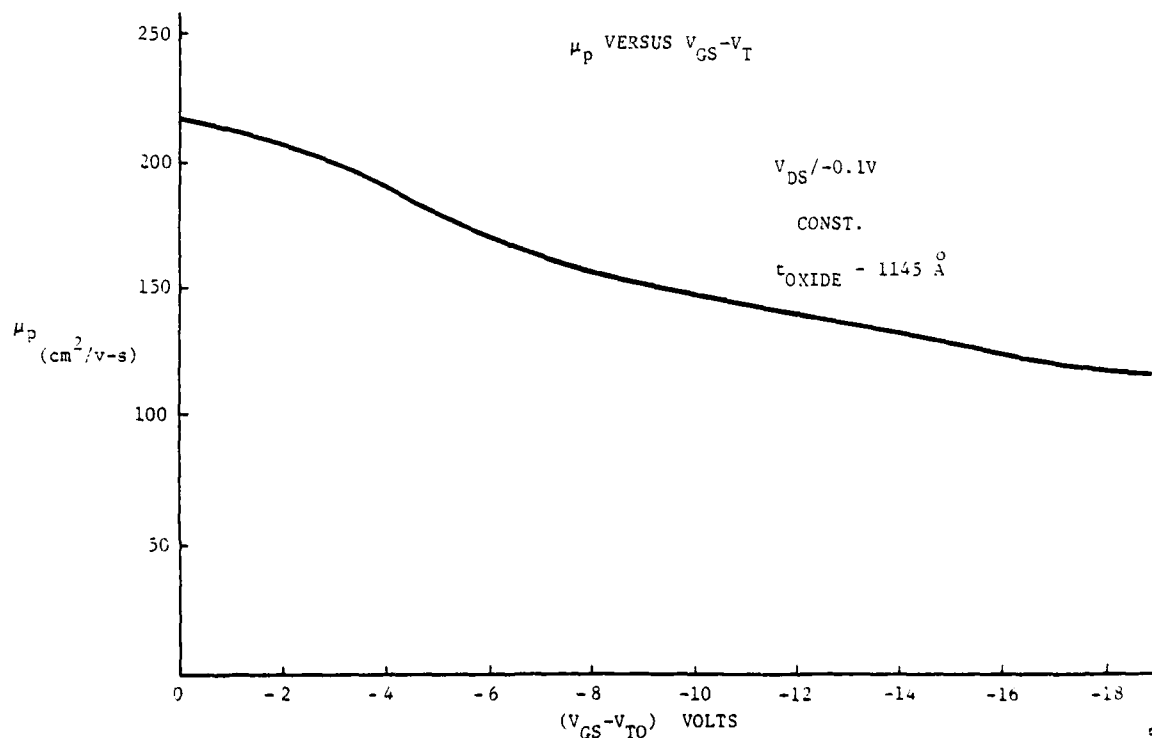
FIGURE 3.8 SCHEMATIC OF MODEL ELEMENTS

The actual parameters, which are based on a large statistical sample from test pattern measurements, are shown in table 3.4 for both the pre-rad 25°C case and the post-rad 125 C condition. Figure 3.9 shows a plot of p-channel surface mobility as a function of normal field. From this normal field dependent mobility, parameters are obtained which are necessary for an accurate model.

TABLE 3.4 ISPICE SCM MOSFET PARAMETERS FOR HV-PENT, HV-NDMT & PMT\*

String Input Order	Keyword	HV-PENT		HV-NDMT		Units
		Pre-Rad 25°C	Post-Rad 125°C	Pre-Rad 25°C	Post-Rad 125°C	
1	VTO	-2.0	-4.5	-3.0	-4.0	Volts
2	PHI	0.56	0.56	0.70	0.70	Volts
3	UO	160	75	300	195	CM <sup>2</sup> /V-Sec.
4	NB	1E15	1E15	1E16	1E16	CM <sup>-3</sup>
5	RD	0.069	0.069	0.046	0.046	OHM-CM
6	RS	.069	.069	0.046	0.046	OHM-CM
7	CO	3.14 E-8	3.14 E-8	3.14 E-8	3.14 E-8	F/CM <sup>2</sup>
*7 (Memory)	C0	10.8 E-8	10.8 E-8	--	--	F/CM <sup>2</sup>
8	C1	3.14 E-12	3.14 E-12	3.14 E-12	3.14 E-12	F/CM
9	C2	6.28 E-12	6.28 E-12	6.28 E-12	6.28 E-12	F/CM
10	CBD	6.1 E-13	6.1 E-13	6.1 E-13	6.1 E-13	F/CM
11	CBS	6.1 E-13	6.1 E-13	6.1 E-13	6.1 E-13	F/CM
12	PB	0.56	0.56	0.56	0.56	Volts
13	IS	1 E-14	1 E-14	1 E-14	1 E-14	Amps
14	KN	0.038	0.038	--	--	Volts
15	MN	1.07	1.07	--	--	Volts
16	BETA	2.51 E-6	1.18 E-6	4.71 E-6	3.06 E-6	A/V <sup>2</sup>
*16 (Memory)	BETA	8.64 E-6	4.05 E-6	--	--	V/V <sup>2</sup>
17	ECRIT	--	--	--	--	V/CM
18	GAMMA	0.58	0.58	1.83	1.83	V 1/2
*18 (Memory)	GAMMA	0.17	0.17	--	--	V 1/2
19	LAMBDA	33.8 E-6	33.8 E-6	33.8 E-6	33.8 E-6	CM/V 1/2

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FIGURE 3.9 MOBILITY VERSUS APPLIED FIELD

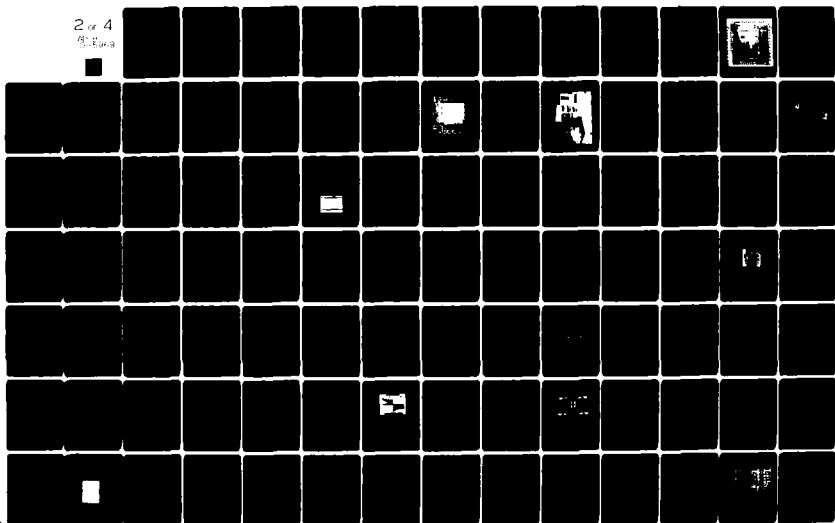
AD-A085 969 NORTHROP CORP PALOS VERDES PENINSULA CALIF ELECTRONICS DIV. F/G 9/2  
ADVANCED COMPUTER TECHNOLOGY-I (ACT I)  
01 MAY 80 F04704-75-C-0006 NL

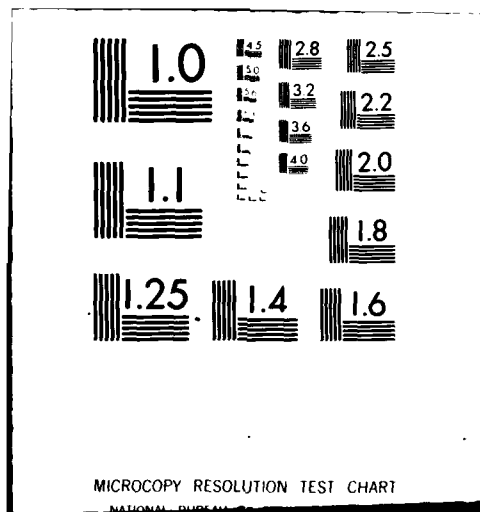
UNCLASSIFIED

NORT-80-11

2 of 4

5:14pm

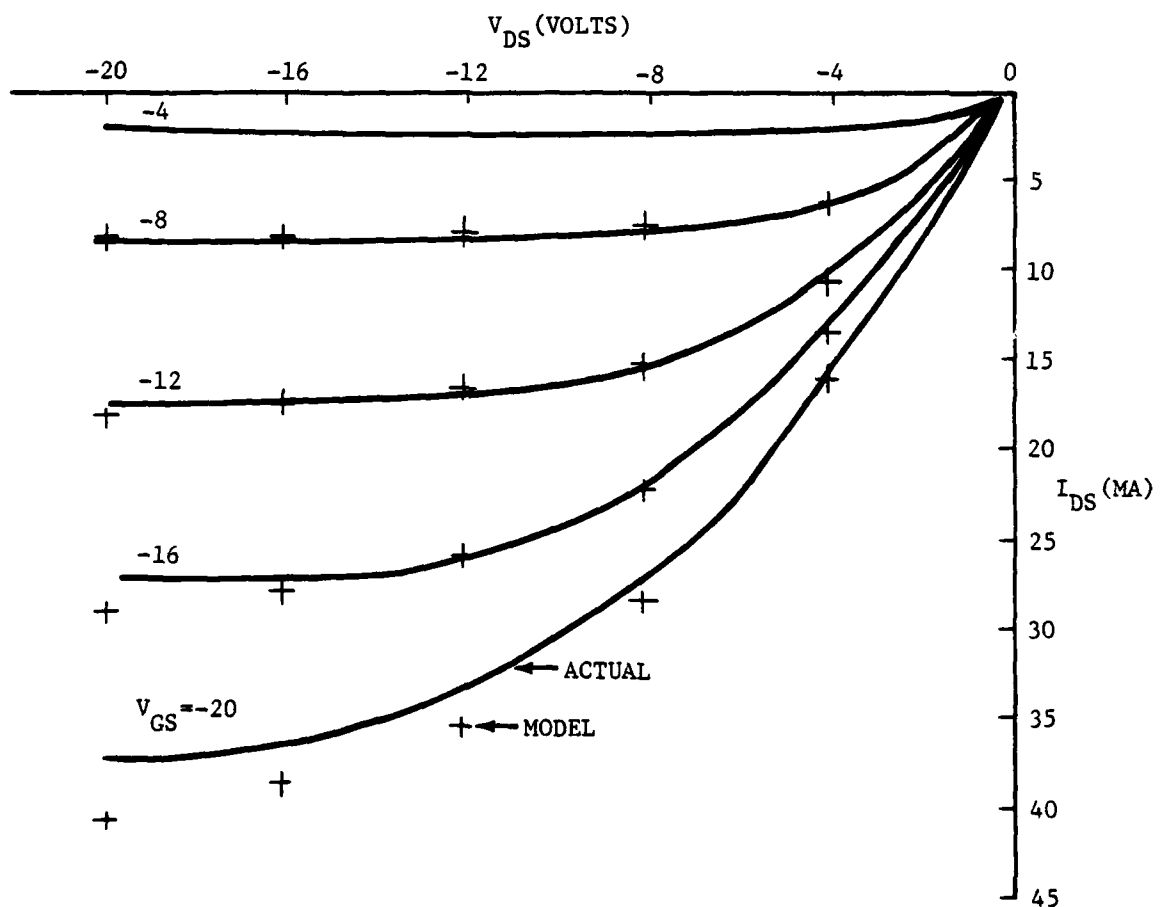




Once all the MOSFET parameters were obtained, individual models for p-enhancement mode and n-depletion mode FETS were created. A family of I-V curves were simulated and compared to the measured characteristics. Figure 3.10 shows the actual vs. simulated characteristics of an enhancement mode device.

Excellent agreement is obtained between the actual and ISPICE curves.

Once accurate models were obtained for the individual circuit elements, design and simulation of the actual circuits which comprise the PSM LSIC proceeded with a great deal of confidence.



## MODEL PARAMETERS

$V_{TO} = 1.2$	$BETA = 3.26 \times 10^{-6}$	
$\Phi = 0.56$	$KN = 0.038$	$LAMBDA = 33.8 \times 10^{-6}$
$CO = 3.02 \times 10^{-8}$	$MN = 1.07$	$GAMMA = 0.60$

FIGURE 3.10  $I_{DS}$  vs  $V_{DS}$  FOR MODEL AND MEASURED TRANSISTORS

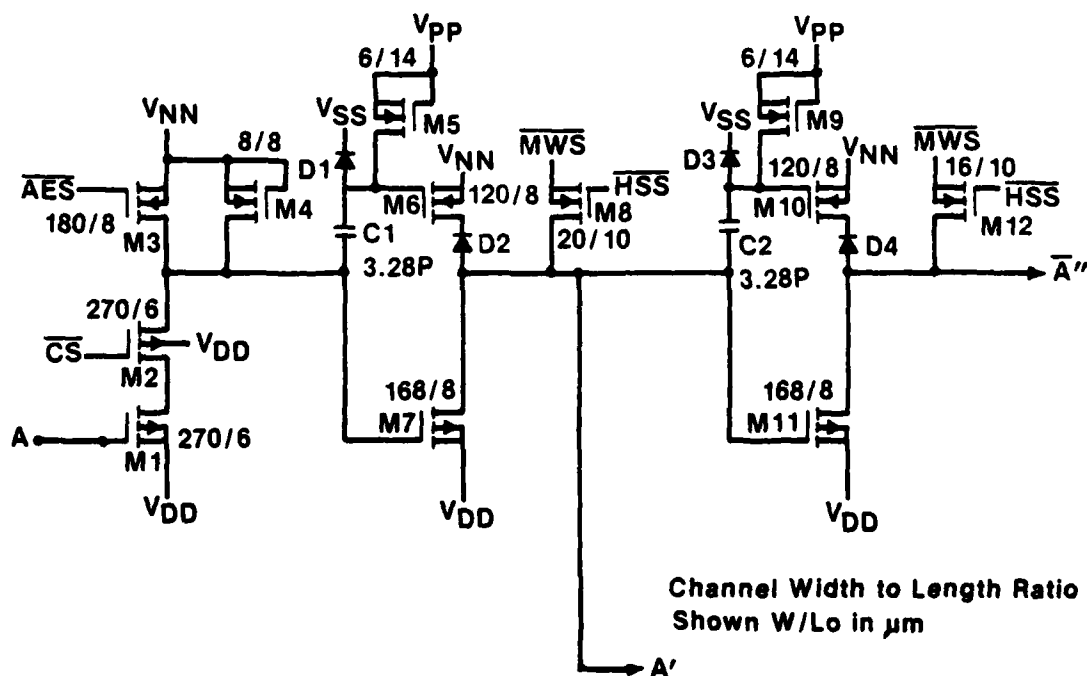
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## 3.1.5.2 Design and Simulation of LSI Circuit Blocks

Each block in the block diagram was simulated separately and in combination where necessary. In some cases the output of a previously simulated circuit was used as the input for circuit which it drove. After all circuits were simulated, an estimate of access time was made based on time constants and delays in successive portions of the memory circuitry.

Design and simulation of all circuits were worst case, that is post rad and 125°C for functional operation (this will yield slowest transitions and longest delays) and post rad at -55°C for power dissipation determination. This will yield maximum power dissipation .

**3.1.5.2.1 Address Buffer:** Figure 3.11 shows the address buffer design used to drive both the X(row) and Y(column) decoder. The buffer configuration is a three-stage design which maximizes internal switching speed while minimizing input capacitance. Each inverter stage is composed of one or more p-channel enhancement mode devices and an n-channel depletion mode device. These operate in a push-pull mode due to either clocking or an integrated level shift network. N-channel depletion mode load elements are used to supply an additional 10 volt drive during write mode operation. The buffer is chip select (CS) addressable, so that unselected arrays may be deselected and will draw only a small leakage current from the supply resulting in very low standby power.



52407

FIGURE 3.11 PSM: ADDRESS BUFFER

Figure 3.12 is the ISPIICE transient simulation of the address buffer operation. Maximum delay to output address is 80 ns.

3.1.5.2.2 Address Enable Buffer: Once the internal address signals are valid at the decoder input, the address enable buffer shown in Figure 3.13 is used to enable the X and Y decoders.

The address enable buffer is of the same basic three stage design as the address buffer.

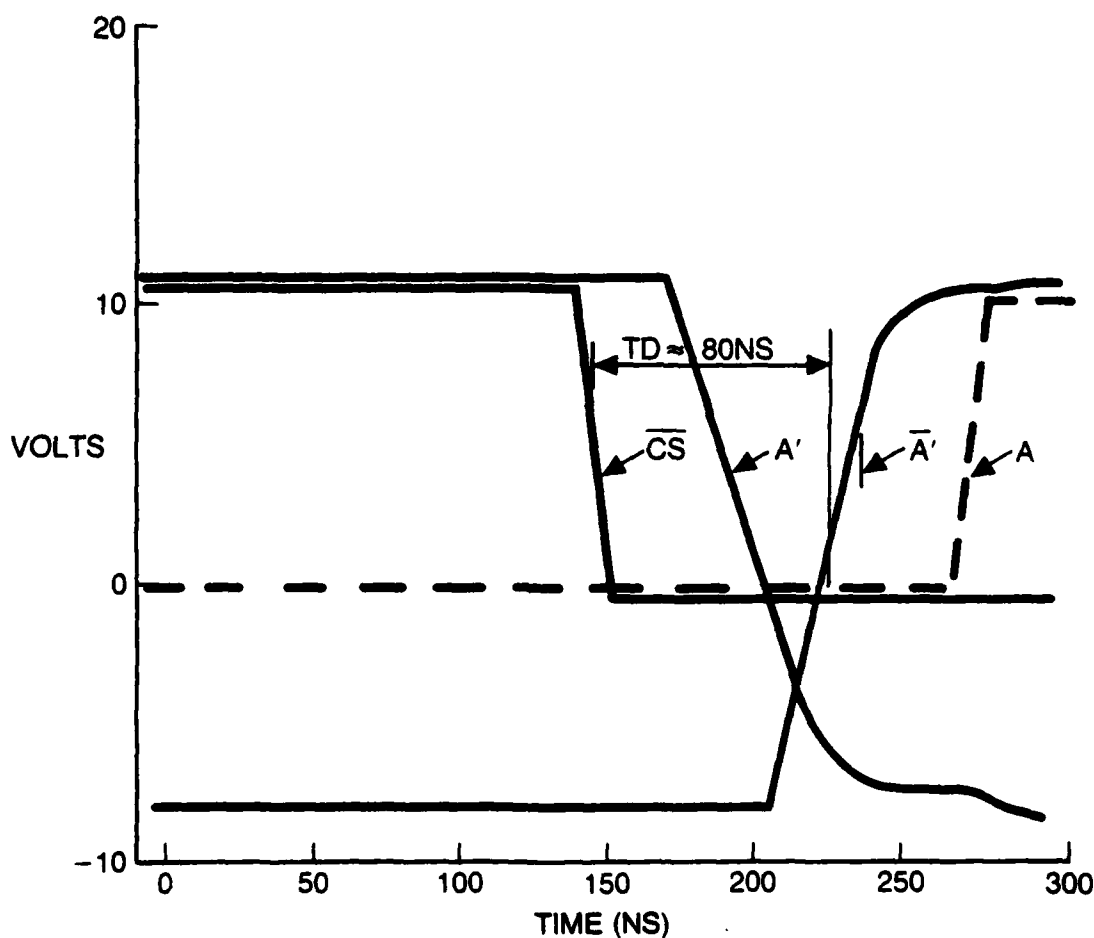
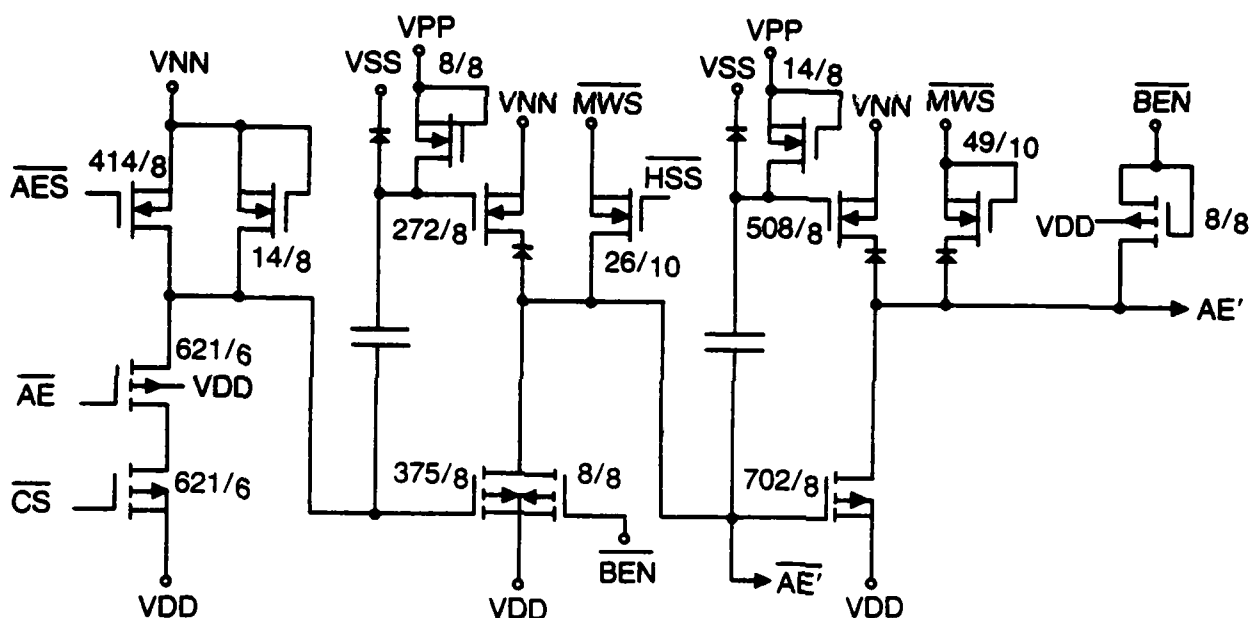


FIGURE 3.12 PSM: ADDRESS BUFFER SIMULATION POST RAD, 125°C

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NOTE: ALL W/L SHOWN IN  $\mu\text{M}$ .

52409

FIGURE 3.13 PSM: ADDRESS ENABLE BUFFER

Simulation results shown in figure 3.14 indicate the delay time to  $\overline{\text{AE}}$ , which enables the decoders, is 50 ns.

**3.1.5.2.3 Row (X) Decoder:** The X decoder shown in figure 3.15 used to select one of 64 rows of the memory array matrix once it is enabled with the  $\overline{\text{AE}}$  signal.

This type of decoder is known as a "tree" or series "and" decoder which dissipates no dc power. The Y-decoder, which is of the same design type, selects 4 of 16 columns at a time.

The simulated delay time between  $\overline{\text{AE}}$ , the decoder enable signal, and the X decoder output waveform which drives the memory gates is shown to be 120ns in figure 3.16.

**3.1.5.2.4 Memory Array Device:** A three FET model which uses two, fixed threshold transistors and one, variable threshold transistor to simulate the drain-source protected (DSP) memory device is shown in figure 3.17. Each memory cell in the array is made of two of DSP memory devices, one

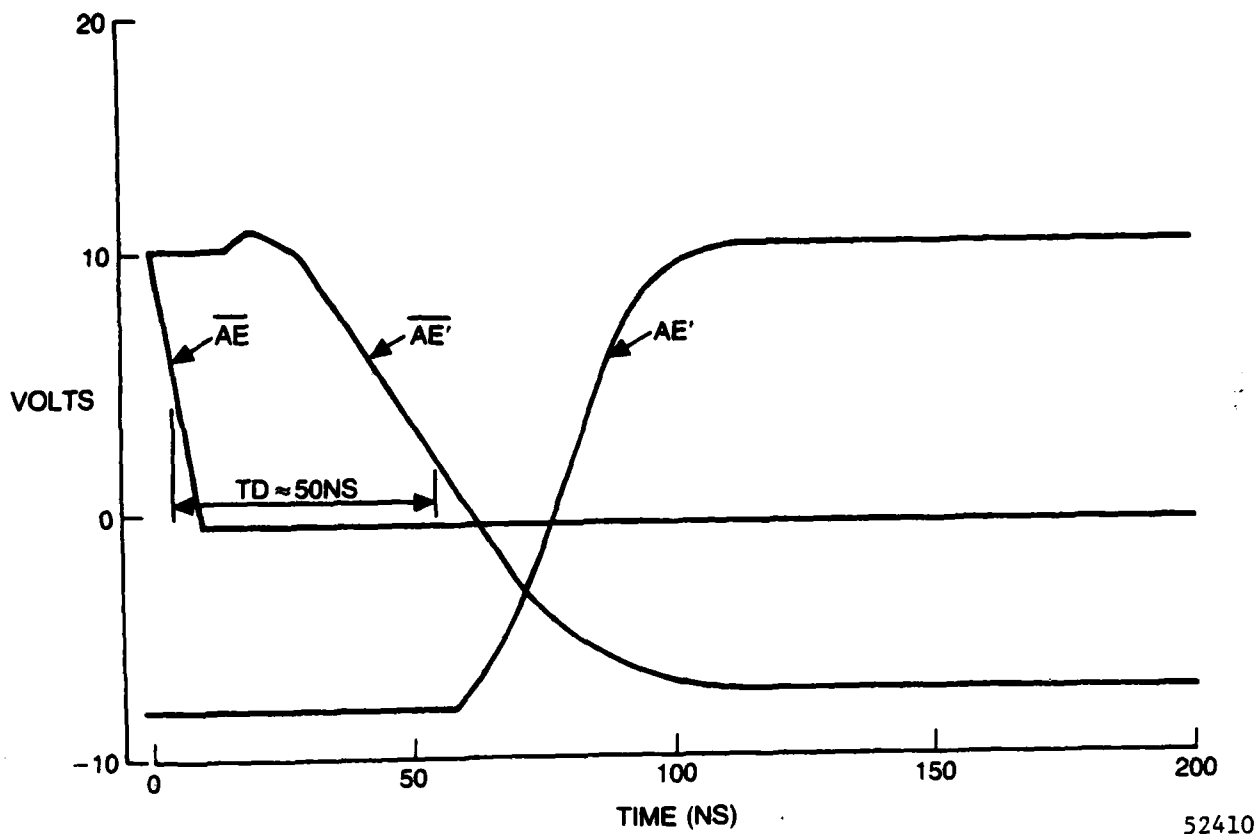


FIGURE 3.14 PSM: ADDRESS ENABLE BUFFER SIMULATION POST RAD, 125°C

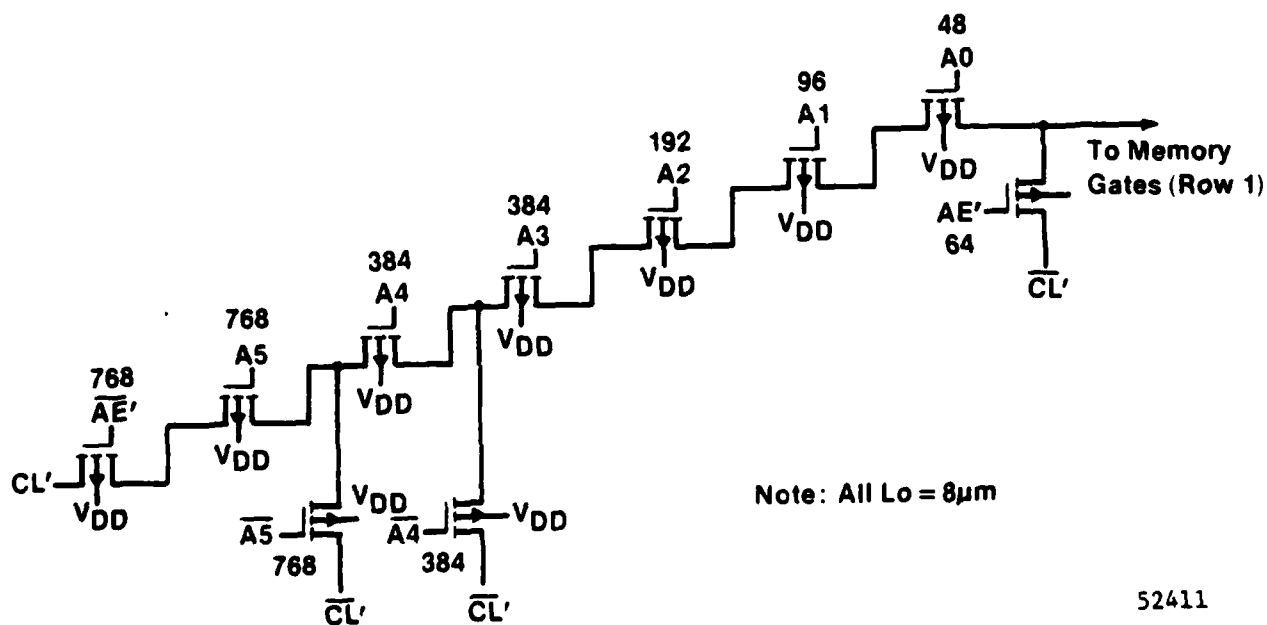


FIGURE 3.15 PSM: X DECODER (1 OF 64 ROWS)

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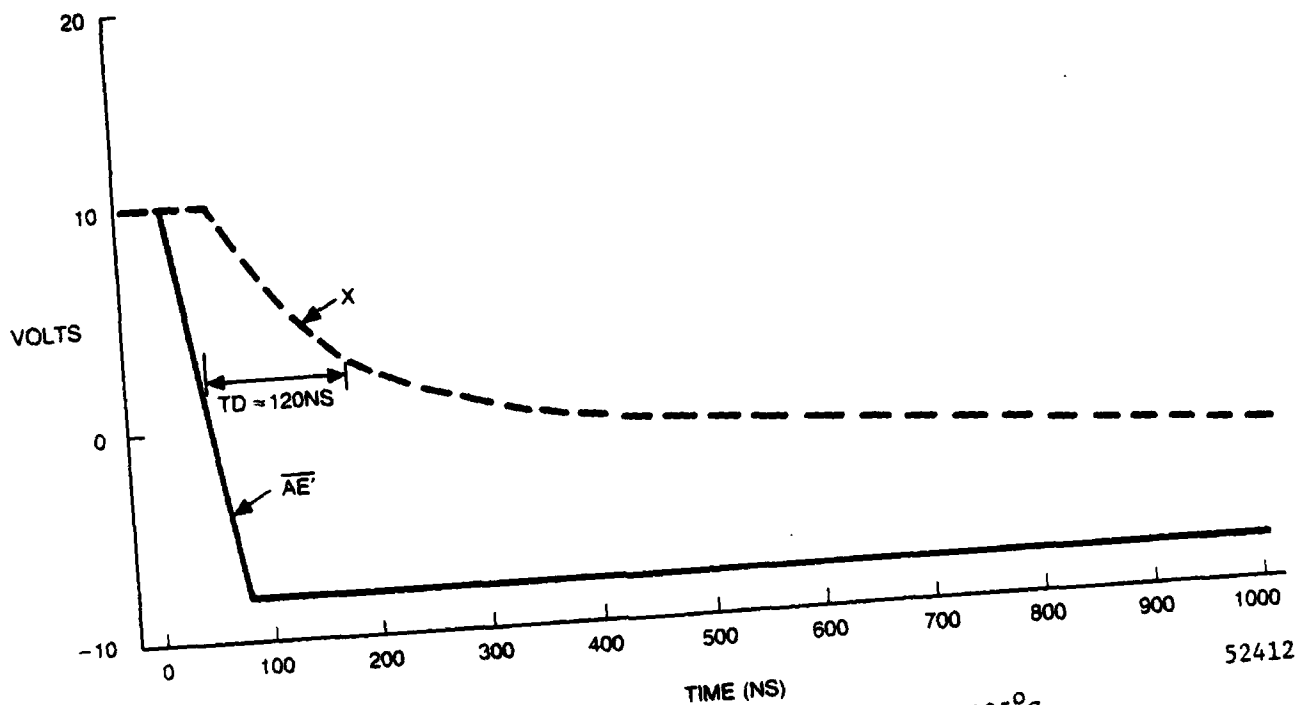


FIGURE 3.16 PSM: ROW DECODER SIMULATION POST RAD, 125°C

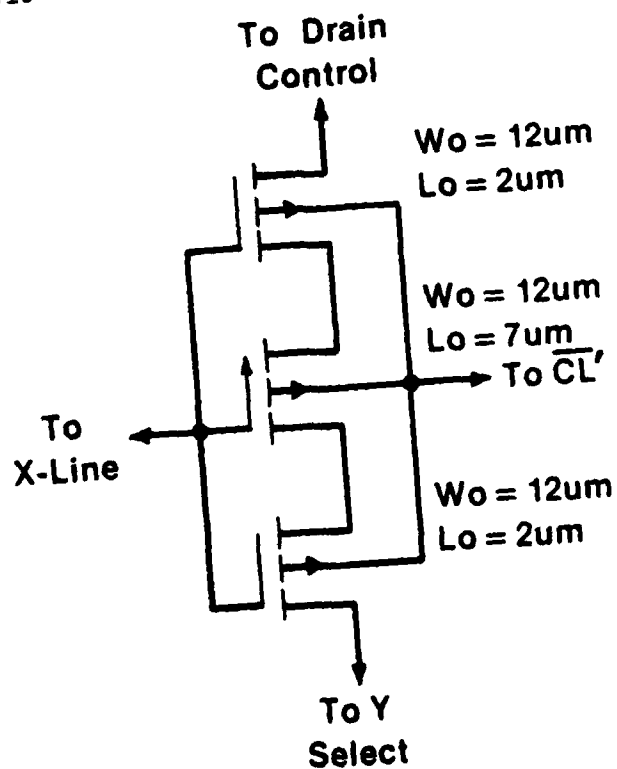


FIGURE 3.17 PSM: 3 FET MNOS MEMORY ARRAY DEVICE

This three FET model has proven successful in previous designs. Simulation results of the array are combined with those of the column detection circuit.

52414

FIGURE 3.18 PSM: COLUMN DETECTION CIRCUIT

The circuit is essentially a cross-coupled bistable latch. Initially both sides of the latch are reset to  $V_{DD}$ . Then both memory source line nodes begin to charge low at different rates through the two memory devices in the selected cell. The memory device in the high conductance state will supply more current to the latch and set the opposite side of the latch to  $V_{DD}$ , thus latching in the stored data information. This information is then passed on to the I/O circuit for buffering to the outside system data bus lines.

Two important features of this circuit should be pointed out.

A unique test feature is included so that the memory window, the difference in threshold voltages of the two memory elements which make up a cell, can be measured for all 1024 cells. This is done by disabling the latch and gating the proper waveforms to external pins at the MT and MT terminals. This type of information is invaluable in predicting actual endurance/retention characteristics of the array. A more detailed description of this circuit operation is contained in CDRL Item C002 Preliminary Specification for MNOS/SOS PSM Permanent Store Memory Part No. 6023 dated 20 July 1978.

The second feature yields greatly enhanced post rad functional performance resulting in much faster access time. This performance improvement is facilitated by devices P47 and P48 and the Delayed Read Clock (DR). Once a slight difference in current (and voltage) is established at the two nodes of the flip-flop the DR clock turns on P47 and P48 which supply equal and additional currents to the flip-flop. This additional current greatly increases the speed at which the flip-flop sets, thereby determining access time, while the currents from the memory cell are simply used to imbalance or "steer" the circuit to the proper state.

Simulation of the detection circuit is shown in figure 3.19 both with and without the Delayed Read Clock being applied. The speed advantages of using this clock are obvious. With delayed read the latch sets in approximately 200ns.

**3.1.5.2.6 Three State I/O Buffer:** The three-state I/O buffer shown in figure 3.20 is intended to buffer input data from the data bus into the detection latch in the write mode and to buffer data out of the detection latch onto the data bus during normal read mode of operation. System expansion is facilitated by having the I/O pins in a high-impedance state when a given chip is in the write mode or not selected.

The output section consists of a pair of two-stage buffers each of which is similar to the address buffer design. These buffers are driven by two complimentary signals,  $DO'$  and  $DO$ , from the detection circuit and in turn drive the p-channel output pair in push-pull fashion. The input section consists of a simple inverter gated on by write control signals.

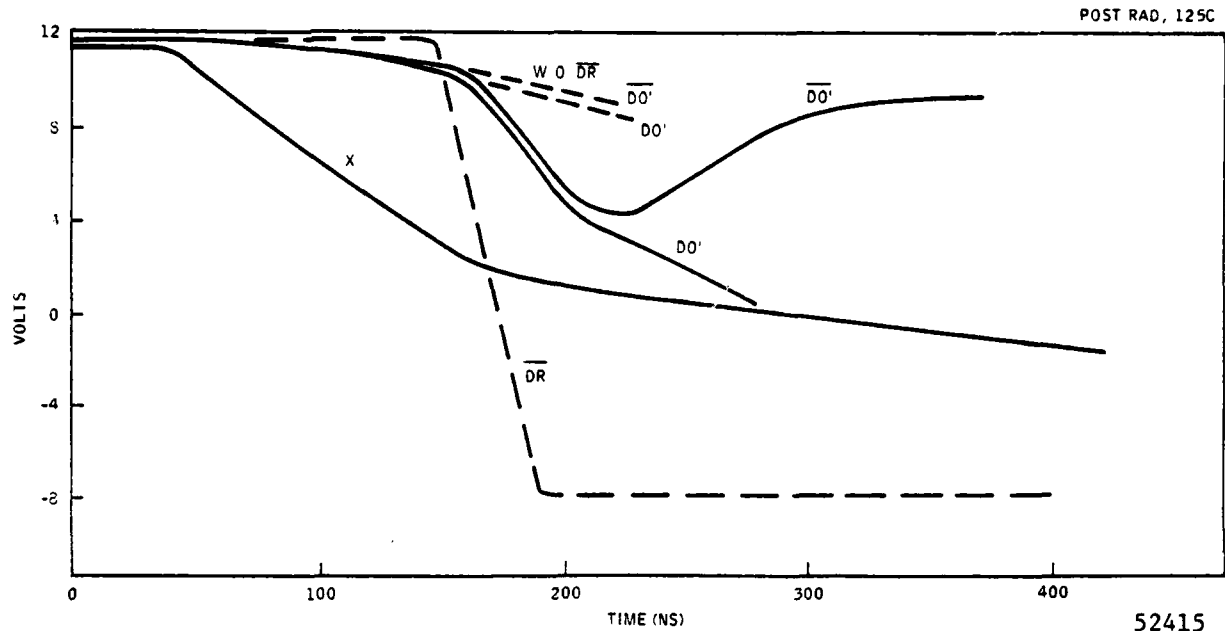


FIGURE 3.19 PSM: COLUMN DETECTION SIMULATION USING DELAYED READ,  $\overline{DR}$

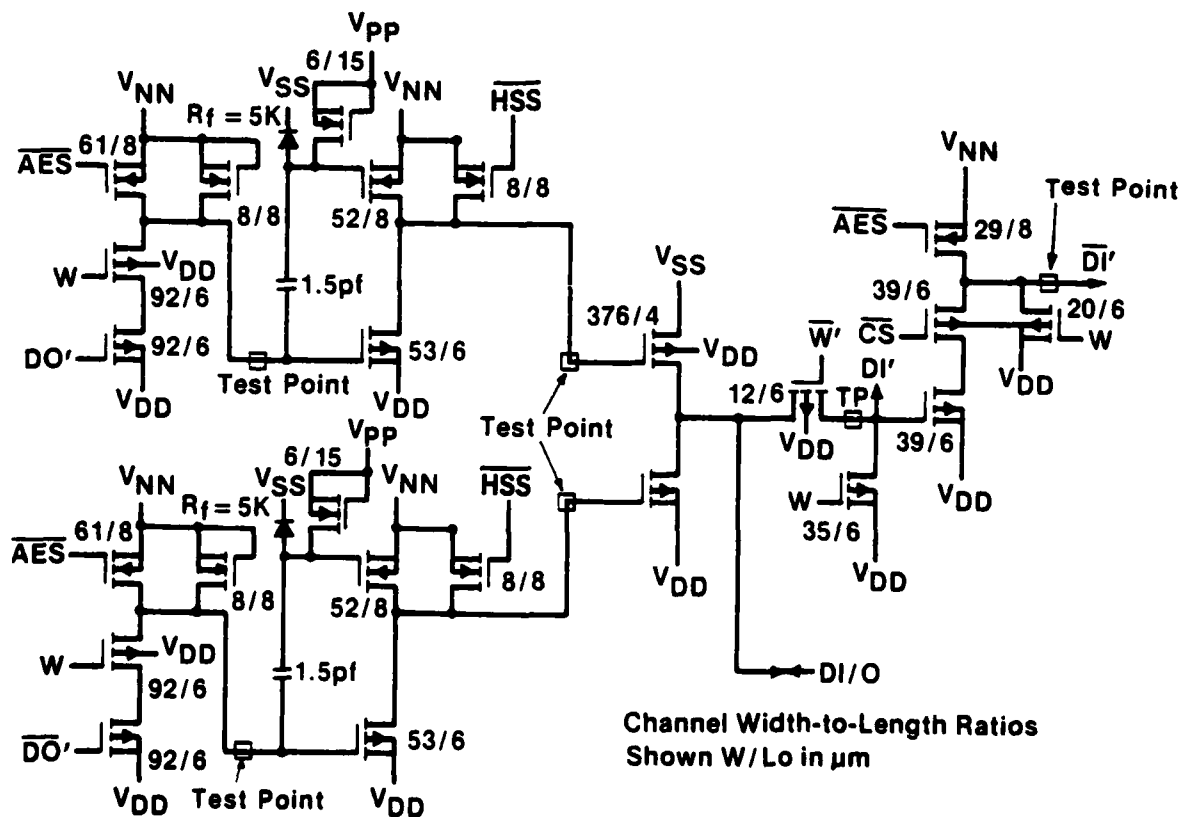
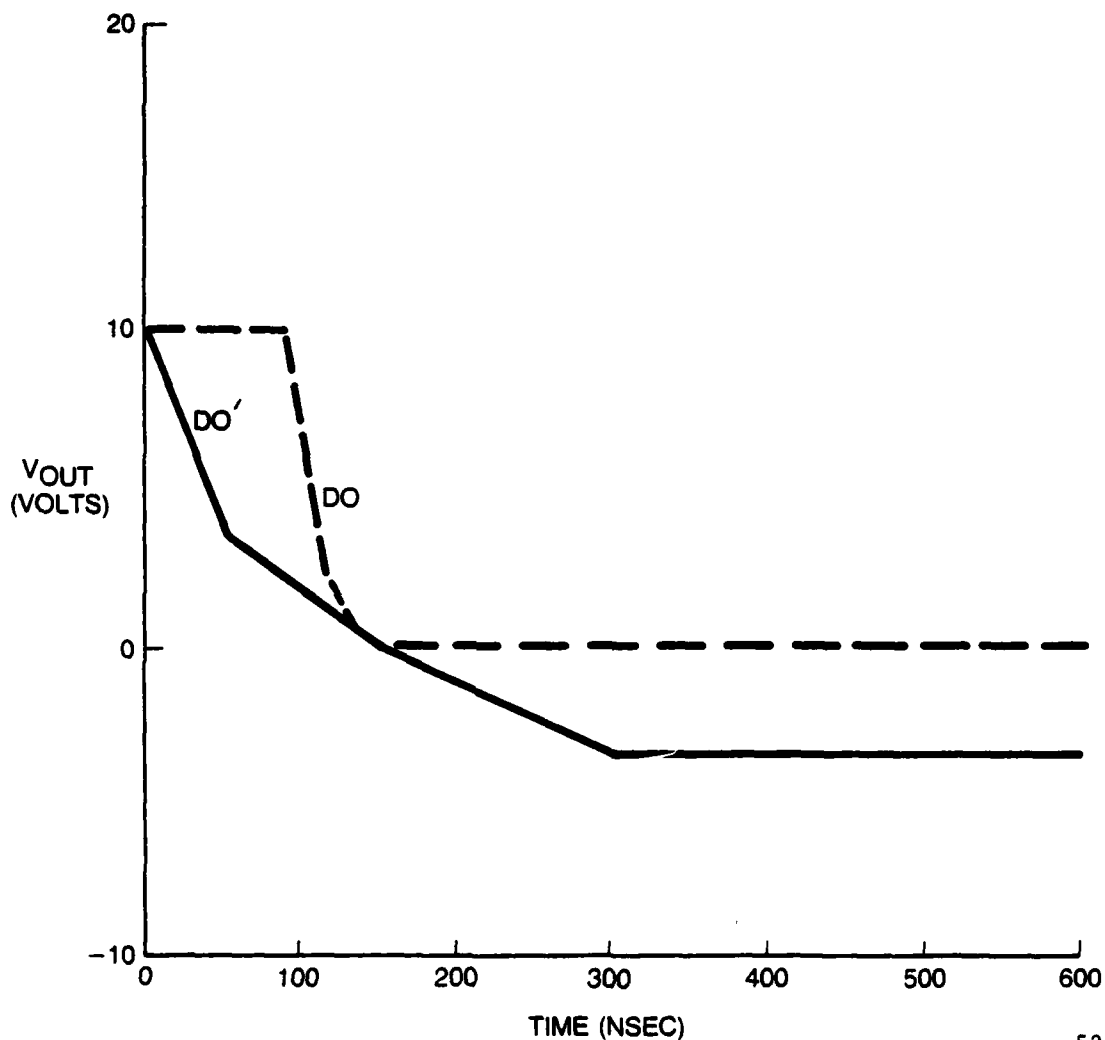


FIGURE 3.20 PSM: TRI-STATE I/O BUFFER

Output buffer simulation shown in figure 3.21 indicates an output delay of 60 ns.



52417

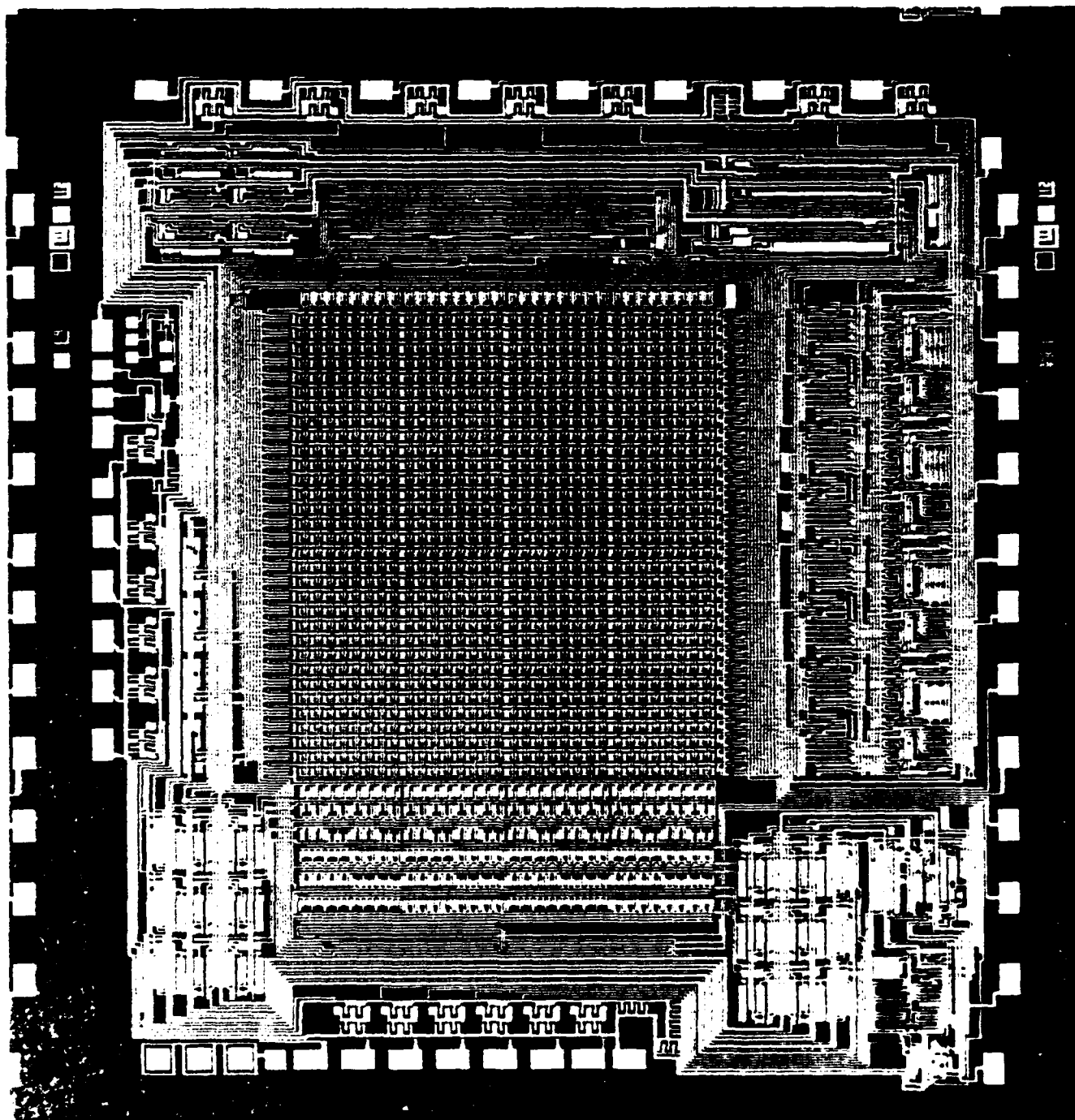
FIGURE 3.21 PSM: I/O BUFFER (DO) SIMULATION POST RAD, 125°C

### 3.1.5.3 6013 PSM Design Summary

All circuits of the 6013 PSM LSIC circuit were designed and simulated for worst case conditions. Simulation results indicated that the final LSI would meet the program goals for access time and low power dissipation. An actual die photo showing final interconnect layout of the 6013 is shown in Figure 3.22. Die size is 237 mils x 236 mils.

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ELECTRICALLY ALTERABLE READ ONLY MEMORY

FIGURE 3.22

## 3.1.6 PSM 6023 LSIC Design and Circuit Simulation

After completing the electrical and yield evaluation of the 6013 PSM LSIC, some minor mask modifications were determined to be beneficial to overall performance. This new mask set, 6023 was designed. A summary of the changes made to the original 6013 to generate the 6023 are shown below:

### PSM MASK DESIGN CHANGES

- Change I/O 3 crossunder to correspond to other I/O's and increase CW size
- Standardization of I/O protect networks
- Connect second size of test FET input protect network
- Change memory window test feature circuitry to avoid unnecessary power dissipation
- Relayout of DR buffer to avoid jutting corner in mask
- Computer-aided design rule check
- Addition of load element to improve security block clear-write

#### 3.1.6.1 Computer Aided Design Rule Checks

Prior to making any changes to the 6013 mask set, it was checked for possible design rule violations. This was done automatically through a CAD service provided by NCA Corporation of Santa Clara, California. The design rule violations checked for are summarized below:  
Only one violation was found, that being a metal to metal spacing which was corrected prior to generation of the 6023 mask set.

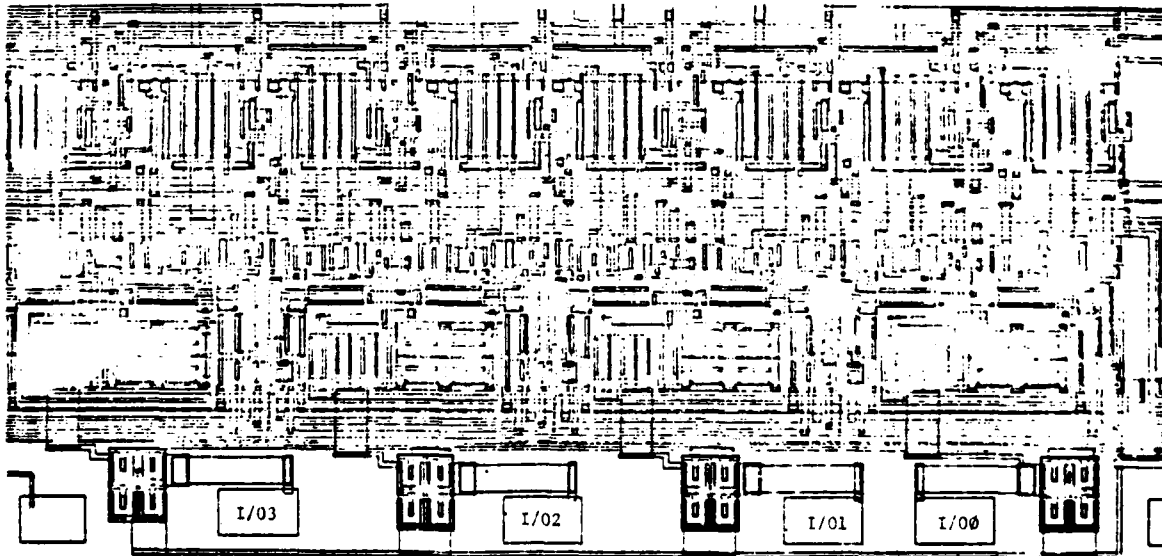
#### 6013 COMPUTER-AIDED DESIGN RULE CHECKS BY NCA

- |   |                 |
|---|-----------------|
| • Minimum metal to metal spacing                                  | 8 $\mu\text{m}$ |
| • Metal overlap of gate protect                                   | 1 $\mu\text{m}$ |
| • Gate protect overlap of silicon island                          | 4 $\mu\text{m}$ |
| • Minimum contact window over silicon island                      | 6 $\mu\text{m}$ |
| • Minimum N+ or P+ spacing to silicon island with opposite dopant | 6 $\mu\text{m}$ |

### 3.1.6.2 I/O Protect Network Modifications

It was noted during transient radiation testing and during functional test of the 6013 that the I/O3 output did not have the current sink capability of the other three I/O ports. This problem was traced to a unique narrow N+ crossunder on the I/O3 output line. In the 6023 modification all I/O crossunders were made identical and output protect networks were added as shown in figure 3.24. A close-up of the output protect network along with component values is shown in figure 3.25.

An improved input protect network was also designed and included in the 6023 mask set and is shown in figure 3.26 along with an old type. Details of input protect networks are included in another section of the report.



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FIGURE 3.24 PSM 6023: I/O PROTECT NETWORK

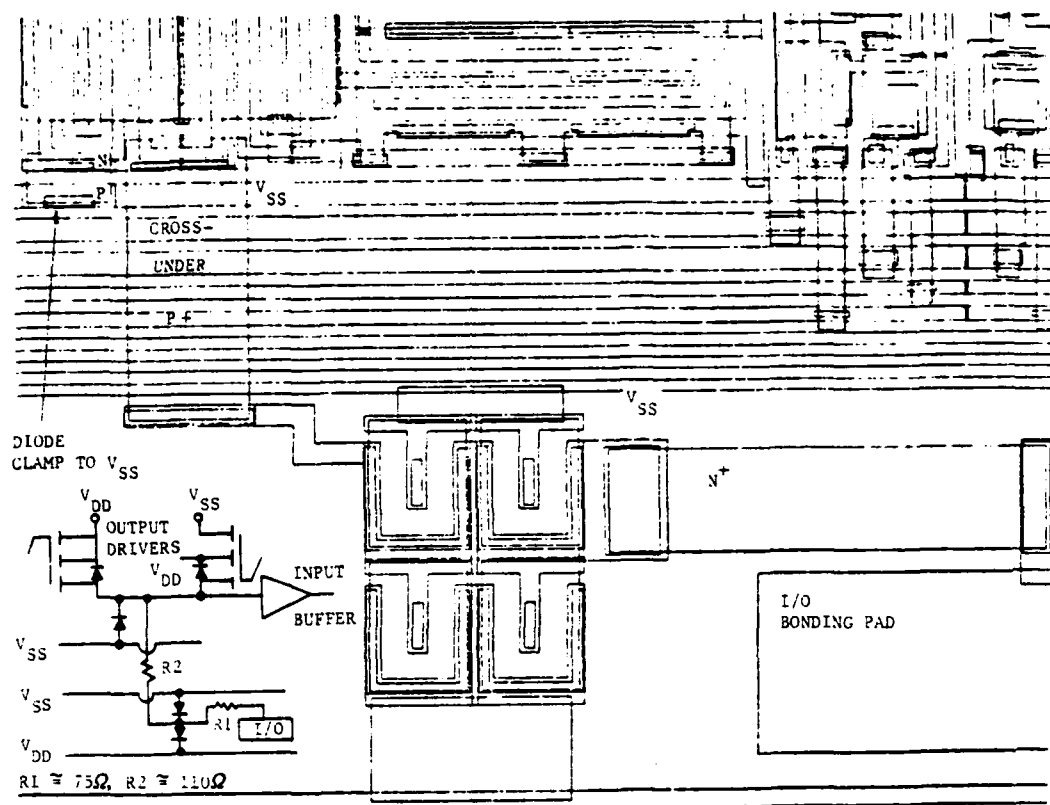


FIGURE 3.25 PSM 6023: OUTPUT PROTECT NETWORK

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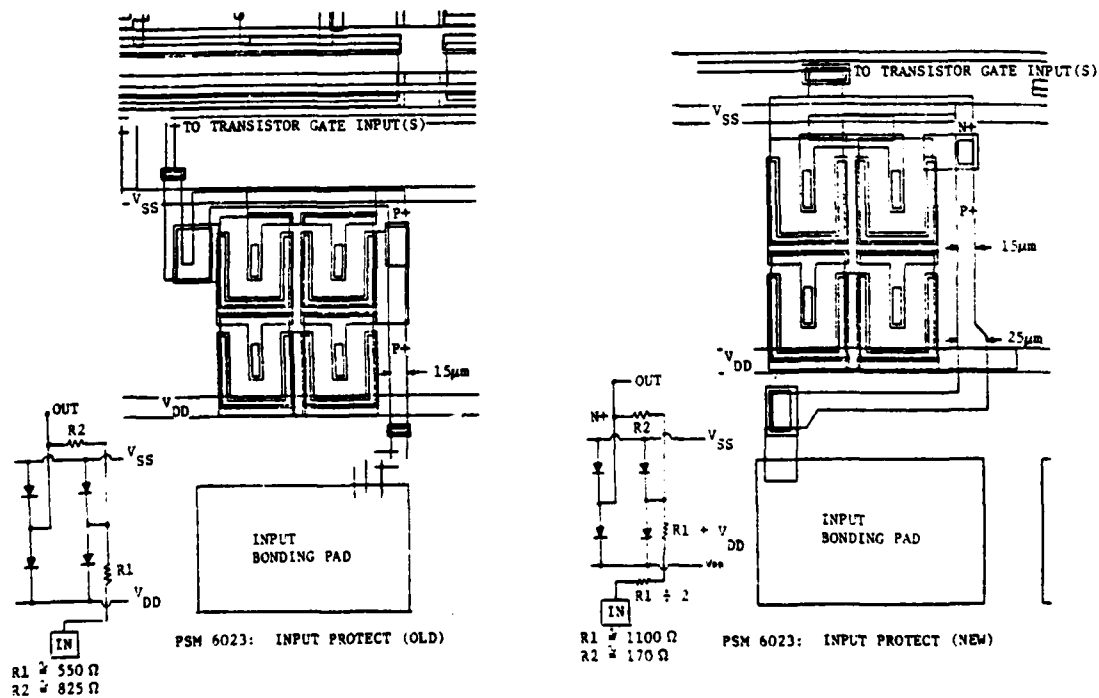


FIGURE 3.26 PSM 6023: INPUT PROTECT (OLD)

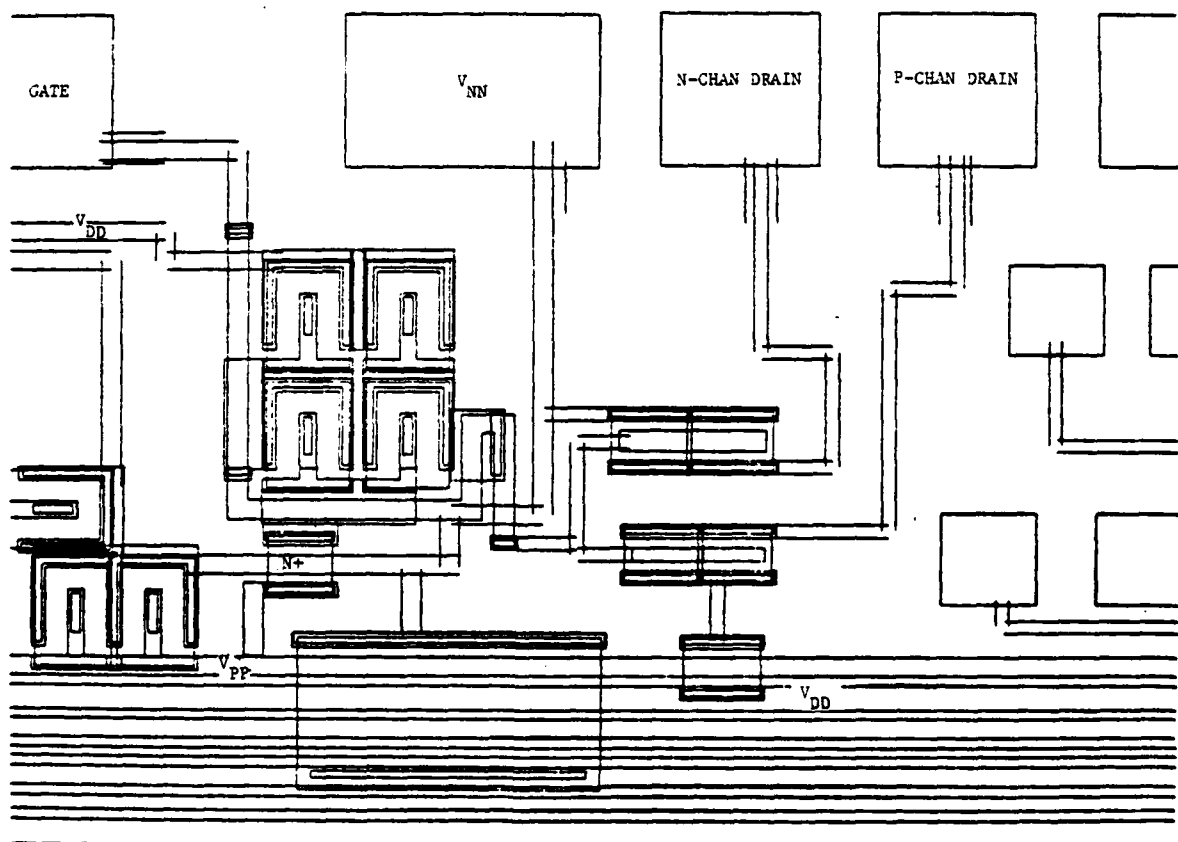
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On the 6013, one side of the input protect network to the test inverter was not connected to a supply. On the 6023 mask this connection was made to provide adequate protection and is shown in figure 3.27.

A more complete description of the input protect network development is given in section 2, reference

### 3.1.6.3 Memory Window Test Circuit Change

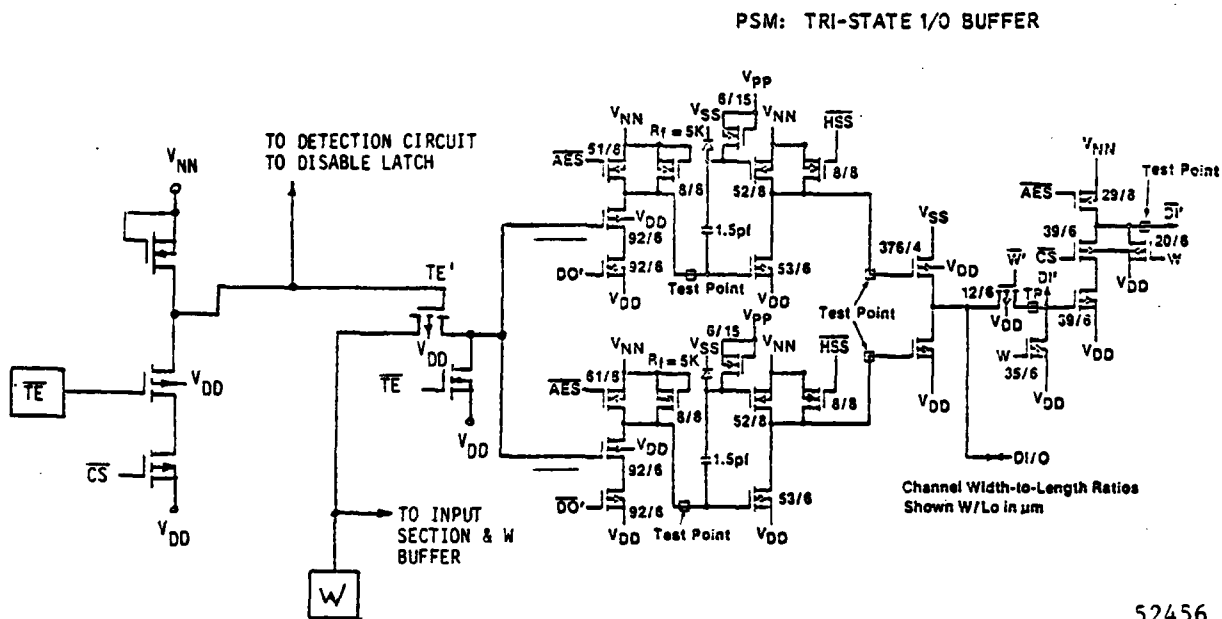
It was found on the 6013 design that when the chip was operated in the memory window test mode of operation that the array dissipated an abnormal amount of power, mainly from the  $V_{DD}$  supply. This was because the I/O buffer was no longer being driven by complimentary inputs, both p-channel devices in the output driver pair were turned on at the same time, conducting much current.



52419

FIGURE 3.27 PSM 6023: TEST FET INPUT PROTECT

This problem was remedied by the addition of the circuit shown in figure 3.28 which completely disables the I/O buffer (puts it in the high impedance output state) when the array is in the memory window test mode of operation.



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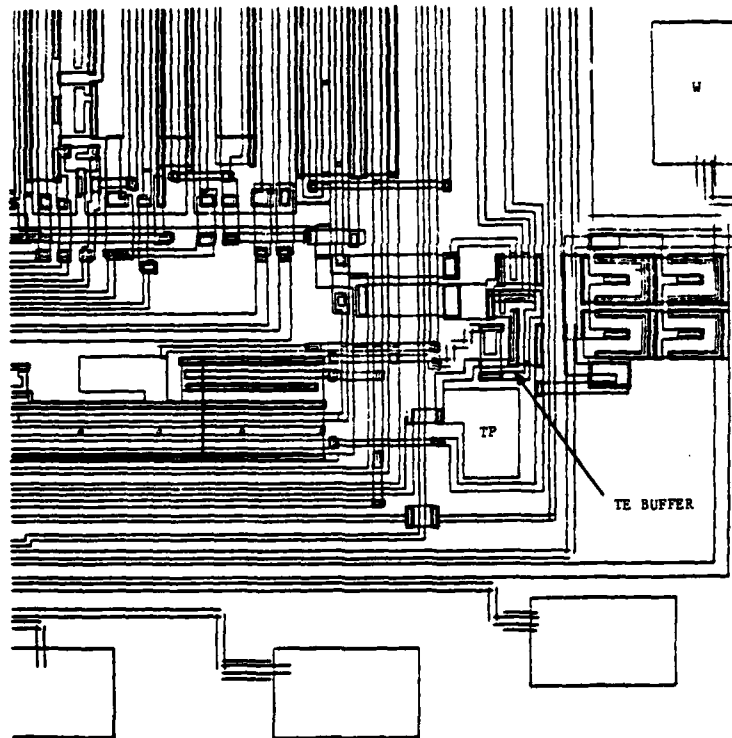
FIGURE 3.28 PSM 6013: MEMORY WINDOW TEST CIRCUITRY CHANGE

ISPIICE simulation of this circuit is shown in figures 3.29 and 3.30 while the layout of the cell and placement within the array is shown in figure 3.31. Note that the addition of this cell did not cause the die size to increase.

#### 3.1.6.4 Relayout of Delayed Read (DR) Buffer

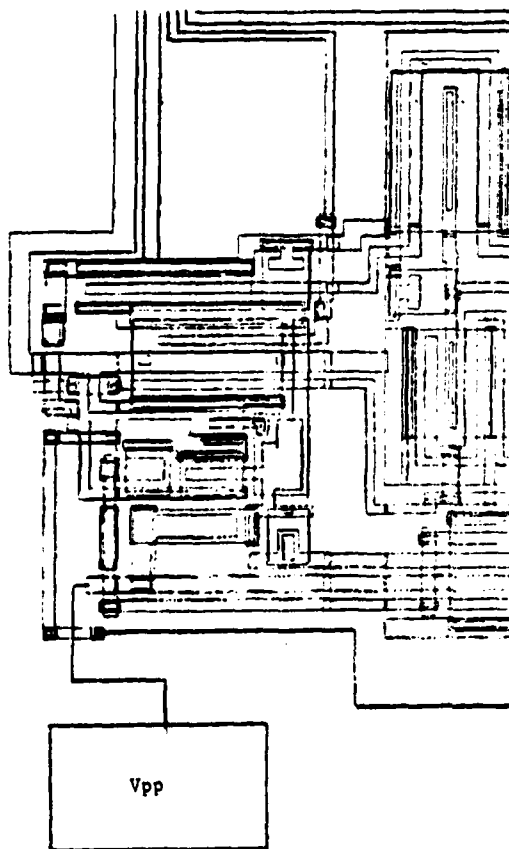
It can be noted from figure 3.32(A) that the DR buffer layout in the lower left hand corner of the 6013 array was not optimum. The outer bus line juttred out past the rest of the circuitry and pads. It was occasionally damaged during the wafer sawing operation in parts assembly.



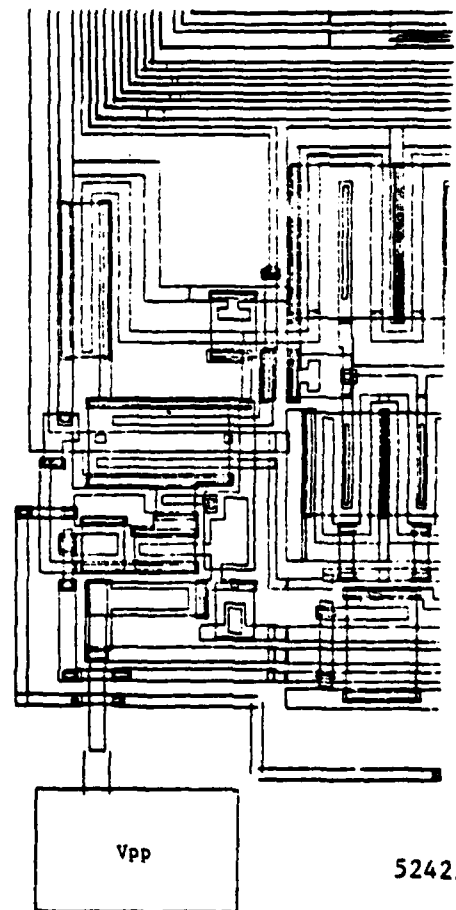


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FIGURE 3.31 PSM 6023: TE BUFFER LAYOUT



PSM 6013: LOWER LEFT HAND CORNER (A)



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PSM 6023: LOWER LEFT HAND CORNER (B)

FIGURE 3.32

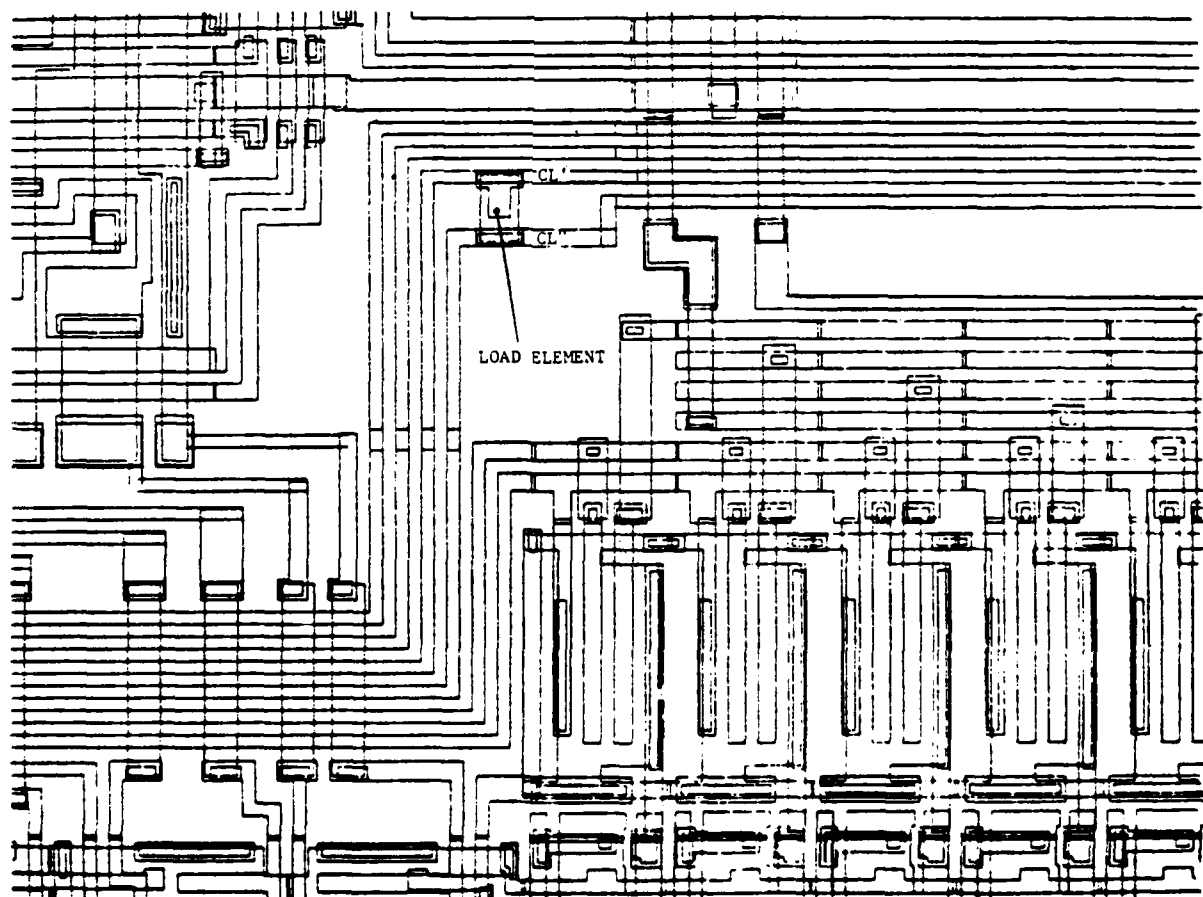
In the 6023, this buffer was relayed out so that this bus line came straight down the side of the die. Because of this, no further yield losses of this sort occurred during the sawing operation.

#### 3.1.6.5 Security Block Clear-Write Load Element

An additional load element was included in the 6023 mask set to facilitate the security block clear-write function of the array. Layout and array placement of this device is shown in figure 3.33.

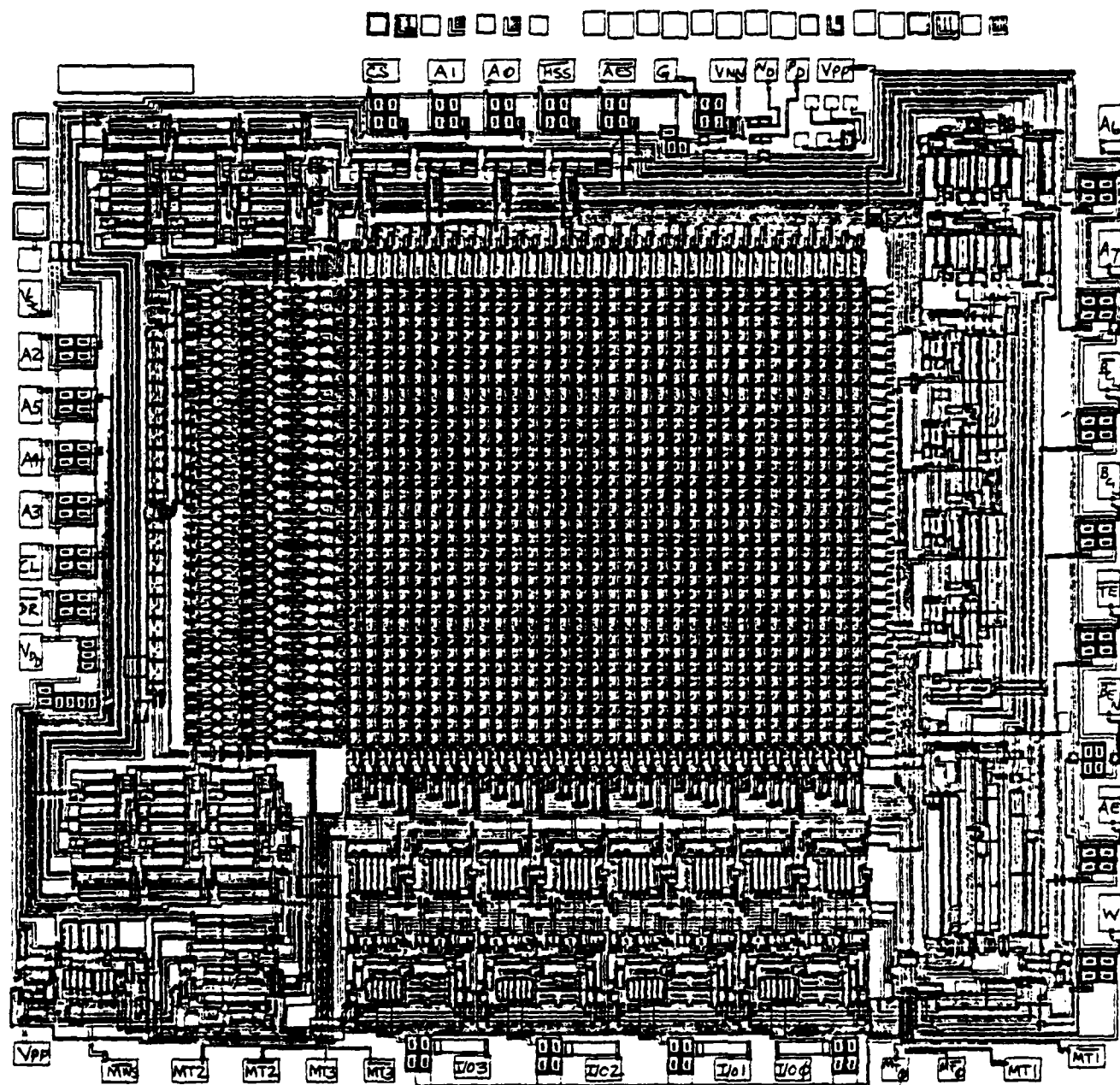
#### 3.1.6.6 6023 Mask and Circuit Design Summary

With minor mask modifications to the 6013 mask set, the 6023 mask set was designed. The changes incorporated improved both yield and electrical performance characteristics of the PSM LSIC. Metal interconnect for the 6023 PSM is shown in figure 3.34. Die size is still 237 mils x 260 mils.



52423

FIGURE 3.33 PSM 6023: SECURITY BLOCK CLEAR-WRITE LOAD ELEMENT



52424

FIGURE 3.34 PSM 6023

### 3.1.7 PSM LSIC Test Equipment and Programs

In order to test the PSM LSIC in a thorough and cost-effective manner, sophisticated state of the art test equipment must be employed. At Westinghouse two such test systems were used at both the wafer test and package test levels. These two LSI test systems, the Macrodata 154 and Macrodata 501 are described in significant detail below.

In addition to these two test systems, a laboratory test set of in-house design was used extensively for engineering characterization of the PSM LSIC in packaged form.

#### 3.1.7.1 Macrodata 154 Test System

The MD-154, shown in figure 3.35, is a very high speed system designed for automatic testing of semiconductor devices and systems at rates up to 10MHz. Both functional tests and precision dc measurements are performed, separately or in combination, thereby satisfying the specific needs of testing at all stages of manufacture and for engineering evaluation. Reports of various kinds can be printed.

The system is completely general purpose. It can be used equally well for almost any kind of memory or logic array, including core memories. The semiconductor storage devices can be any type--shift registers, random access memories (RAM's), read-only memories (ROM's), and content-addressable memories (CAM's). They can be static or multiphase dynamic, bipolar or MOS. The logic arrays can include any scale of integrated logic circuitry, small, medium, or large. They can have such functions as counters and timers, or they can be structured as random logic, from a simple configuration to the most complex. The testing of ROM's and very complex logic requires the buffer memory to store the ROM or logic pattern.

This versatility lends the system to use in wafer probe, package test, card test, system test, or engineering characterizations for design. The system includes a functional test whose high-speed RAM can store standard and custom routines tailored to the memory or logic device, allowing the system to be programmed for special test sequences that are peculiar to individual requirements. Device handling equipment also can be controlled.

The MD-154 is a cascaded test system composed of modules under computer control. Each module is relatively autonomous and can function independently of the other units. Master control resides in the sequencer, which transfers data and control to or from the modules as necessary to accomplish the test activity. The modules in the MD-154 system are:

- a) Sequencer (MD-55), for test control and data storage,
- b) Pattern Generator (MD-104), for functional testing,
- c) Automatic Parameter Tester (MD-84), for dc testing,

MACRODATA MD-154  
LSI AUTOMATIC TESTER



42776

- d) Programmable Power Supply (MD-45), for V and I,
- e) Programmable Clock Generator (MD-74), for timing,
- f) Pin Electronics (MD-34), for device-system interconnection, and
- g) Teletype (ASR-33), for data entry.

The system regards the device under test (DUT) as a logical black box, regardless of whether it is actually a logic unit or a storage device. Testing becomes primarily a matter of suitable interfacing between the DUT and the MD-154 under programmed control. The conditions required for test, including signal levels, timing, and test patterns, are made available to the Pin Electronics module for proper connection to the device. This module consists of a test head for physical mounting of the DUT plus a switching matrix for connection of each device pin to either (a) any required input signal or supply voltage, or (b) any output channel for measurement or comparison. The system can handle equally well a breadboard model of four bits, a chip of 1024 bits, or a system of 64K words.

During functional testing, control is transferred to the MD-104 Pattern Generator. The power of the MD-104 derives from its being a microprogrammed processor that allows algorithmic generation of patterns. The functional test program is stored within the MD-104's own internal control memory.

An advantageous consequence is that the algorithmic test patterns can be generated at optimum efficiency without time lost in calculation. This inherent capability for high speed, when coupled to the fast clock cycle of 100nsec. allows the system to operate at continuous test rates of up to 10MHz.

The random-access data buffer memory under control of the MD-104 processor permits a similar efficiency for testing ROM's or complex random logic devices without the overhead that must be carried by the classical large general-purpose LSI testers.

For parametric measurements, control is transferred to the Automatic Parameter Tester. These dc tests are also made at high speed, retarded only by the time required to change connection from one device pin to another by relay action. The results of tests can be reflected into logging (counting) of individual kinds of tests as having either passed or failed.

### 3.1.7.2 Macrodata MD-501 Test System

In the electrical test area, a recently (1977) installed Macrodata MD-501 Test System is highlighted as a significant increase in capability at ATL for the production testing of LSI circuitry. A summary of the Macrodata MD-501 significant points is presented in the following paragraphs.

## 3.1.7.2.1 General Characteristics

The MD-501 system has been created with two basic goals in mind. Primarily, it is meant to provide versatility and speedy, efficient, accurate testing of virtually all types of LSI/MOS and bipolar devices on the market today, including RAM, ROM, and circuit logic arrays. Second, the MD-501 is designed to be simple to use, at the same time providing all the multileveled power and setup data necessary to accomplish its primary task. The major features provided by the MD-501 are described below.

- a) Concurrent Test Execution and Compilation: The number of users that can use the system at one time is one more than the number of test heads available (one test head is standard) up to a maximum total of four users. A user can be using the system compiler software while the system is performing tests concurrently.
- b) Statistical Analysis of Test Results: Allows hard copy management reports such as binning summaries, histograms, and machine usage criteria.
- c) Tests both MNOS and Bipolar Devices: Up to 64 channels at data rates as high as 10MHz. Accepts a 64-pin dedicated ECL test lead with 50psec resolution. This addition is planned for 1978.
- d) Concurrent High-Speed Functional and DC Parametric Testing: Testing of either type also can be done independently of each other. Many tests can be performed manually, using various system modules, from the front panel controls.
- e) Up to Eight Digital Programmable Clocks are Available: Each clock is individually programmable with independent frequencies. Double strobing within a single clock period is possible.
- f) Up to 13 Independently Programmable Power Supplies: Device power and reference voltages and currents. Nine are standard.
- g) Subroutine Nesting Capability: Test generation is reduced because sub-routines can be nested in any fashion, coded once, and permanently stored.
- h) Stored "Macro" Test Subroutines: Immediately available to be called by the user through the operating system software (TCOM) for automatic functional and parametric tests as required.
- i) A Data Buffer Memory and a Superbuffer Memory: Optionally available for increasing system utility and data storage.

## 3.1.7.2.2 Test and Operation

In the MD-501 system, functional and parametric testing of LSI/MOS and bipolar devices can be done either at the wafer level or at the completely

packaged device level. Input/output testing can be done at speeds as high as a 10 MHz data rate. System capability also includes the testing of multi-phase dynamic and static devices in either high volume production or design-engineering environments. The system uses a high level, easy-to-use test language called TCOM, developed by Macrodata specifically for use on the MD-501 Test System.

The system regards the DUT as a "logical" black box. Testing becomes primarily a matter of suitable interfacing between the DUT and program control. The conditions required for test are made available to the pin electronics for proper connection to the device. This consists of a test head for physically mounting the DUT, and an electronic switching matrix for connecting each device pin to form the desired pin-test configuration. This allows wafers to be tested by connecting the MD-501 to a probe test stand or packaged devices to be tested by plugging a switchable socket board onto the MD-501 test head.

### 3.1.7.3 PSM Laboratory Test Set

The PSM lab test set shown in figure 3.36 is used to functionally operate both 6013 and 6023 LSIC memory devices. Single, continuous, or a preset number of cycles may be run for clear, write, clear/write, and read modes of operation. All, single, or a preset number of addresses may also be cycled through in any mode.

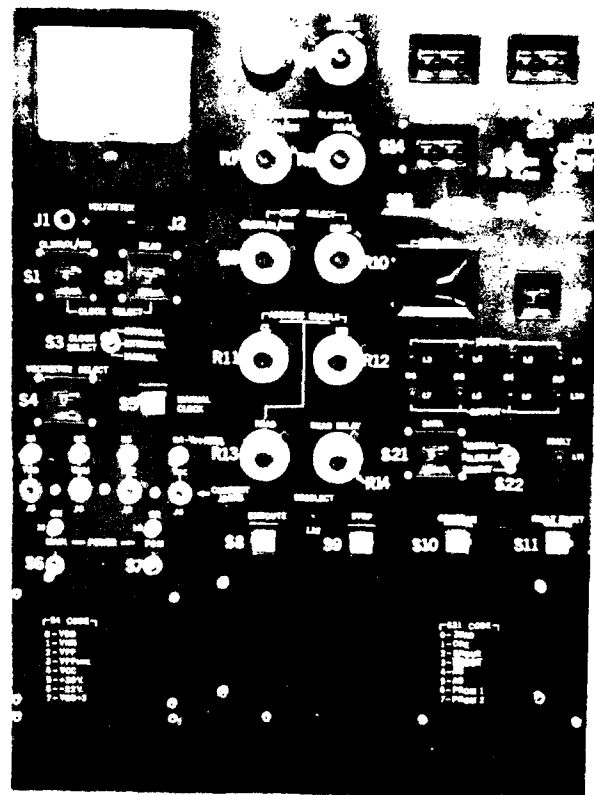
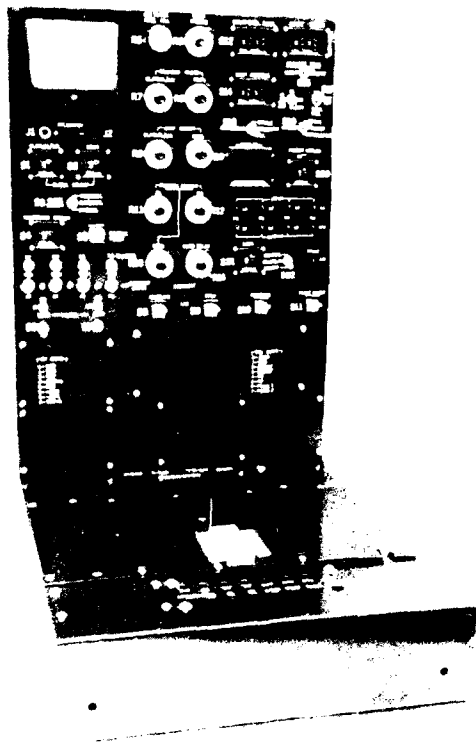
In the read mode, data comparison is made. The tester can run continuously indicating a fault or can stop on fault displaying error address, proper data, and actual data readout at that address.

In addition there is a memory test mode which will allow readout of memory windows.

There are several front panel adjustments which facilitate characterization of electrical performance for the PSM. Adjustments for all PSM input signal pulse widths as well as cycle time for all modes of operation are included for timing evaluation. In addition, all supply voltages and input signal swings may be varied several volts for margin testing. Supply current jacks are included to monitor PSM power dissipation for the various modes of operation.

### 3.1.7.4 PSM LSIC Test Programs

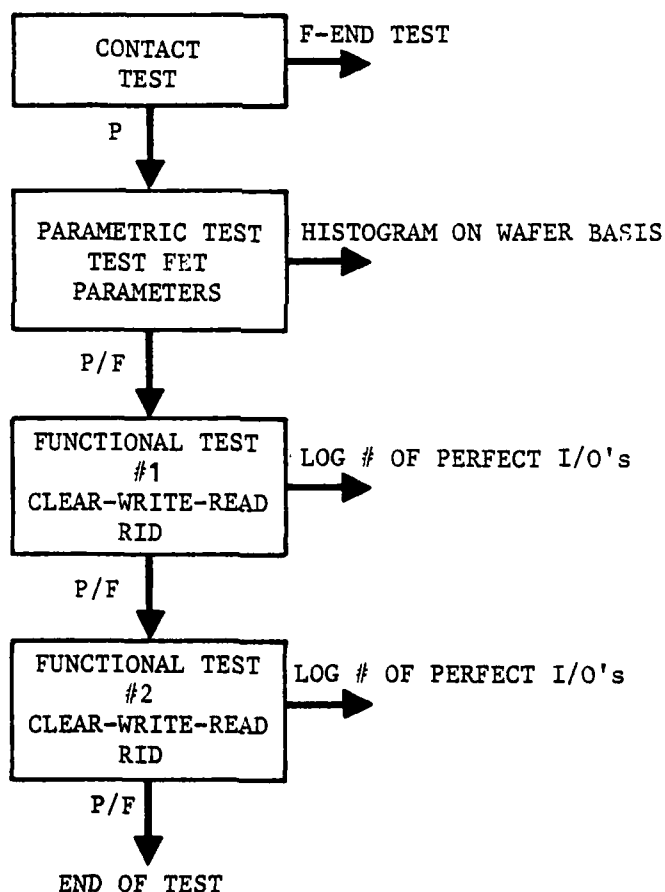
Several test programs were generated to fully characterize operation of the PSM LSIC. These include both wafer and package tests.



## 3.1.7.4.1 PSM Wafer Test Program

Initially the PSM arrays are tested in wafer form on the MD-154 test system so that selection of devices for packaging/screen can be made.

The wafer test flow diagram is shown in figure 3.37. DC measurements of test FET parameters are made as well as a functional test of array performance. Maximum test time per die is about 3 seconds.



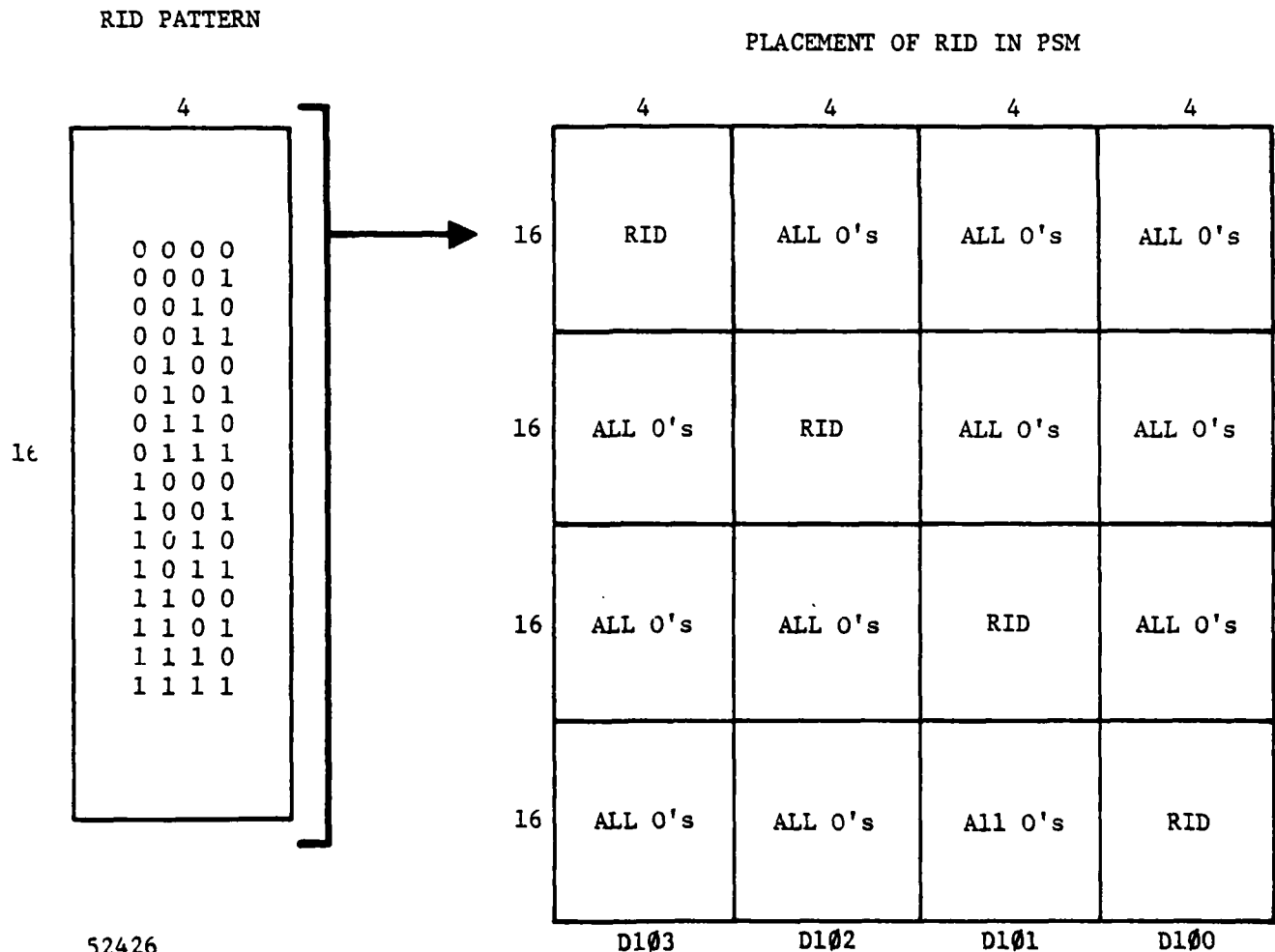
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ALL FUNCTIONAL TESTS DONE WITH NOMINAL SUPPLIES ( $V_{DD} = +12V$ ,  $V_{SS} = 0V$ ,  $V_{NN} = -9V$ ,  $V_{PP} = -18V$ ). LOOSE READ MODE TIMING

FIGURE 3.37 SIMPLIFIED 6023 WAFER TEST FLOW DIAGRAM ID = MX6023 W1REV00

a) Parametric Test Measurements: Parametric tests include both p-and n-channel device threshold voltages as well as source drain leakage currents.

b) Functional Test Measurements: Functional testing is done with a Repetitive Incrementing Diagonal (RID) test pattern and its compliment (RID\*) which were developed by Westinghouse specifically for PSM testing. The RID pattern shown in figure 3.38 results in a unique row and column pattern being written into the memory. If there are any defects in the decoder which produce multiple addresses or no addresses to some cells they will be detected using this pattern. It could be thought of as an address verification pattern. Also, by testing the array with the compliment of this pattern in addition to RID, proper data storage of both "1's" and "0's" can be verified for each storage cell.



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FIGURE 3.38 REPETITIVE INCREMENTING DIAGONAL (RID) TEST PATTERN

c) Data Output Reports Results: Output results from wafer test may be reported in one or a combination of ways. In all cases an LED display attached to the MD-154 shows the number of perfect I/O sections (a maximum of 4) for both the RID and RID\* test pattern. This data is recorded by an operator on a wafer map.

In addition, both parametric and functional test results may be printed out as shown in figure 3.39.

The program also has the capability to provide frequency histograms for parametric measurements. Through operator control, these histograms may contain data from a single wafer, a complete lot, or several lots. A sample printout of a frequency histogram table and plot for p-channel threshold voltage,  $V_{Tp}$ , is shown in figure 3.40.

### 3.1.7.4.2 PSM Package Test Programs

Based on the results of wafer test, good dice then begin the screen on MIL-STD-883 level B. Once the devices are packaged they must be inspected, stressed, and tested several times during the screen flow.

Two programs, 6013/6023 P2 and 6013/6023 P3, were generated on the MD-154 to test packaged parts. The P3 test, which takes about 1.5 minutes per package, is used for intermediate tests while the P2 test, which takes 3 minutes per package, is used for final electrical test.

Both of these programs contain numerous functional and parametric tests designed to completely test all aspects of device performance. Output of test results is hardcopy from a high speed line printer. The tests are best summarized by examining sample printouts from both test programs which have the tests coded. These are included in the following pages. A more detailed explanation of some of these tests is contained in CDRL item C002: Preliminary Specification for MNOS/SOS Permanent Store Memory, Part No. 6023, dated 20 July 1978.

### 3.1.7.5 PSM LSIC Memory Window Test

As previously mentioned, the PSM LSIC has a unique test feature which allows one to measure the memory window of all 1024 memory cells. This feature is invaluable for making long term endurance/retention measurements which are directly applicable to actual array performance.

#### 3.1.7.5.1 Laboratory Test Set Techniques

Originally all memory window endurance/retention measurements were made using the lab test set. Window measurements were made by connecting the

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1 SWN	21 PRN	1 M9,80A-1 V	STA 000100	P CONTACT	
1 SWN	22 PRN	2 M1,0A-2 UA	STA 000100	P ILP	
1 SWN	23 PRN	3 M-4,5A-2 UA	STA 000100	P I-LN	
1 SWN	24 PRN	4 M-3,95A0 V	STA 000100	P VTP	
1 SWN	25 PRN	5 M-6,50A2 UA	STA 000100	P IDSC	
1 SWN	30 PTN	1 A000000 X000000 T000000 M020263 0177777 R003 C004 J000 Y000 MP000000 020263			CLEAR
1 SWN	31 PTN	2 A000000 X000000 T177776 M020201 0177777 R003 C022 J000 Y000 MP000000 020201			WRITE PS
1 SWN	32 PTN	3 A000000 X000000 T177776 M020201 0177777 R003 C030 J000 Y000 MP000000 020201			READ IOP
1 SWN	33 PTN	4 A000000 X000000 T177776 M020203 0177777 R003 C030 J000 Y000 MP000000 020203			READ IOP
1 SWN	34 PTN	5 A000000 X000000 T177776 M020221 0177777 R003 C030 J000 Y000 MP000000 020221			READ IOP
1 SWN	35 PTN	6 A000000 X000000 T177776 M020241 0177777 R003 C030 J000 Y000 MP000000 020241			READ IOP
1 SWN	40 PRN	6 M-3,250A0 V	STA 000100	P HOLD LOG DELAY for 2000	
1 SWN	40 PRN	7 M-3,250A0 V	STA 000100	P RESET LOG DELAY TO 10	
1 SWN	50 PTN	1 A000000 X000000 T000000 M020263 0177777 R003 C004 J000 Y000 MP000000 020263			CLEAR
1 SWN	51 PTN	7 A000000 X000000 T000001 M020263 0177777 R003 C010 J000 Y000 MP000000 020262			WRITE R0
1 SWN	52 PTN	8 A000000 X000000 T000001 M020263 0177777 R003 C015 J000 Y000 MP000000 020263			READ IOP
1 SWN	53 PTN	9 A000000 X000000 T000001 M020263 0177777 R003 C015 J000 Y000 MP000000 020262			READ IOP
1 SWN	54 PTN	10 A000000 X000000 T000001 M020263 0177777 R003 C015 J000 Y000 MP000000 020262			READ IOP
1 SWN	55 PTN	11 A000000 X000000 T000001 M020263 0177777 R003 C015 J000 Y000 MP000000 020262			READ IOP

FIGURE 3.39

## SUMMARY TABLE

TITLE: VTP010UA

Lot 3714 WF 5

SAMPLE COUNT: 00029

NUMBER CELLS: 00011

CELL LOWER CELL

NO.	BOUNDARY	FREQUENCY	RELATIVE FREQUENCY	CUMULATIVE REL. FREQ.
01	-3.99951 V	00000	0.000	0.000
02	-3.79951 V	00000	0.000	0.000
03	-3.59950 V	00000	0.000	0.000
04	-3.39950 V	00000	0.000	0.000
05	-3.19950 V	00000	0.000	0.000
06	-2.99951 V	00002	0.069	0.069
07	-2.79951 V	00004	0.138	0.207
08	-2.59950 V	00011	0.379	0.586
09	-2.39950 V	00010	0.345	0.931
10	-2.19950 V	00001	0.034	0.965
11	-1.99951 V	00001	0.034	0.999

-1.79951

MODE: -2.59950

MEAN: -2.55101

MEDIAN: -2.69950

VARIANCE: 0.04550

STANDARD DEVIATION: 0.21095

NO. VALUES BELOW RANGE: 000

NO. VALUES ABOVE RANGE: 002

## FREQUENCY HISTOGRAM

TITLE: VTP010UA

CELL LOWER	0	0010	0020	0030	0040	0050	0060
NO. BOUND	+	+	+	+	+	+	+
01-3.99951	.						
02-3.79951	.						
03-3.59950	.						
04-3.39950	.						
05-3.19950	.						
06-2.99951	.XX						
07-2.79951	.XXXX						
08-2.59950	.XXXXXXXXXXXX						
09-2.39950	.XXXXXXXXXXXX						
10-2.19950	.X						
11-1.99951	.X						
-1.79951							

FIGURE 3.40

MT and MT terminals to the differential input of an oscilloscope. A typical waveform for 256 memory windows (one I/O section) is shown in figure 3.41. The magnitude of windows was measured as a function of time for both endurance stressed and unstressed memory cells to give a very accurate prediction of long term array retention. While this method of obtaining window measurements was quite adequate, it was very time consuming to make for a large number of addressed memory cells of each array.

- Notes: 1. Single Write Cycle,  $t_w = 100 \mu s$   
 2. Nominal Supply Voltages  
 3. Test Enable Mode (TE = +12)  
 4. Checkerboard Pattern  
 5. Read Delay = 30 Sec

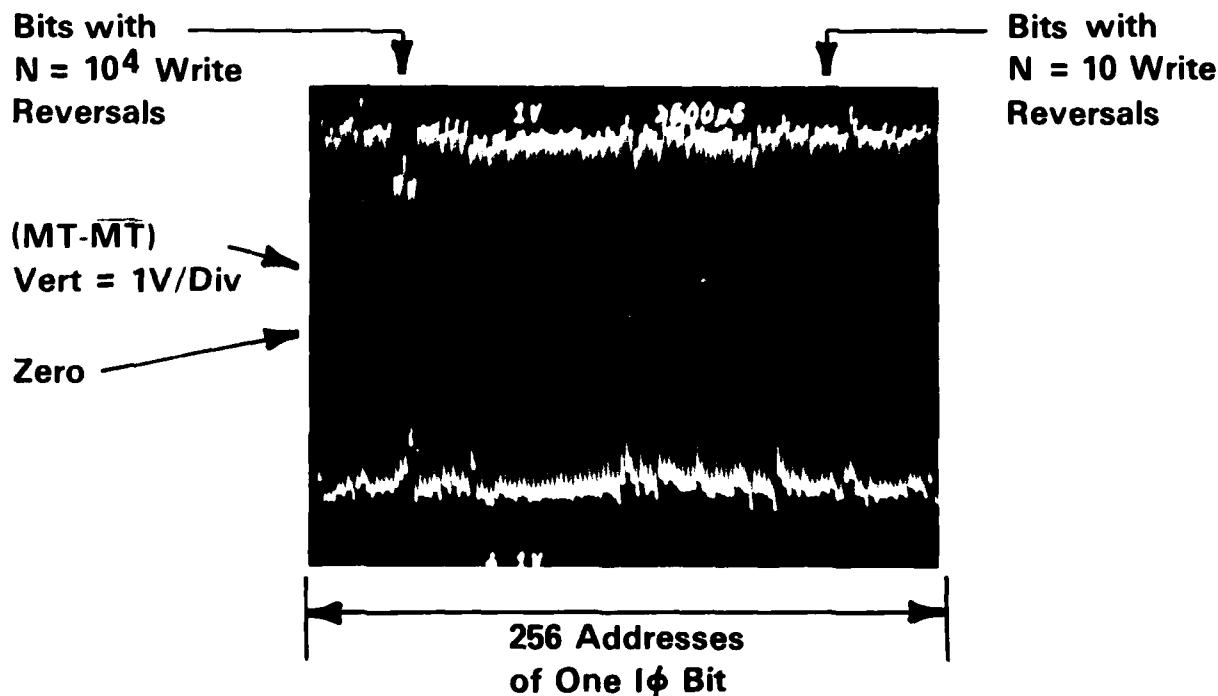
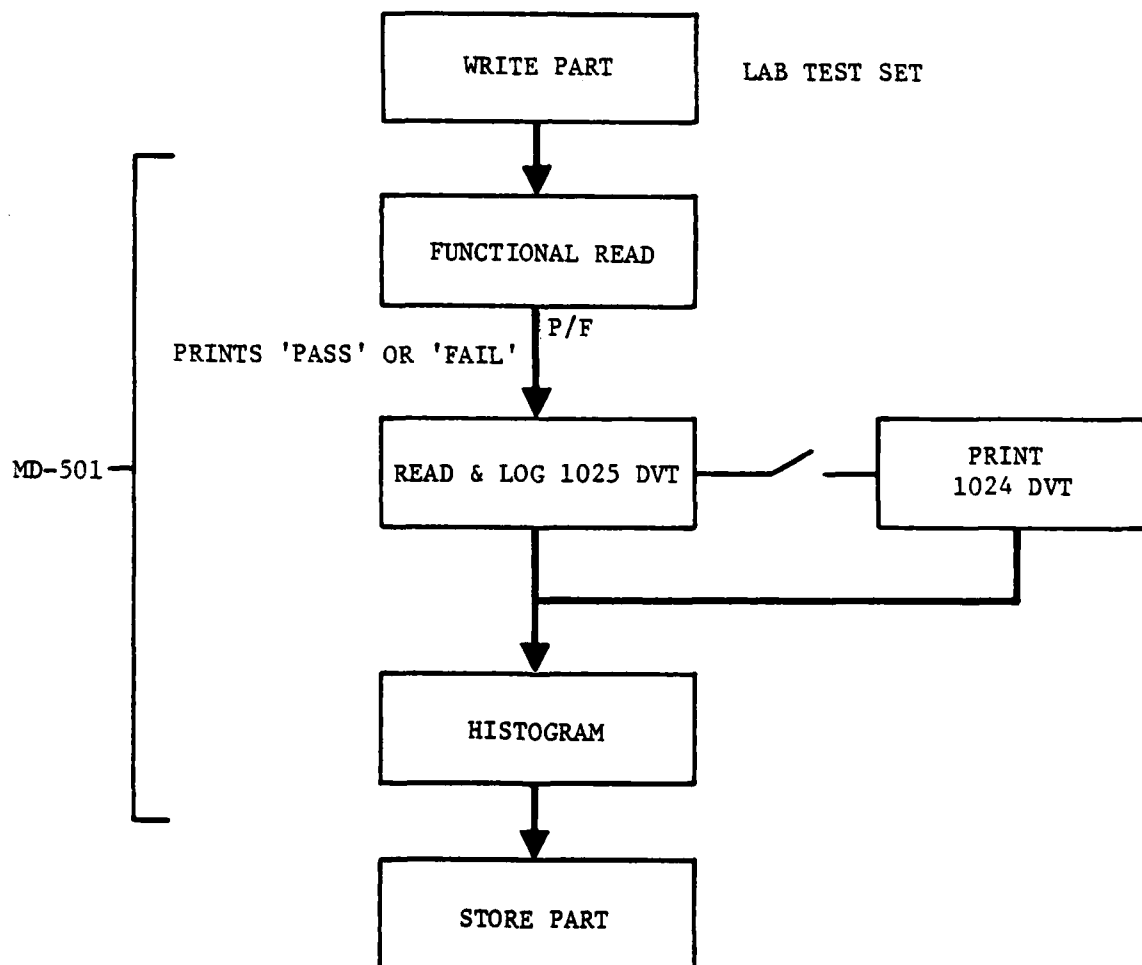


FIGURE 3.41 6013 PSM - MEASUREMENT OF MEMORY WINDOW

## 3.1.7.5.2 MD-501 Test Program

In order to increase the statistical sample of memory window measurements made and decrease the amount of test time required, a test program was generated on the MD-501 to automatically measure the 256 memory windows of each I/O section (1024 total) for a packaged PSM. Details of this program are given in the flow diagram shown in figure 3.42.

In this test a functional read is first performed to insure that the proper data pattern is stored. Then 1024 memory window measurements are made. By a front panel switch control, this data may be printed out as a true geographical map of memory windows as shown in figure 3.43. From this printout one can determine if there are any write level sensitivities within the array.



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FIGURE 3.42 6023/6013 MEMORY WINDOW TEST FLOW DIAGRAM



The 1024 memory windows may also be shown in frequency histogram form. A frequency histogram table for 1024 memory windows obtained using this program is shown in figure 3.44. This data may also be plotted as a frequency histogram.

SAMPLE COUNT: 1021  
NUMBER OF CELLS: 32  
VARIABLE: BRVO

CELL NO	LOWER CELL BOUNDARY	FREQUENCY	RELATIVE FREQUENCY	CUMULATIVE REL. FREQ.
0	0	0	0	0
1	.2	0	0	0
2	.4	0	0	0
3	.6	0	0	0
4	.8	0	0	0
5	1	0	0	0
6	1.2	0	0	0
7	1.4	0	0	0
8	1.6	0	0	0
9	1.8	2	.2E-02	.2E-02
10	2	14	.14E-01	.16E-01
11	2.2	25	.240001E-01	.4E-01
12	2.4	24	.240001E-01	.640001E-01
13	2.6	93	.920001E-01	.116
14	2.8	77	.75E-01	.191
15	3	152	.149	.34
16	3.2	191	.197	.527
17	3.4	247	.242	.769
18	3.6	280	.196	.965
19	3.8	30	.290001E-01	.994001
20	4	4	.400001E-02	.998001
21	4.2	2	.2E-02	1.
22	4.4	0	0	1.
23	4.6	0	0	1.
24	4.8	0	0	1.
25	5	0	0	1.
26	5.2	0	0	1.
27	5.4	0	0	1.
28	5.6	0	0	1.
29	5.8	0	0	1.

MODE: 2.3 3.5  
MEAN: 3.29346  
MEDIAN: 3.3  
VARIANCE: .154083  
STANDARD DEVIATION: .392536  
COEFFICIENT OF SKEWNESS: -.852176  
NO. OF DATA VALUES BELOW RANGE: 0  
NO. OF DATA VALUES ABOVE RANGE: 3

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FROM THE QUALITY CONTROL DEPARTMENT

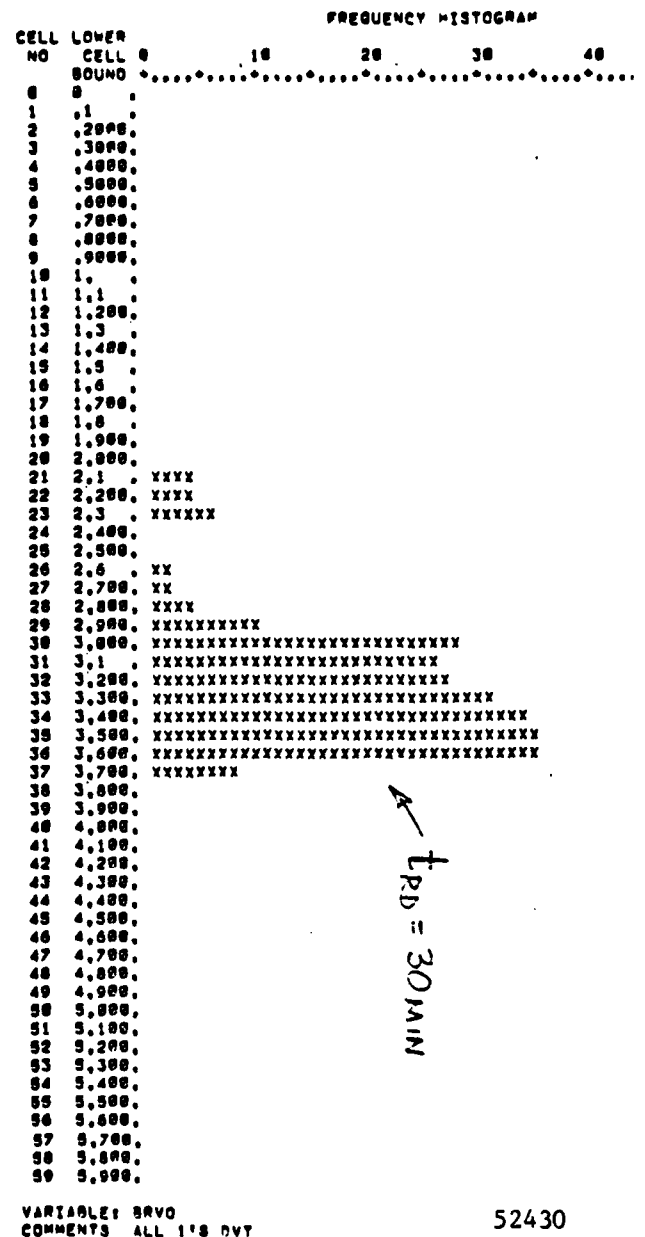
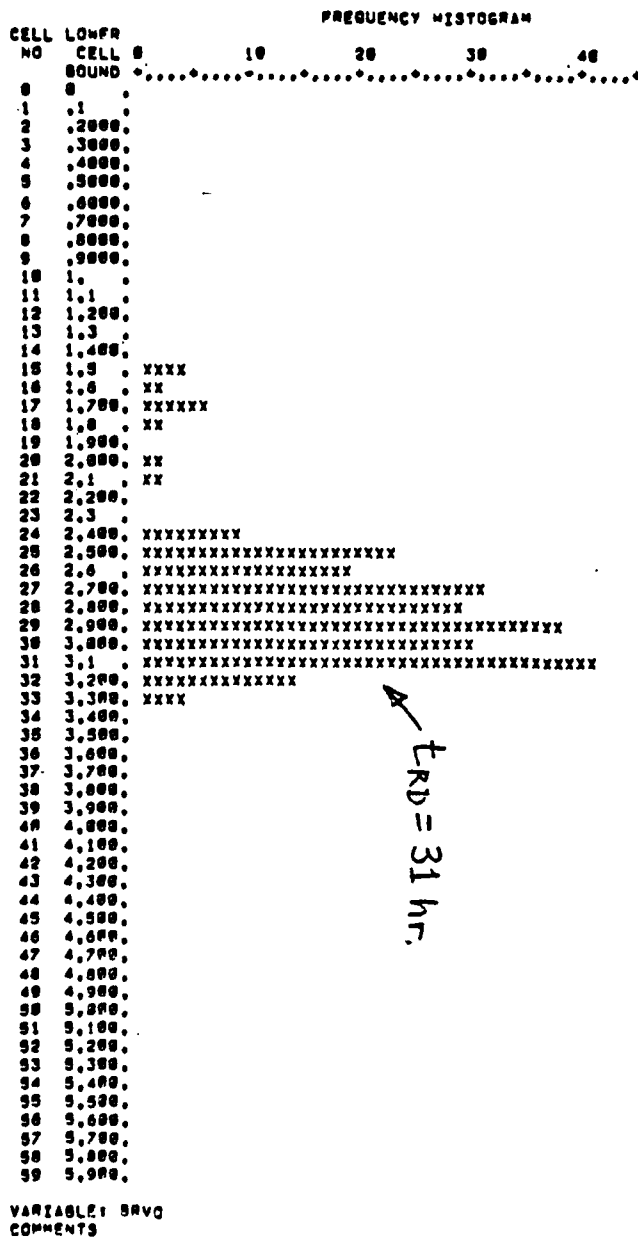
Figure 3.44 MD-501 PSM Memory Window Histogram Table

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Retention measurements may also be made by obtaining an initial histogram of memory windows and then obtaining additional histograms at later points in time. Figure 3.45 shows this type of measurement for 256 memory windows. The initial data was taken 30 minutes after writing while the second histogram was obtained 31 hours later. From this data, distribution and window magnitude as a function of time may be determined, to provide an accurate prediction of array retention.

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FIGURE 3.45 DI100 MEMORY WINDOW HISTOGRAM (256 BITS VS TIME)

## 3.1.7.6 PSM Testing Capability Summary

Using sophisticated state of the art automated test equipment the PSM LSIC can be thoroughly tested and characterized in a cost effective manner both at the wafer and package level.

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27. 24 P I CP  
PT+ = 001 101

tacc

1 SWN 25 PTN 0 A000102 X000000 T177777 M000200 B000000  
R001 C015 J077 Y000 MP000010 000263

CKB-READ I103

28. 26 P I CP  
PD- = 001 173

tacc

1 SWN 26 PTN 1 A000000 X000000 T000000 M000263 B177777  
R002 C024 J000 Y000 MP000010 000263

CKB-CLEAR

1 SWN 27 PTN 4 A000000 X000000 T177777 M000200 B000000  
R003 C012 J000 Y000 MP000010 000263

CKB-WRITE

1 SWN 28 PTN 0 A000102 X000000 T177777 M000200 B000000  
R001 C015 J077 Y000 MP000010 000263

CKB-READ I104

29. 29 P I CP  
PT- = 001 029

tacc

1 SWN 29 PTN 0 A000102 X000000 T177777 M000200 B000000  
R001 C015 J077 Y000 MP000010 000263

CKB-READ I101

30. 29 P I CP  
PD- = 001 110

tacc

1 SWN 30 PTN 0 A000102 X000000 T177777 M000200 B000000  
R001 C015 J077 Y000 MP000010 000263

CKB-READ I102

31. 30 P I CP  
PD- = 001 098

tacc

1 SWN 31 PTN 0 A000102 X000000 T177777 M000200 B000000  
R001 C015 J077 Y000 MP000010 000263

CKB-READ I103

32. 31 P I CP  
PT+ = 001 155

tacc

1 SWN 5 PTN 1 A000000 X000000 T000000 M000263 B177777  
R002 C024 J000 Y000 MP000010 000263

RID-CLEAR

1 SWN 6 PTN 2 A000000 X000000 T000001 M000263 B177777  
R003 C004 J000 Y000 MP000010 000262

RID-WRITE

1 SWN 7 PTN 3 A000000 X000000 T000001 M000263 B177777  
R003 C004 J000 Y000 MP000010 000263

RID-READ

1 SWN 8 PTN 1 A000000 X000000 T000000 M000263 B177777  
R002 C024 J000 Y000 MP000010 000263

CKB-CLEAR

1 SWN 9 PTN 4 A000000 X000000 T177777 M000200 B000000  
R002 C012 J000 Y000 MP000010 000263

CKB-WRITE

1 SWN 10 PTN 5 A000000 X000000 T177777 M000263 B000000  
R002 C012 J000 Y000 MP000010 000263

CKB-READ

1 SWN 11 PTN 1 A000000 X000000 T000000 M000263 B177777  
R001 C024 J000 Y000 MP000010 000263

CKB-CLEAR

1 SWN 12 PTN 6 A000000 X000000 T000000 M000263 B177777  
R002 C012 J000 Y000 MP000010 000200

CKB-WRITE

1 SWN 13 PTN 7 A000000 X000000 T000000 M000263 B177777  
R002 C012 J000 Y000 MP000010 000262

CKB-READ

Post RAD.TIM  
W/O DR  
NOM. PWR.  
INC. ADD

Loose Tim.  
W/O DR  
NOM. PWR.  
INC. ADD

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1 SUN 22 PTN 1 A000000 T000000 M000263 B177777 CKB-CLEAR  
R002 C024 J000 Y000 MP000010 000263

1 SUN 23 PTN 4 A000000 X000000 T177777 M000200 0000000 CKB--WRITE  
R002 C012 J000 Y000 MP000010 000263

1 SUN 24 PTN 0 A000102 M000000 T177777 M000200 0000000 CKB-READ I/O 1  
R001 C015 J077 Y000 MP000010 000263

EST 24 P I OP  
E2+ = 001 068 tacc

1 SUN 25 PTN 0 A000102 X000000 T177777 M000200 0000000 CKB-READ I/O 1  
R001 C015 J077 Y000 MP000010 000263

EST 25 P I OP  
E2+ = 001 076 tacc

1 SUN 26 PTN 0 A000102 X000000 T177777 M000200 0000000 CKB-READ I/O 2  
R001 C015 J077 Y000 MP000010 000263

EST 26 P I OP  
E2+ = 001 067 tacc

1 SUN 27 PTN 0 A000102 X000000 T177777 M000200 0000000 CKB-READ I/O 3  
R001 C015 J077 Y000 MP000010 000263

EST 27 P I OP  
E2+ = 001 104 tacc

1 SUN 28 PTN 1 A000000 X000000 T000000 M000263 B177777 CKB-CLEAR  
R002 C024 J000 Y000 MP000010 000263

1 SUN 29 PTN 4 A000000 X000000 T177777 M000200 0000000 CKB-WRITE  
R002 C012 J000 Y000 MP000010 000263

1 SUN 40 PTN 0 A000102 X000000 T177777 M000200 0000000 CKB-READ I/O 1  
R001 C015 J077 Y000 MP000010 000263

EST 40 P I OP  
E2+ = 001 144 tacc

1 SUN 41 PTN 0 A000102 X000000 T177777 M000200 0000000 CKB-READ I/O 1  
R001 C015 J077 Y000 MP000010 000263

EST 41 P I OP  
E2+ = 001 159 tacc

1 SUN 42 PTN 0 A000102 X000000 T177777 M000200 0000000 CKB-READ I/O 2  
R001 C015 J077 Y000 MP000010 000263

EST 42 P I OP  
E2+ = 001 173 tacc

1 SUN 43 PTN 0 A000102 X000000 T177777 M000200 0000000 CKB-READ I/O 3  
R001 C015 J077 Y000 MP000010 000263

EST 43 P I OP  
E2+ = 001 420 tacc

1 SUN 44 PTN 1 A000000 X000000 T000000 M000263 B177777 CKB-CLEAR  
R002 C024 J000 Y000 MP000010 000263

1 SUN 45 PTN 6 A000000 X000000 T000000 M000263 B177777 CKB-WRITE  
R002 C012 J000 Y000 MP000010 000200

Post RADTIM  
W DR  
MAX. PWR.  
INC. ADD.

Post RADTIM  
W DR  
MIN. PWR.  
INC. ADD.

1 SWN 45 PTN 0 A0000000 1177777 M000200 8000000  
R001 C013 J077 Y000 MP000010 000263

CK3-READ I/O 0

ESN 45 P I OP  
PD- = 001 073

tacc

1 SWN 47 PTN 0 A0000000 1177777 M000200 8000000  
R001 C013 J077 Y000 MP000010 000263

CK3-READ I/O 1

ESN 47 P I OP  
PD- = 001 091

tacc

1 SWN 49 PTN 0 A0000000 1177777 M000200 8000000  
R001 C013 J077 Y000 MP000010 000263

CK3-READ I/O 2

ESN 49 P I OP  
PD- = 001 091

tacc

1 SWN 49 PTN 0 A0000000 1177777 M000200 8000000  
R001 C013 J077 Y000 MP000010 000263

CK3-READ I/O 3

ESN 49 P I OP  
PD- = 001 126

tacc

1 SWN 50 PTN 1 A0000000 1000000 T000000 M000000 B177777  
R001 C024 J000 Y000 MP000010 000263

CK3-CLEAR

1 SWN 51 PTN 6 A000000 1000000 T000000 M000000 B177777  
R001 C012 J000 Y000 MP000010 000200

CK3-WRITE

1 SWN 52 PTN 0 A000000 1177777 M000200 8000000  
R001 C013 J077 Y000 MP000010 000263

CK3-READ I/O 0

ESN 52 P I OP  
PD- = 001 167

tacc

1 SWN 53 PTN 0 A000000 1177777 M000200 8000000  
R001 C013 J077 Y000 MP000010 000263

CK3-READ I/O 1

ESN 53 P I OP  
PD- = 001 180

tacc

1 SWN 54 PTN 0 A000000 1177777 M000200 8000000  
R001 C013 J077 Y000 MP000010 000263

CK3-READ I/O 2

ESN 54 P I OP  
PD- = 001 173

tacc

1 SWN 55 PTN 0 A000000 1177777 M000200 8000000  
R001 C013 J077 Y000 MP000010 000263

CK3-READ I/O 3

ESN 55 P I OP  
PD- = 001 423

tacc

1 SWN 172 PRN 52 M-2 0-2	UA	STA 000100	P	IOL (HIGH Z)	I/O 0
1 SWN 173 PRN 53 M-3 0-3	UA	STA 000100	P	"	I/O 1
1 SWN 174 PRN 54 M-3 0-3	UA	STA 000100	P	"	I/O 2
1 SWN 175 PRN 55 M-3 0-3	UA	STA 000100	P	"	I/O 3
1 SWN 176 PRN 56 M-2 5-2	UA	STA 000100	P	IOL (HIGH Z)	I/O 0
1 SWN 177 PRN 57 M-1 5-2	UA	STA 000100	P		I/O 1

Post Rad Tim  
W DR  
Max, PWR.  
INC. ADD

Post Rad. Tim  
W DR  
Min, PWR  
INC. ADD

1 SWN 178 PRN 59 M1 51-2 UA STA 000100 P IOL (HIGH Z) IIO 2  
 1 SWN 179 PRN 59 M1 51-2 UA STA 000100 P " IIO 3  
 1 SWN 180 PTN 1 A000000 X000000 T000000 M000263 B177777 "0's" - CLEAR  
 R003 C024 J000 Y000 MF000010 000263  
 1 SWN 181 PTN 35 A000000 X000000 T000000 M000263 B000000 "0's" - WRITE  
 R003 C012 J000 Y000 MF000010 000263  
 1 SWN 182 PTN 14 A000000 X000000 T000000 M000263 B177777 "0's" - READ  
 R003 C050 J000 Y000 MF000010 000263  
 1 SWN 183 PRN 60 M1 021571 V STA 000100 F 0 Vol @ IOL = 0 IIO 0  
 1 SWN 184 PRN 61 M1 021571 V STA 000100 P " IIO 1  
 1 SWN 185 PRN 62 M1 021571 V STA 000100 P " IIO 2  
 1 SWN 186 PRN 63 M1 021571 V STA 000100 P " IIO 3  
 1 SWN 187 PTN 24 A000000 X000000 T000000 M000263 B177777 "0's" - READ  
 R003 C050 J000 Y000 MF000010 000263  
 1 SWN 188 PRN 64 M1 021571 V STA 000100 F 0 Vol @ IOL = 1 mA IIO 0  
 1 SWN 189 PRN 65 M1 021571 V STA 000100 P " IIO 1  
 1 SWN 190 PRN 66 M1 021571 V STA 000100 P " IIO 2  
 1 SWN 191 PRN 67 M1 021571 V STA 000100 P " IIO 3  
 1 SWN 192 PTN 24 A000000 X000000 T000000 M000263 B177777 "0's" - READ  
 R003 C050 J000 Y000 MF000010 000263  
 1 SWN 193 PRN 68 M1 021571 UA STA 000100 P IOL IIO 0  
 1 SWN 194 PRN 69 M1 021571 UA STA 000100 P " IIO 1  
 1 SWN 195 PRN 70 M1 021571 UA STA 000100 P " IIO 2  
 1 SWN 196 PRN 71 M1 021571 UA STA 000100 P " IIO 3  
 1 SWN 197 PTN 1 A000000 X000000 T000000 M000263 B177777 "1's" - CLEAR  
 R003 C024 J000 Y000 MF000010 000263  
 1 SWN 198 PTN 37 A000000 X000000 T177777 M000263 B177777 "1's" - WRITE  
 R003 C012 J000 Y000 MF000010 000263  
 1 SWN 199 PTN 25 A000000 X000000 T177777 M000263 B177777 "1's" - READ  
 R003 C070 J000 Y000 MF000010 000263  
 1 SWN 200 PRN 72 M1 09071 V STA 000100 P Vol @ IOH = 0 IIO 0  
 1 SWN 201 PRN 73 M1 09071 V STA 000100 P " IIO 1  
 1 SWN 202 PRN 74 M1 09071 V STA 000100 P " IIO 2  
 1 SWN 203 PRN 75 M1 09071 V STA 000100 P " IIO 3  
 1 SWN 204 PTN 23 A000000 X000000 T177777 M000263 B177777 "1's" - READ  
 R003 C070 J000 Y000 MF000010 000263  
 1 SWN 205 PRN 76 M1 09071 V STA 000100 P Vol @ IOH = 1 mA IIO 0  
 1 SWN 206 PRN 77 M1 09071 V STA 000100 P " IIO 1

1 SW 207 PRN 73 M1 05071 V STA 000100 P VOH @ I<sub>OH</sub> = 1mA I102  
 1 SW 208 PRN 79 M1 05071 V STA 000100 P " I103  
 1 SW 209 PTN 25 A000001 M000000 T177777 M000263 B177777 \* 1's - READ  
 P002 0070 1000 Y000 M0000010 M00263  
 1 SW 210 PRN 80 M2 57574 UA STA 000100 P I<sub>SCH</sub>. I104  
 1 SW 211 PRN 81 M2 57574 UA STA 000100 P " I101  
 1 SW 212 PRN 82 M2 57574 UA STA 000100 P " I102  
 1 SW 213 PRN 83 M1 57574 UA STA 000100 P " I103  
 1 SW 120 PRN 2 M3 7-2 UA STA 000100 P I<sub>IH</sub> (VDD)  
 1 SW 123 PRN 3 M5 7-2 UA STA 000100 P I<sub>IH</sub> (VNN)  
 1 SW 124 PRN 4 M5 7-2 UA STA 000100 P I<sub>IL</sub> (VSS)  
 1 SW 121 PRN 93 M5 7-3 UA STA 000100 P I<sub>IL</sub> (Vpp)  
 1 SW 125 PRN 5 M1 39570 V STA 000100 P VI<sub>PH</sub> @ 3mA  
 1 SW 126 PRN 6 M-2 39570 V STA 000100 P VI<sub>PL</sub> @ 3mA  
 1 SW 127 PRN 7 M-3 78570 UA STA 000100 P I<sub>DS</sub> - STEY  
 1 SW 128 PRN 8 M5 UA STA 000100 P I<sub>SS</sub> - "  
 1 SW 129 PRN 9 M1 53572 UA STA 000100 P I<sub>NN</sub> - "  
 1 SW 130 PRN 10 M3 70 UA STA 000100 P I<sub>PP</sub> - "  
 1 SW 131 PRN 11 M0 UA STA 000100 P I<sub>MWS</sub> - "  
 1 SW 132 PRN 12 M-4 4070 UA STA 000100 P I<sub>SD</sub> - CLEAR PRE CHARGE  
 1 SW 133 PRN 13 M0 UA STA 000100 P I<sub>SS</sub> - "  
 1 SW 134 PRN 14 M5 570 UA STA 000100 P I<sub>NN</sub> - "  
 1 SW 135 PRN 15 M5 71 UA STA 000100 P I<sub>PP</sub> - "  
 1 SW 136 PRN 16 M4 1570 UA STA 000100 P I<sub>MWS</sub> - "  
 1 SW 137 PRN 17 M-4 1070 UA STA 000100 P I<sub>DS</sub> - "  
 1 SW 138 PRN 18 M0 UA STA 000100 P I<sub>SS</sub> - "  
 1 SW 139 PRN 19 M5 070 UA STA 000100 P I<sub>NN</sub> - "  
 1 SW 140 PRN 20 M5 71 UA STA 000100 P I<sub>PP</sub> - "  
 1 SW 141 PRN 21 M0 9570 UA STA 000100 P I<sub>MWS</sub> - "  
 1 SW 152 PRN 32 M-3 6070 UA STA 000100 P I<sub>DD</sub> - WRITE  
 1 SW 153 PRN 33 M0 UA STA 000100 P I<sub>SS</sub> - "  
 1 SW 154 PRN 34 M5 570 UA STA 000100 P I<sub>NN</sub> - "  
 1 SW 155 PRN 35 M4 5070 UA STA 000100 P I<sub>PP</sub> - "

DIFF. ADD.

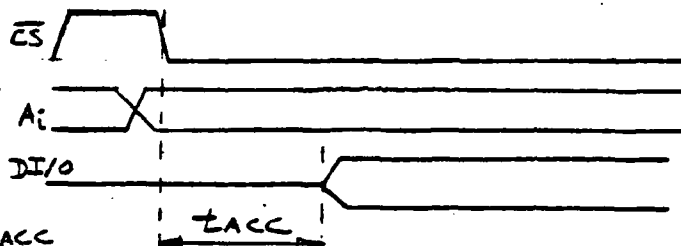
1 SWN 157 PPN 36 M-1 13974	UA	STA 000100	P	IMWS - WRITE	
1 SWN 157 PPN 37 M-1 13974	UA	STA 000100	P	IDD - "	} DIFF. ADD.
1 SWN 158 PPN 38 M0.	UA	STA 000100	P	ISS - "	
1 SWN 159 PPN 39 M1 8070	UA	STA 000100	P	INN - "	
1 SWN 160 PPN 40 M4 1070	UA	STA 000100	P	IPP - "	
1 SWN 161 PPN 41 M4 5570	UA	STA 000100	P	IMWS - "	
1 SWN 162 PPN 42 M-1 14574	UA	STA 000100	P	IDD - READ	
1 SWN 163 PPN 43 M0	UA	STA 000100	P	ISS - "	
1 SWN 164 PPN 44 M0 1070	UA	STA 000100	P	INN - "	
1 SWN 165 PPN 45 M0 8070	UA	STA 000100	P	IPP - "	
1 SWN 166 PPN 46 M1 5070	UA	STA 000100	P	IMWS - "	
1 SWN 167 PPN 47 M-1 13974	UA	STA 000100	P	IDD - "	} DIFF. ADD.
1 SWN 168 PPN 48 M0	UA	STA 000100	P	ISS - "	
1 SWN 169 PPN 49 M1 01574	UA	STA 000100	P	INN - "	
1 SWN 170 PPN 50 M1 5070	UA	STA 000100	P	IPP - "	
1 SWN 171 PPN 51 M1 7570	UA	STA 000100	P	IMWS - "	
1 SWN 214 PPN 84 M0 7-3	UA	STA 000100	P	ILP	
1 SWN 215 PPN 85 M1 257-1	UA	STA 000100	P	ILN	
1 SWN 216 PPN 86 M-2 8070	V	STA 000100	P	VTP	
1 SWN 219 PPN 89 M4 8070	UA	STA 000100	P	ISSN @ Vgs=0	
1 SWN 220 PPN 90 M0 7-1	UA	STA 000100	P	ISSN @ Vgs=-2	
1 SWN 221 PPN 91 M0 7-1	UA	STA 000100	P	ISSN @ Vgs=-4	
1 SWN 222 PPN 92 M0 7-2	UA	STA 000100	P	ISSN @ Vgs=6	
1 SWN 223 PPN 93 M0 57-2	UA	STA 000100	P	ILN	
1 SWN 94 PTN 1	A000000 0000000 1000001 M000263 8177777			RID - CLEAR	
	R000 0004 1000 0000 MP000010 000263				
1 SWN 95 PTN 2	A000000 0000000 1000001 M000263 8177777			RID - WRITE	
	R000 0004 1000 0000 MP000010 000262				
1 SWN 96 PTN 3	A000000 0000000 1000001 M000263 8177777			RID - READ	I/O 0
	R000 0004 1000 0000 MP000010 000263				
1 SWN 97 PTN 9	A000000 0000000 1000001 M000263 8177777			"	I/O 1
	R000 0004 1000 0000 MP000010 000262				
1 SWN 98 PTN 10	A000000 0000000 1000001 M000263 8177777			"	I/O 2
	R000 0004 1000 0000 MP000010 000262				
1 SWN 99 PTN 11	A000000 0000000 1000001 M000263 8177777			"	I/O 3
	R000 0004 1000 0000 MP000010 000262				

6013 ATL TAPE P3 REV 00 #3438 3/10/77 (R)  
 1 SWN 1 PRN 1 001 12370 V 5TH 000100 P CONTACT (LW2)

ESN 33 P I OP tacc  
 PT+ = 001 032 I/O 4  
 ESN 31 P I OP tacc  
 PT+ = 001 101 I/O 1  
 ESN 32 P I OP tacc  
 PT+ = 001 088 I/O 2  
 ESN 31 P I OP tacc  
 PT+ = 001 121 I/O 3

READ RID  
 W DR  
 NOM. PWR.  
 INC. ADD.

P3+8.05=tacc  
 ACTUAL



1 SWN 14 PTN 1 000000 000000 000000 0000262 8177777  
 0002 0024 0000 0000 MP000010 000263

RID - CLEAR

1 SWN 15 PTN 2 000000 000000 000001 0000263 8177777  
 0002 0004 0000 0000 MP000010 000262

RID - WRITE

1 SWN 15 PTN 3 0000264 000000 000001 0000262 8177777  
 0001 0005 0000 0000 MP000010 000263

RID - READ I/O 4

ESN 15 P I OP  
 PT+ = 001 032 tacc

1 SWN 17 PTN 0 0000262 000000 000000 0000261 8177777  
 0001 0005 0000 0000 MP000010 000263

RID - READ I/O 1

ESN 17 P I OP  
 PT+ = 001 101 tacc

1 SWN 13 PTN 0 000000 000000 000000 0000243 8177777  
 0001 0005 0000 0000 MP000010 000263

RID - READ I/O 2

ESN 13 P I OP  
 PT+ = 001 088 tacc

1 SWN 13 PTN 0 000000 000000 000000 0000223 8177777  
 0001 0005 0000 0000 MP000010 000263

RID - READ I/O 3

ESN 13 P I OP  
 PT+ = 001 123 tacc

1 SWN 20 PTN 1 000000 000000 000000 0000262 8177777  
 0002 0024 0000 0000 MP000010 000263

CKB - CLEAR

1 SWN 21 PTN 4 000000 000000 000000 0000200 8000000  
 0001 0012 0000 0000 MP000010 000263

CKB - WRITE

1 SWN 22 PTN 0 000000 000000 000000 0000200 8000000  
 0001 0013 0000 0000 MP000010 000263

CKB - READ I/O 4

ESN 22 P I OP  
 PT+ = 001 102 tacc

1 SWN 23 PTN 0 000000 000000 000000 0000200 8000000  
 0001 0015 0000 0000 MP000010 000263

CKB - READ I/O 1

ESN 23 P I OP  
 PT+ = 001 114 tacc

1 SWN 24 PTN 0 000000 000000 000000 0000200 8000000  
 0001 0015 0000 0000 MP000010 000263

CKB - READ I/O 2

Post RAD Tim  
 W DR  
 Nom. PWR.  
 INC. ADD.

Post RAD Tim  
 W DR  
 Nom. PWR.  
 INC. ADD.

TAPE: 6013/603 P3 REV 00  
 AT1

STN 14 - I OP  
PDA - 001 100

tacc

1 SWN 15 PTN 0 A000102 M000000 T177777 M000200 B000000 CKB-READ ID3  
P001 0013 J000 Y000 MF000010 000263

STN 15 - I OP  
PDA - 001 100

tacc

1 SWN 5 PTN 1 A000000 M000000 T000000 M000263 B177777 RID-CLEAR  
P002 0024 J000 Y000 MF000010 000263

1 SWN 6 PTN 2 A000000 M000000 T000001 M000263 B177777 RID-WRITE  
P003 0034 J000 Y000 MF000010 000262

1 SWN 7 PTN 3 A000000 M000000 T000001 M000263 B177777 RID-READ  
P004 0044 J000 Y000 MF000010 000263

1 SWN 8 PTN 1 A000000 M000000 T000000 M000263 B177777 CKB-CLEAR  
P001 0014 J000 Y000 MF000010 000263

1 SWN 9 PTN 4 A000000 M000000 T177777 M000200 B000000 CK3-WRITE  
P002 0012 J000 Y000 MF000010 000263

1 SWN 10 PTN 5 A000000 M000000 T177777 M000263 B000000 CK2-READ  
P003 0012 J000 Y000 MF000010 000263

1 SWN 11 PTN 1 A000000 M000000 T000000 M000263 B177777 CKB-CLEAR  
P001 0024 J000 Y000 MF000010 000263

1 SWN 12 PTN 6 A000000 M000000 T000000 M000263 B177777 CK3-WRITE  
P002 0012 J000 Y000 MF000010 000200

1 SWN 13 PTN 7 A000000 M000000 T000000 M000263 B177777 CK3-READ  
P003 0012 J000 Y000 MF000010 000263

1 SWN 172 PPN 52 M-2 57-2 UA STA 000100 P I<sub>OH</sub>(HIGH Z) I<sub>IO</sub>φ

1 SWN 173 PPN 53 M-5 7-2 UA STA 000100 P " I<sub>IO</sub>1

1 SWN 174 PPN 54 M-5 7-2 UA STA 000100 P " I<sub>IO</sub>2

1 SWN 175 PPN 55 M-5 7-2 UA STA 000100 P " I<sub>IO</sub>3

1 SWN 176 PPN 56 M1 67-2 UA STA 000100 P I<sub>OL</sub>(HIGH Z) I<sub>IO</sub>φ

1 SWN 177 PPN 57 M1 57-2 UA STA 000100 P " I<sub>IO</sub>1

1 SWN 178 PPN 58 M5 7-2 UA STA 000100 P " I<sub>IO</sub>2

1 SWN 179 PPN 59 M1 57-2 UA STA 000100 P " I<sub>IO</sub>3

1 SWN 180 PPN 1 A000000 M000000 T000000 M000263 B177777 "0's"-CLEAR  
P001 0012 J000 Y000 MF000010 000263

1 SWN 181 PPN 15 A000000 M000000 T000000 M000263 B000000 "0's"-WRITE  
P002 0012 J000 Y000 MF000010 000263

1 SWN 182 PPN 34 A000000 M000000 T000000 M000263 B177777 "0's"-READ  
P001 0012 J000 Y000 MF000010 000263

1 SWN 183 PPN 60 M1 000511 V STA 100100 F 0 Vol @ I<sub>OL</sub>=0 I<sub>IO</sub>φ

1 SWN 184 PPN 61 M0 V STA 000100 P " I<sub>IO</sub>1

SWN 185 PPN 62 M0 V STA 000100 P " I<sub>IO</sub>2

Loose Tim.  
w/o DR  
Nom. PWR.  
INC. 22.

1 STM 196 PRN 63 MD V STA 000100 P Vol @ IOL = 0 IIO 3

1 STM 197 PRN 24 4000000 0000000 1000000 M000263 B177777 "0's" - READ  
P002 0050 J000 Y000 M0000010 000263

1 STM 198 PRN 64 ML 001501 V STA 000100 F 0 Vol @ IOL = 1 mA IIO 0

1 STM 199 PRN 65 ML 550-1 V STA 000100 P " IIO 1

1 STM 200 PRN 66 ML 550-1 V STA 000100 P " IIO 2

1 STM 201 PRN 67 ML 550-1 V STA 000100 P " IIO 3

1 STM 202 PRN 24 4000000 0000000 1000000 M000263 B177777 "0's" - READ  
P002 0050 J000 Y000 M0000010 000263

1 STM 203 PRN 68 M-2 512 UR STA 000100 P Isc L IIO 0

1 STM 204 PRN 69 M-2 012 UR STA 000100 P " IIO 1

1 STM 205 PRN 70 M-2 550-4 UR STA 000100 P " IIO 2

1 STM 206 PRN 71 M-1 512 UR STA 000100 P " IIO 3

1 STM 197 PRN 1 4000000 0000000 1000000 M000263 B177777 "1's" - CLEAR  
P002 0024 J000 Y000 M0000010 000263

1 STM 198 PRN 37 4000000 0000000 1177777 M000263 B177777 "1's" - WRITE  
P002 0012 J000 Y000 M0000010 000263

1 STM 199 PRN 25 4000000 0000000 1177777 M000263 B177777 "1's" - READ  
P002 0070 J000 Y000 M0000010 000263

1 STM 200 PRN 72 ML 05501 V STA 000100 P Voh @ IOL = 0 IIO 0

1 STM 201 PRN 73 ML 05501 V STA 000100 P " IIO 1

1 STM 202 PRN 74 ML 05501 V STA 000100 P " IIO 2

1 STM 203 PRN 75 ML 05501 V STA 000100 P " IIO 3

1 STM 204 PRN 25 4000000 0000000 1177777 M000263 B177777 "1's" - READ  
P002 0070 J000 Y000 M0000010 000263

1 STM 205 PRN 76 ML 05501 V STA 000100 P Voh @ IOL = 1 mA IIO 0

1 STM 206 PRN 77 ML 05501 V STA 000100 P " IIO 1

1 STM 207 PRN 78 ML 05501 V STA 000100 P " IIO 2

1 STM 208 PRN 79 ML 05501 V STA 000100 P " IIO 3

1 STM 209 PRN 25 4000000 0000000 1177777 M000263 B177777 "1's" - READ  
P002 0070 J000 Y000 M0000010 000263

1 STM 210 PRN 80 ML 550-4 UR STA 000100 P Isc H IIO 0

1 STM 211 PRN 81 ML 550-4 UR STA 000100 P " IIO 1

1 STM 212 PRN 82 ML 550-4 UR STA 000100 P " IIO 2

1 STM 213 PRN 83 ML 550-4 UR STA 000100 P " IIO 3

1 STM 214 PRN 2 MD UR STA 000100 P ITH (VDD)

1	EN	121	PRN	2	M5	0-2	UA	STA	000100	P	I <sub>IH</sub> (V <sub>NN</sub> )	
1	EN	124	PRN	4	M5	0-2	UA	STA	000100	P	I <sub>IL</sub> (V <sub>SS</sub> )	
1	EN	121	PRN	93	M5	0-2	UA	STA	000100	P	I <sub>IL</sub> (V <sub>PP</sub> )	
1	EN	125	PRN	5	M2	08570	V	STA	000100	P	V <sub>IPH</sub> @ 3mA	
1	EN	125	PRN	5	M2	08570	V	STA	000100	P	V <sub>IPL</sub> @ 3mA	
1	EN	127	PRN	7	M2	65503	UA	STA	000100	P	I <sub>DD</sub> - STBY	
1	EN	128	PRN	8	M0		UA	STA	000100	P	I <sub>SS</sub> - "	
1	EN	129	PRN	9	M1	67573	UA	STA	000100	P	I <sub>NN</sub> - "	
1	EN	130	PRN	10	M2	071	UA	STA	000100	P	I <sub>PP</sub> - "	
1	EN	131	PRN	11	M0		UA	STA	000100	P	I <sub>MWS</sub> - "	
1	EN	132	PRN	12	M4	4073	UA	STA	000100	P	I <sub>DD</sub> - CLEAR PRE CHARGE	
1	EN	133	PRN	13	M0		UA	STA	000100	P	I <sub>SS</sub> - "	
1	EN	134	PRN	14	M5	072	UA	STA	000100	P	I <sub>NN</sub> - "	
1	EN	135	PRN	15	M1	072	UA	STA	000100	P	I <sub>PP</sub> - "	
1	EN	136	PRN	16	M4	1073	UA	STA	000100	P	I <sub>MWS</sub> - "	
1	EN	137	PRN	17	M4	08573	UA	STA	000100	P	I <sub>DD</sub> - "	
1	EN	138	PRN	18	M0		UA	STA	000100	P	I <sub>SS</sub> - "	
1	EN	139	PRN	19	M4	572	UA	STA	000100	P	I <sub>NN</sub> - "	
1	EN	140	PRN	20	M1	072	UA	STA	000100	P	I <sub>PP</sub> - "	
1	EN	141	PRN	21	M2	5073	UA	STA	000100	P	I <sub>MWS</sub> - "	
1	EN	142	PRN	22	M2	5073	UA	STA	000100	P	I <sub>DD</sub> - WRITE	
1	EN	153	PRN	33	M0		UA	STA	000100	P	I <sub>SS</sub> - "	
1	EN	154	PRN	34	M2	572	UA	STA	000100	P	I <sub>NN</sub> - "	
1	EN	155	PRN	35	M4	5573	UA	STA	000100	P	I <sub>PP</sub> - "	
1	EN	156	PRN	36	M2	9573	UA	STA	000100	P	I <sub>MWS</sub> - "	
1	EN	157	PRN	37	M1	17574	UA	STA	000100	P	I <sub>DD</sub> - "	
1	EN	158	PRN	38	M0		UA	STA	000100	P	I <sub>SS</sub> - "	
1	EN	159	PRN	39	M1	5073	UA	STA	000100	P	I <sub>NN</sub> - "	
1	EN	160	PRN	40	M4	2073	UA	STA	000100	P	I <sub>PP</sub> - "	
1	EN	161	PRN	41	M4	5073	UA	STA	000100	P	I <sub>MWS</sub> - "	
1	EN	162	PRN	42	M1	17574	UA	STA	000100	P	I <sub>DD</sub> - READ	
1	EN	163	PRN	43	M0		UA	STA	000100	P	I <sub>SS</sub> - "	
1	EN	164	PRN	44	M4	0073	UA	STA	000100	P	I <sub>NN</sub> - "	

} DIFF. ADD.

} DIFF. ADD

1	STN 165	PPN 45	ML 0073	UA	STA 000100	P	IPP - READ	
1	STN 166	PPN 46	ML 5573	UA	STA 000100	P	IMW3 - //	
1	STN 167	PPN 47	M-1 38074	UA	STA 000100	P	IDD - "	} DIFF. ADD.
1	STN 168	PPN 48	ML	UA	STA 000100	P	ISS - "	
1	STN 169	PPN 49	ML 01574	UA	STA 000100	P	INN - "	
1	STN 170	PPN 50	ML 3073	UA	STA 000100	P	IPP - "	
1	STN 171	PPN 51	ML 7073	UA	STA 000100	P	IMW3 - "	
1	STN 214	PPN 54	ML 57-2	UA	STA 000100	P	ILP	} TEST DEVICE CHAR.
1	STN 215	PPN 55	MS 57-2	UA	STA 000100	P	ILN	
1	STN 216	PPN 56	M-2 0070	V	STA 000100	P	VTP	
1	STN 217	PPN 57	ML 0072	UA	STA 000100	P	IDSN @ VGS=0	
1	STN 220	PPN 59	MS 7-1	UA	STA 000100	P	IDSN @ VGS=-2	
1	STN 221	PPN 91	MS 7-1	UA	STA 000100	P	IDSN @ VGS=-4	
1	STN 222	PPN 92	MS 7-2	UA	STA 000100	P	IDSN @ VGS=-6	
1	STN 223	PPN 93	MS 57-2	UA	STA 000100	P	ILN	
1	STN 24	PTN 1	A000000 X000000 T000000 M000263 B177777				RID - CLEAR	
			P003 0004 J000 Y000 M0000010 000263					
1	STN 25	PTN 2	A000000 X000000 T000001 M000263 B177777				RID - WRITE	
			P002 0004 J000 Y000 M0000010 000262					
1	STN 26	PTN 3	A000000 X000000 T000001 M000263 B177777				RID - READ	
			P003 0004 J000 Y000 M0000010 000263					

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### 3.1.8 PSM LSIC Fabrication and Wafer Test

With any new LSIC design and process there is a learning curve associated with the ability to produce fully functional circuits. It is not uncommon for initial yield to be zero for the first several lots. In general, the most significant initial yield detractor is mask errors which result in improper circuit function and which can only be uncovered by the running of device lots followed by diagnostic engineering test. Of course it is also possible for a catastrophic event to occur in processing, when people may be running a new process for the first time.

Once all mask errors and major process problems are corrected, yield will typically follow a normal learning curve which applies to the IC industry. Yields tend to increase due to operator familiarity with both the mask set and process which facilitates proper mask alignment, to identification of critical defects, and to an improvement in overall processing efficiency.

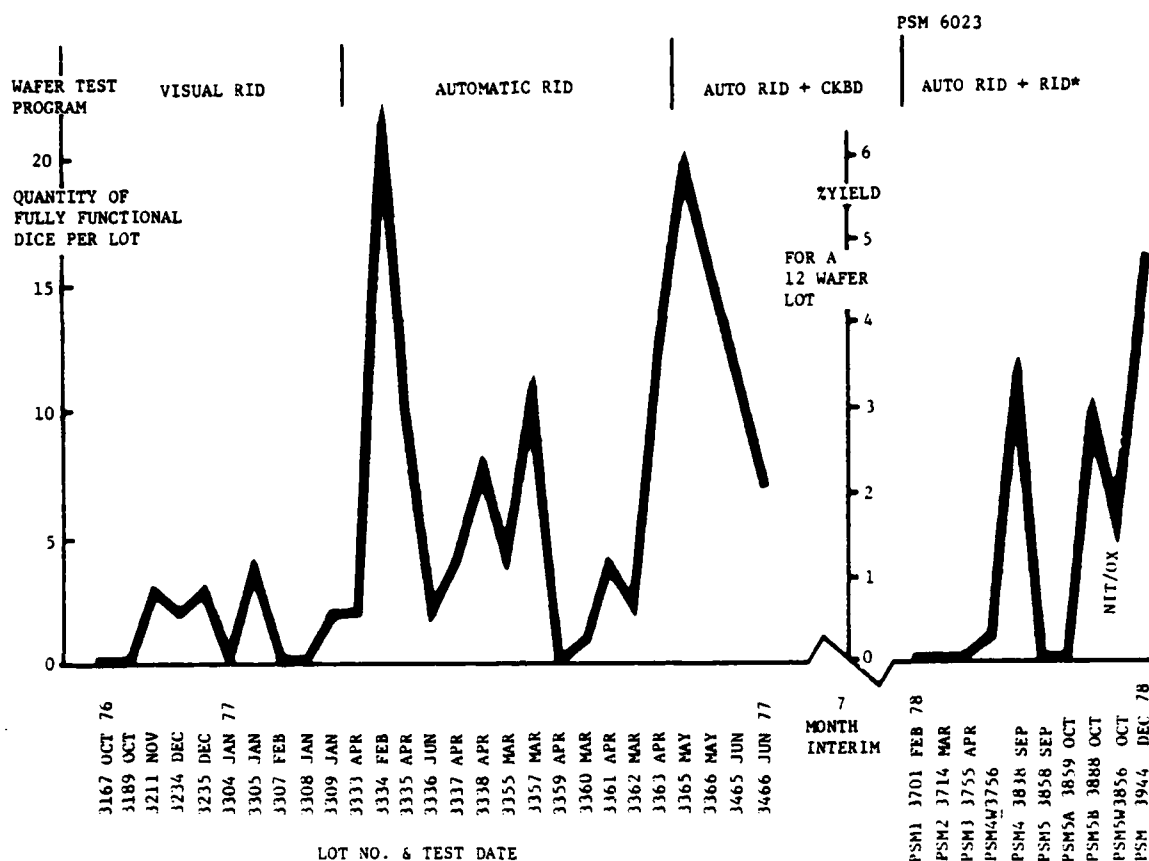
The manufacture of PSM LSIC's has followed this typical industry learning curve.

Wafer yield results for both the 6013 and 6023 are shown in figure 3.46. Initial wafer yield for the 6013 was zero followed by a gradual increase in yield. While a maximum yield per lot of 6013 PSM's was about 7%, average yield on the last 16 lots was about 3%. It should also be noted that the wafer test program became a more rigorous and complete functional test as the ACT 1 program (6013 production) progressed.

Starting July 77 there was a seven month delay in follow-on funding. During this time the ACT process line was essentially shut down. Because of the interruption of lot flow and redesign of the PSM mask set, the 6023 had an initial yield of zero on the first three lots. This was due to both a mask error and initial process problems. Once the problems were rectified there was a marked improvement in LSIC yield. The last six lots processed had an average yield of a little over 2%. This includes two zero yield lots in this group, which had obvious process problems. For the four lots without process errors, device yield was 3.3% even though the most strenuous and complete wafer test program to date was used to functionally evaluate the PSM arrays.

Maximum final yield of the LSIC after roll-off of the learning curve is determined primarily by die size, number of photomaskings, and defect density. The 3% average yield obtained on the PSM LSIC die, which measures 237 by 260 mils and requires 11 masking steps, is much better than the 0.1-0.3% yield which was initially predicted for this part.

In conclusion, the high performance MNOS/SOS PSM LSIC has been manufactured with an average yield of about 3%. A total of 190 fully functional PSM LSIC arrays at wafer test including both 6013's and 6023's were produced during the ACT 1 program. Yield, producibility and process maturity were typically for a part development program and require additional effort prior to commitment for a production run.



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Figure 3.46. PSM 6013: Functional Wafer Test Results

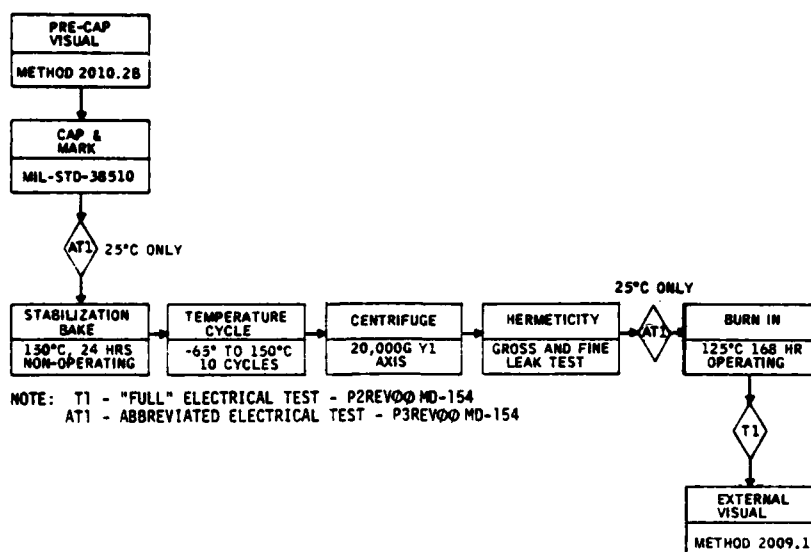
### 3.1.9 PSM LSIC Screen Test

After identification of proper functional operation of the PSM LSIC's through wafer test, these good dice are then packaged and subjected to an environmental and electrical screen per MIL-STD-883 Class B.

The purpose of these tests, which were performed on several 6013 and 6023 device lots, was to screen out any devices which may have long or short term reliability problems.

#### 3.1.9.1 Screen Flow For Class B

The flow of a device subjected to the MIL-STD-883 Class B screen is shown in figure 3.47.



52465

FIGURE 3.47 SCREEN TEST FLOW

Initially a prelid visual inspection of the die after bonding but prior to package lidding is performed. This inspection locates and screens out any dice which may have visual defects due to processing, handling, or packaging. In general these defects would yield an unreliable or even non functional LSIC.

The packages containing dice which pass this inspection are then lidded and tested at 25°C using the MD-154 P3REV00 test program which is detailed in section 7. The parts passing this electrical test proceed for a series of environmental tests.

Included in the environmental tests are stabilization bake, temperature cycle, centrifuge, and hermeticity. The purpose of these tests is to verify the integrity of the package itself and of die mount, wire bond, and lidding which takes place in the packaging operation.

After these environmental tests are completed, devices which pass are then subjected to functional testing at 25°C using the P3REV00 program. Parts passing this test proceed to burn-in.

The main purpose of burn-in is to insure the short term temperature bias stability (TBS) of the PSM LSIC. Prior to burn-in, all arrays are written with the RID pattern. The parts are then subjected to dynamic read bias at 125°C for 168 hours. After removal from this bias, all parts undergo final electrical test, to insure proper functional operation and determine if any shifts in access time or FET parameters have occurred.

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Final electrical test is done on the MD-154 test system using the P2REV00 test program. This program can be run with the device at  $-55^{\circ}\text{C}$  and  $125^{\circ}\text{C}$  as well as the usual  $25^{\circ}\text{C}$ . Packaged devices passing this test are subjected to an external visual inspection prior to buy-off.

## 3.1.9.2 Screen Test Results

PSM LSIC's of both the 6013 and 6023 device type were subjected to the '883 Class B screen described above. Results are summarized in table 3.5.

TABLE 3.5 PSM SCREEN RESULTS

DEVICE TYPE	Q'TY LOTS	Q'TY WF	Q'TY PERFECT INTO SCREEN	Q'TY PERFECT OUT SCREEN	% PASSING SCREEN	Q'TY PARTIAL FCT. ARRAYS OUT OF SCREEN
6013	8	31	46	30	65%	44
6023	3	9	15	12	80%	14
TOTALS	11	40	61	42	69%	58

A total of 46 perfect PSM's from eight 6013 device lots, from 31 different wafers within these lots, were subjected to the screen, and 65% of these passed the screen test. Fewer lots of 6023's have been processed and 15 fully functional die from 3 lots and 9 wafers were screened with 80% of these devices passing.

During the ACT program, 61 perfect devices from a total of 11 lots and 40 wafers were screened with 69% of all devices passing the MIL-STD-883, Class B screen.

In addition to the fully functional arrays, several devices with one or more perfect I/O's were also screened.

These screened parts were used for life test, total dose test, dose rate test, and endurance/retention tests which were performed in part by both Westinghouse and Northrop and will be reported on in detail in later sections of this report.

## 3.1.9.3 Screen Summary

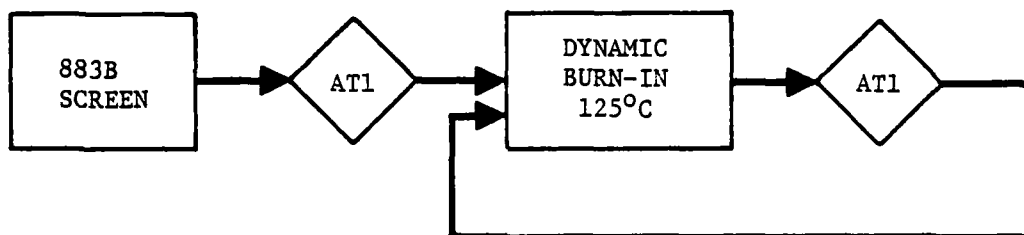
Both 6013 and 6023 PSM LSIC's from several device lots and wafers have been subjected to 883 Class B screen with a high throughput ( 70%) of devices. This indicates that a high performance MNOS/SOS LSIC memory can be produced for use in military system applications. This screening yield is based on a limited sample size and most likely would increase as additional data is collected and corrective actions feedback to eliminate sources of device fallout.

## 3.1.10 PSM LSIC Environmental/Reliability Test Results

During the ACT program both 6013 and 6023 PSM LSIC's were subjected to long term temperature bias stress (TBS) testing to establish long term reliability and stability of the part.

### 3.1.10.1 Life Test Flow Diagram

The flow diagram for this long term temperature bias stress testing, known as life test, is shown in figure 3.48.



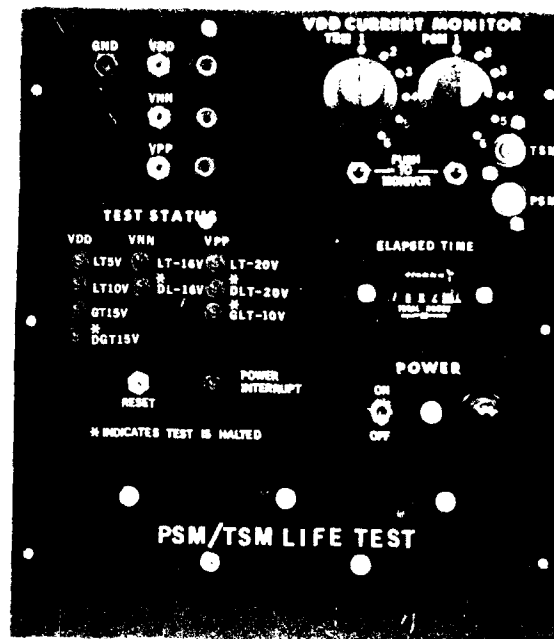
NOTE: AT1 - ABBREVIATED ELECTRICAL TEST - P3REV00 MD-154

FIGURE 3.48 PSM LSIC LIFE TEST FLOW DIAGRAM

Initially parts are selected for life test after they have successfully completed the 883 level B screen. The parts then undergo electrical test for measurement of test FET parameters, array parameters, and access time using the MD-154 P3REV00 program, which is detailed in section 7. The information obtained in this test provides an initial data base for life test.

The selected parts are then subjected to a dynamic burn-in at 125 C. Read mode dynamic input signals are provided to the devices under test (DUT's) by a dedicated life test exerciser (which is shown in figure 3.49) capable of driving 10 device boards, each with seven sockets. Timing details of the output waveforms provided by this exerciser are contained in CDRL item C002: Preliminary Specification for MNOS/SOS PSM Permanent Store Memory, Part No. 6023, dated 20 July 1978. This exerciser contains front panel LED displays to indicate any deviations from normal for the power supply voltages to the PSM devices. If a supply condition occurs due to line transients that could be harmful to the DUTs, the test is automatically halted and is later restarted by a manual reset switch located on the front panel. Also included on the front panel is an elapsed time indicator.

After a selected number of hours, the DUTs are cooled under bias and then removed from bias and retested using the MD-154 P3REV00 program. Any device parameter deviations from the initial data base are noted for each device. The devices are then returned to life test burn-in with later successive post stress electrical tests performed.



## 3.1.10.2 Life Test Results

Life tests were performed on both the 6013 and 6023 PSM LSIC. On-chip test FET parameters as well as worst case array access time were monitored as a function of temperature bias stress hours. A total of 35 LSIC's from 11 device lots and 21 wafers were subjected to life test for a period of time exceeding 53,000 device hours with a resulting failure rate of 5.6% per 1000 device hours. These tests included unscreened as well as screened parts. A much lower failure rate has been observed for the screened parts above.

### 3.1.10.2.1 Stability of Test FET Parameters

The p-enhancement and n-depletion test FET pair located on the LSI die were under static bias, which simulates internal array bias, during life test of the PSM LSIC. P-channel threshold voltage,  $V_{TP}$ , and n-channel zero bias drain-source current,  $I_{DSO}$ , were measured using the MD-154 test system both prior to and following each stress period.

Results of these tests will reveal device parameter temperature bias stress induced shifts, if they occur. These could effect performance of the PSM LSIC.

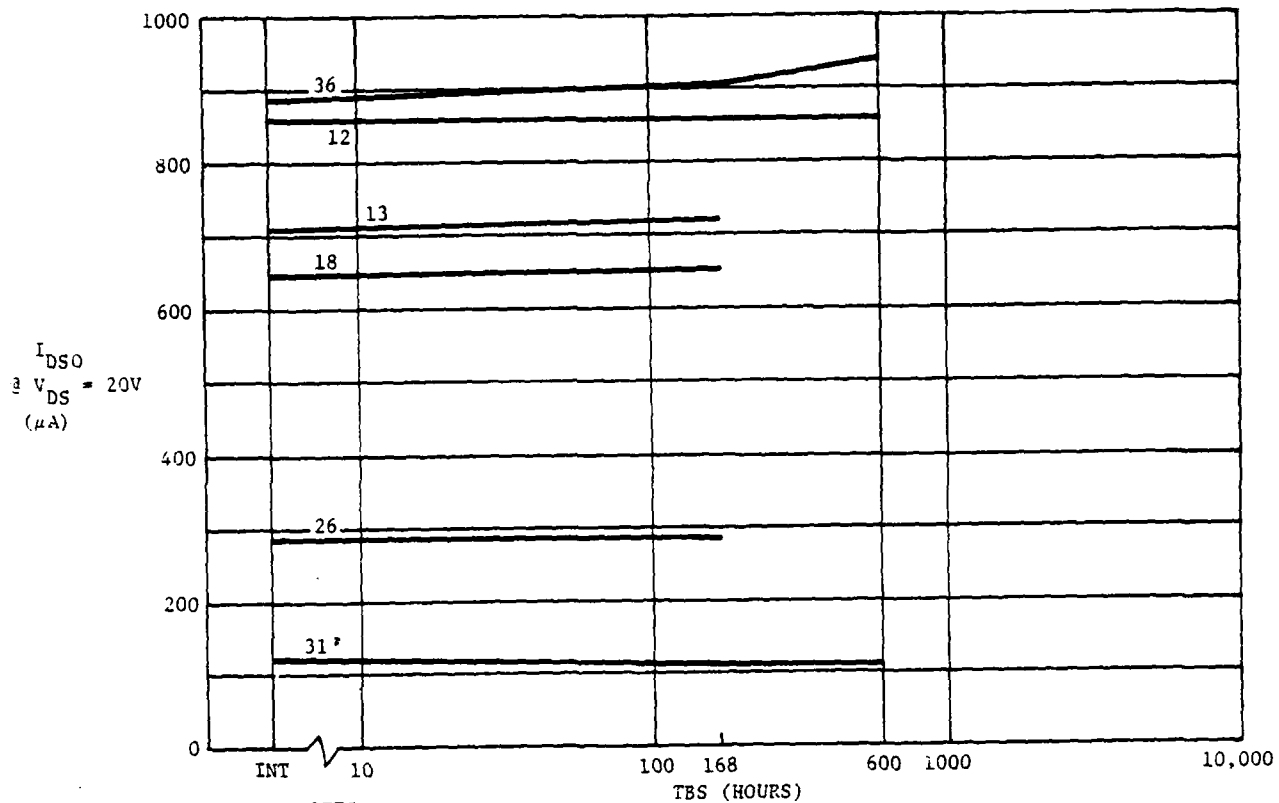
#### a) N-channel depletion Mode Zero Bias Current, $I_{DSO}$

Since measurement of  $I_{DSO}$  is very easily automated and is also a sensitive measure of shifts in the pinchoff voltage,  $V_p$ , with  $I_{DSO}$   $V_p^2$ ,  $I_{DSO}$  was routinely monitored during life test. While results shown herein are for  $I_{DSO}$ ,  $V_p$  stability was also verified by hand measurement on an adequate number of devices.

Figure 3.50 shows  $I_{DSO}$  stability vs TBS for devices from three wafers from a device lot. Shifts of  $I_{DSO}$  remained within the measurement resolution of the MD-154 for all but one device which increased by 6% after 600 hours of TBS.

Figure 3.51 shows TBS results for another device lot after a total life test of 1074 hours. Shifts from initial value after 1074 hours range from 0 to 8%, with the majority of the distribution having less than 1% overall change.

These very small changes in  $I_{DSO}$  are of such a small magnitude that no change in PSM LSIC operation would be expected.



NOTES:

- 1) TBS BIAS:  
VGS = 0V  
VDS = 0V
- 2) PARTS WITH DATA  
ENDING @ 168 HRS.  
TAKEN OFF SCREEN  
FOR OTHER TESTING

S/N	WF
5112, 13, 18	1
5126	7
5131, 36	10

52432

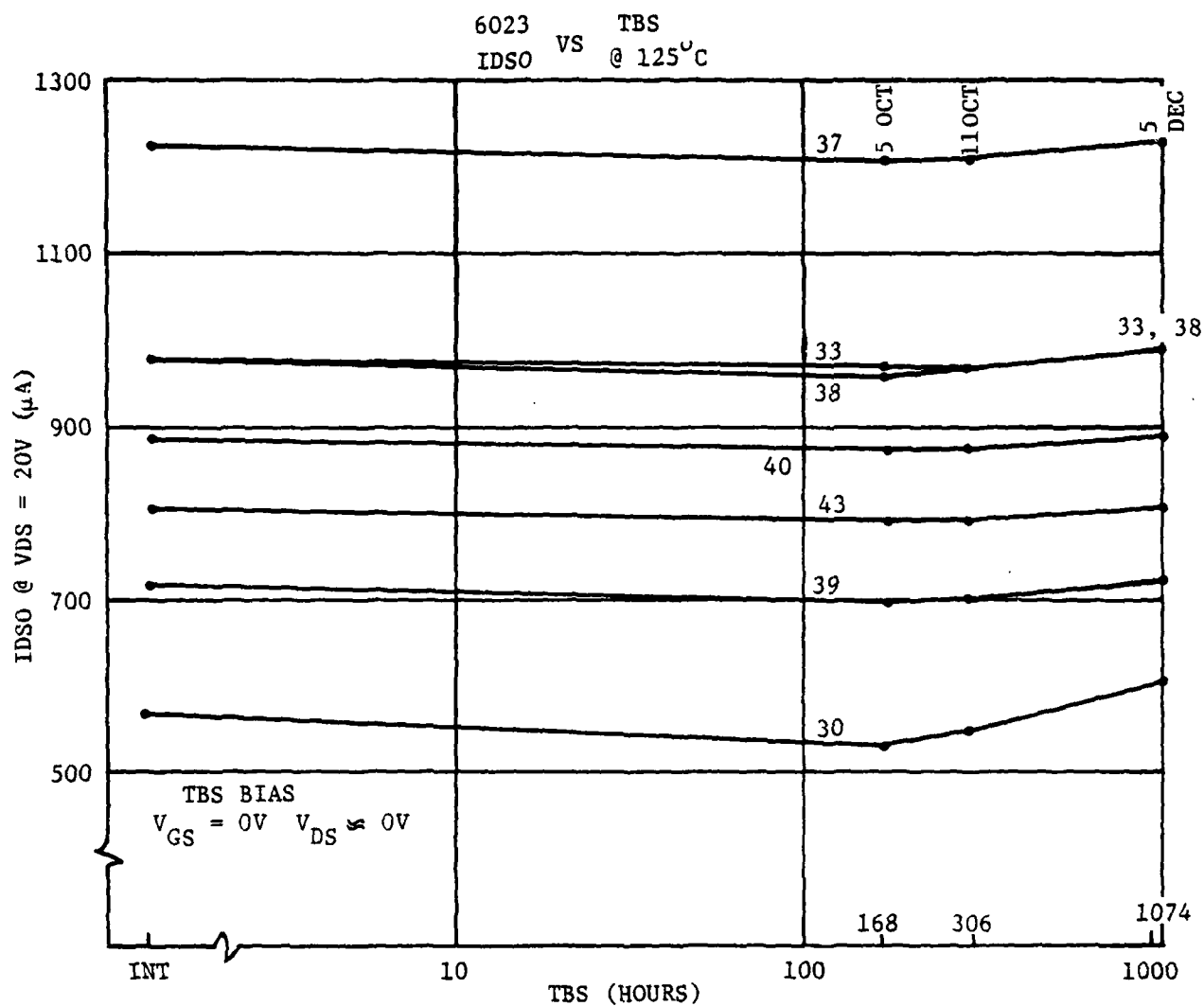
FIGURE 3.50 LOT 3888 SCREEN & LIFE TEST IDS0 VS TBS (T = 125°C)

b) P-channel Threshold Voltage, V<sub>TP</sub>

During life test, the p-channel test FET on the LSIC die was biased with V<sub>GS</sub> = -21.0 volts, which is the maximum bias which occurs within the PSM during the read mode of operation. This bias produces a maximum field of such a polarity as to cause worst-case shifts in V<sub>TP</sub> during life test.

Figures 3.52 and 3.53 show V<sub>TP</sub> versus temperature bias stress hours for several devices from two different lots. Lot 3888 has undergone life test of 600 hours while lot 3838 has completed in excess of 1000 stress hours. V<sub>TP</sub> shifts from initial value range from 1 to 4% over the entire life test period.

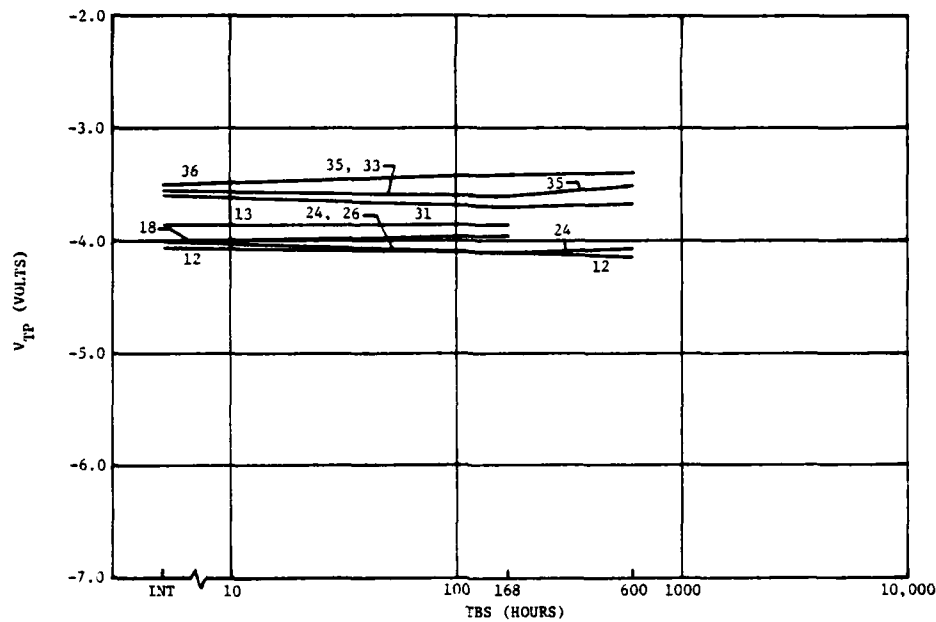
This excellent stability of p-channel threshold voltage should yield excellent stability for the LSIC in which it is embodied.



S/N	WF
5030	9
5033	12
5037, 38, 39, 40, 43	14

52433

FIGURE 3.51 LOT 3838 SCREEN & LIFE TEST



NOTES:

- 1) TBS BIAS:  
VGS = -21V  
VDS = 0V
- 2) PARTS WITH DATA  
ENDING @ 168 HRS  
TAKEN OFF SCREEN  
FOR OTHER TESTING

S/N	WF
5112, 13, 18	1
5124, 26	7
5131, 33, 35, 36	10

52059

FIGURE 3.52 LOT 3888 SCREEN & LIFE TEST  $V_{TP}$  VS TBS ( $T = 125^{\circ}\text{C}$ )

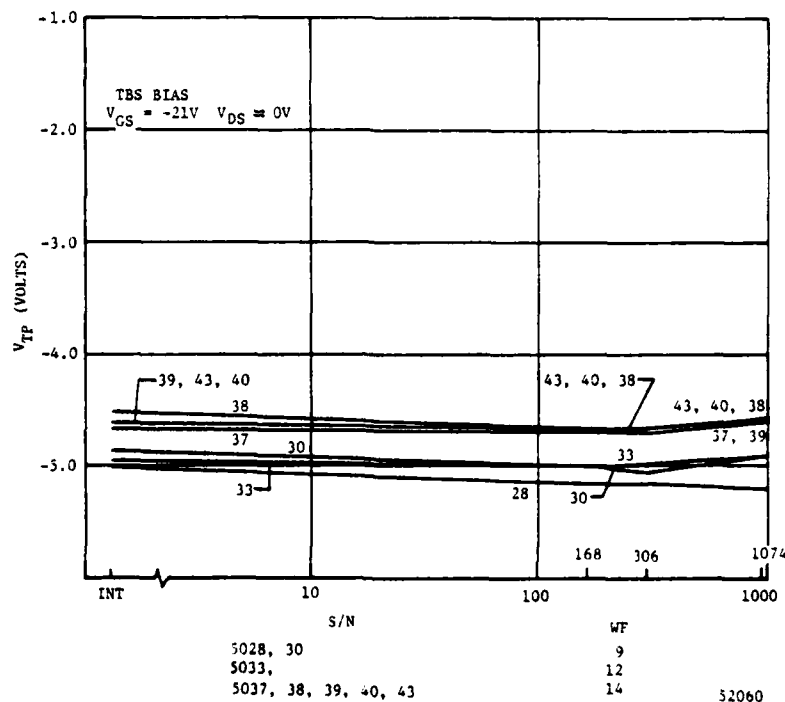


FIGURE 3.53 LOT 3838 SCREEN & LIFE TEST 6023  $V_{TP}$  VS TBS @  $125^{\circ}\text{C}$

## 3.1.10.2.2 Stability of PSM LSIC

As previously mentioned, exhaustive post life test testing is performed on the PSM LSIC using the MD-154 automated test system to ensure that no device parameters have shifted in such a way as to impair functional or reliable operation of the circuit.

Figures 3.54 and 3.55 show the worst case PSM LSIC access time as a function of TB hours for devices from two different lots. Maximum shifts in access time over a life test of more than 1000 hours were 2.5% while the range of shifts for all devices was 1.3-2.5%.

## 3.1.10.3 Life Test Summary

As part of the ACT program, 6013 and 6023 PSM LSIC's have undergone extensive life testing in excess of 53,000 device hours at 125°C under dynamic bias conditions. Excellent stability was observed for the PSM LSIC which offers potential for a low failure rate required for a reliable alternative for nonvolatile program store memory for advanced guidance computers.

## 3.1.11 PSM LSIC Radiation Test Results

During the ACT 1 Program, PSM LSIC's and test vehicles were subjected to various types of radiation testing to determine device characteristics and performance both during and immediately following a radiation event. Total dose, dose rate, and EMP testing was performed on the PSM.

### 3.1.11.1 Total Dose Test Results

Total dose testing was performed on both the 6013 and 6023 PSM LSIC as well as the 6013T and 6023T basic test vehicles. N depletion mode and p enhancement mode FET parameters as well as worst case array access time were measured immediately following successive total dose exposures. In addition to basic test vehicle parts, more than 180 PSM LSIC's, which included 127 partial or fully functional arrays, from 24 device lots and 61 different wafers were subjected to total dose tests.

It should be pointed out that on the first phase of the program an atmospheric chemical vapor deposition (APCVD) system was used to deposit the nitride film which in part forms the gate dielectric. The APCVD nitrides lacked repeatability from wafer to wafer and lot to lot in film thickness,

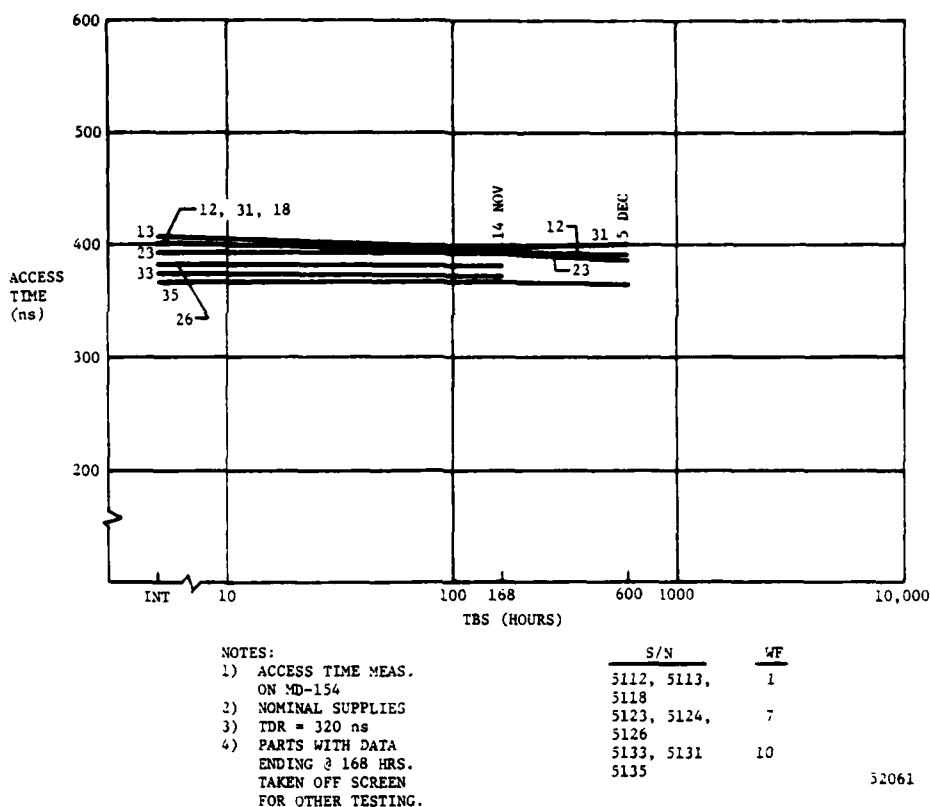


FIGURE 3.54 LOT 3888 SCREEN & LIFE TEST ACCESS TIME VS TBS ( $T = 125^{\circ}\text{C}$ )

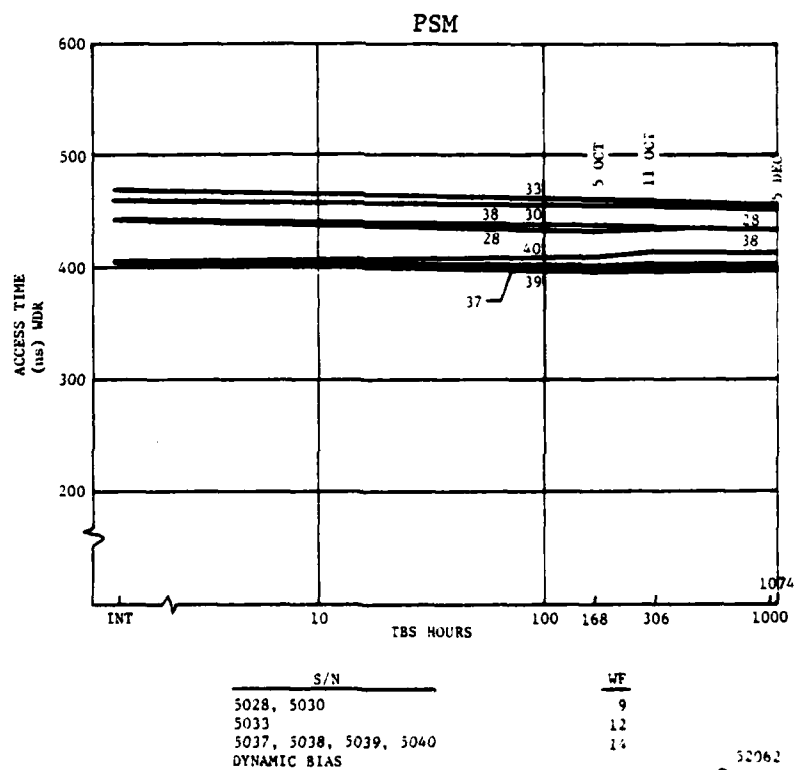


FIGURE 3.55 LOT 3838 SCREEN & LIFE TEST 6023 VS. TBS @  $125^{\circ}\text{C}$

ACCESS TIME (WORST CASE)

charge in the deposited insulator, and conductance properties of the insulator. PSM LSIC's fabricated using this technique tended to fail functionally, often at a total dose exposure level of "1 to 2". Since this was below the program goal, some improvement was necessary.

On the second phase of the program, nitride deposition was performed using a new low pressure chemical vapor deposition (LPCVD) system. In this system there is much tighter control of insulator charge, thickness, and conductivity. Devices fabricated using this process, which is now the standard ACT 1 process, attain a much higher level of radiation hardness, which exceeds the program goals and will be reported on herein.

## 3.1.11.1.1 Total Dose Effects on Test FET Parameters

Test FET's located on both the LSIC array and the basic test vehicles were subjected to varying levels of total dose exposure. These devices were biased to simulate all bias conditions which occur within the array. Device parameters which include p-channel threshold voltage,  $V_{TP}$ ; p-channel leakage current,  $I_{LP}$ ; n-channel depletion mode zero bias drain-source current,  $I_{DSO}$ ; and n-channel (depletion mode) leakage current,  $I_{LN}$ , were measured prior to and following each total dose exposure level.

Results of these tests give an indication of where within the LSI circuitry the greatest changes in functional performance will occur.

### a) N-channel Depletion Mode Leakage Current, $I_{LN}$

Figure 3.56 shows  $I_{LN}$  in nanoamperes per mil of channel width as a function of total dose. Initially this leakage was 10-100 na/mil and increased approximately to ten times this value after a total dose exposure of "3". Maximum  $I_{LN}$  at this exposure level is 0.7us/mil, which is below the design limit of 1uA/mil.

This post-rad magnitude of leakage current has no noticeable effect on overall circuit functional operation, but results in a slightly higher standby power dissipation of about 2 mW for the PSM LSIC device.

### b) N-channel Depletion Mode Zero Bias Current, $I_{DSO}$

In general, under array bias conditions,  $I_{DSO}$  tends to remain fairly constant or actually increase with an increase in total dose exposure. This trend is evident in figure 3.57 which shows  $I_{DSO}$  of an n-depletion mode FET as a function of total dose exposure.

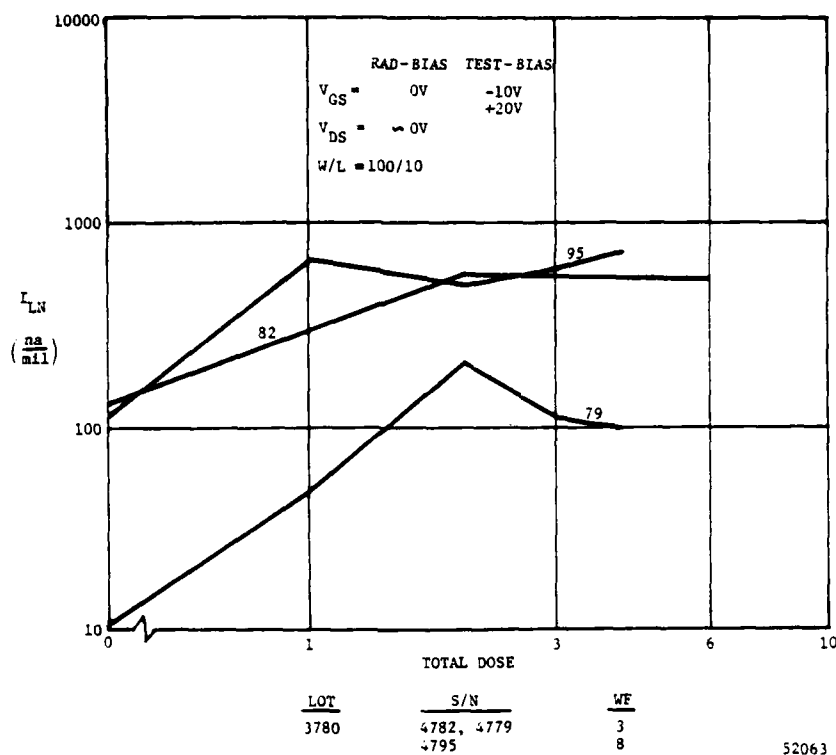


FIGURE 3.56 LEAKAGE CURRENT, n - DEPLETION MODE, VS TOTAL DOSE - 6023 LSI TEST FET

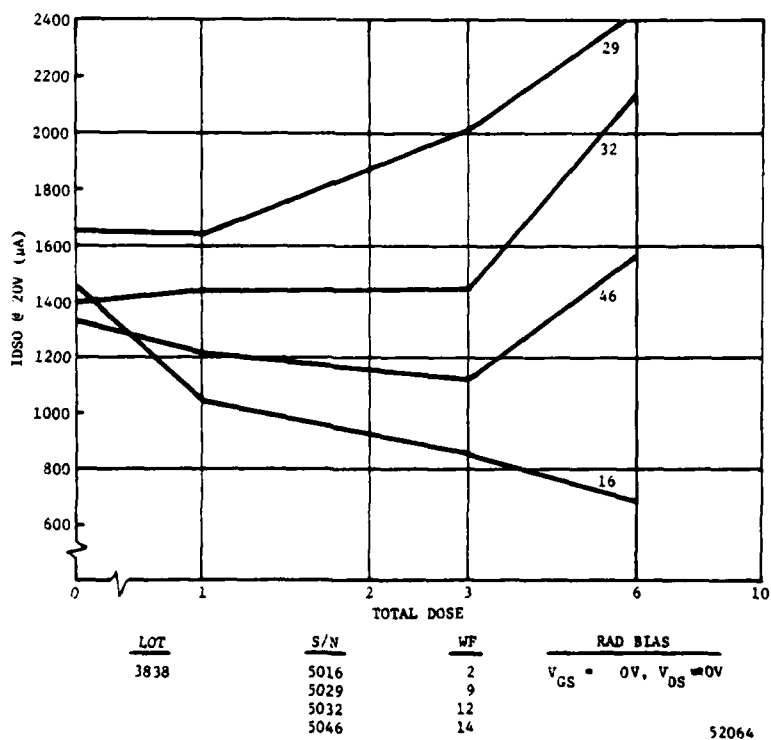


FIGURE 3.57 6023 IDS0 VS. TOTAL DOSE

Both initial  $I_{DSO}$  in the range of 1300-1700uA and post-rad (level "3") in the range of 900-2000uA are quite adequate for proper circuit operation. The increase in  $I_{DSO}$  with total dose exposure actually will result in faster access time of the LSIC array, but at the expense of additional power dissipation.

## c) P-channel Leakage Current, $I_{LP}$

Due to the nature of p-enhancement mode leakage current, no major increases in leakage currents were expected or obtained during total dose exposures. In general, after a total dose exposure to "3",  $I_{LP}$  was at least an order of magnitude below the design limit of 1uA/mil.

## d) P-channel Threshold Voltage, $V_{TP}$

In general, the  $V_{TP}$  shifts with total dose exposure tended to be gate-source bias ( $V_{GS}$ ) dependent.

It was found that the worst shift in  $V_{TP}$  occurred when the FET was biased at  $V_{GS} = -12V$ . This bias condition occurs with the PSM LSIC at several of the signal input pins during normal circuit operation. Figure 3.58 shows test FET  $V_{TP}$  shift versus total dose for this bias conditions. Maximum shift after a total dose exposure of "3" was -2.4 volts, which is within the design limit of -2.5 volts shift after this exposure.

Another bias condition of interest is  $V_{GS} = -21$  volts since this bias appears at several different internal circuit nodes within the PSM LSIC. Test FET  $V_{TP}$  versus total dose exposure while under this bias condition is shown in figure 3.59 and indicates a maximum shifts after an exposure of "3", of -1.5 volts with shift of 0.3-0.5V being typical.

The direction of threshold voltage shift raises the magnitude of  $V_{TP}$ , thereby slowing down switching speed within the LSIC array. This should result in slower overall access time, but in some cases this speed degradation may be overcome by the increase in  $I_{DSO}$  with total dose.

### 3.1.11.2 Total Dose Effects on PSM LSIC

Both functional and parametric measurements were made prior to and following total dose exposure of 6013 and 6023 PSM LSIC arrays which were biased in the dynamic read, static read select, and static deselect modes of operation.

Figure 3.60 shows worst case access time as a function of total dose, for static deselect biased PSM's from several 6023 device lots. Initial access times range from 350 to 540 nanoseconds and in many cases decrease at a

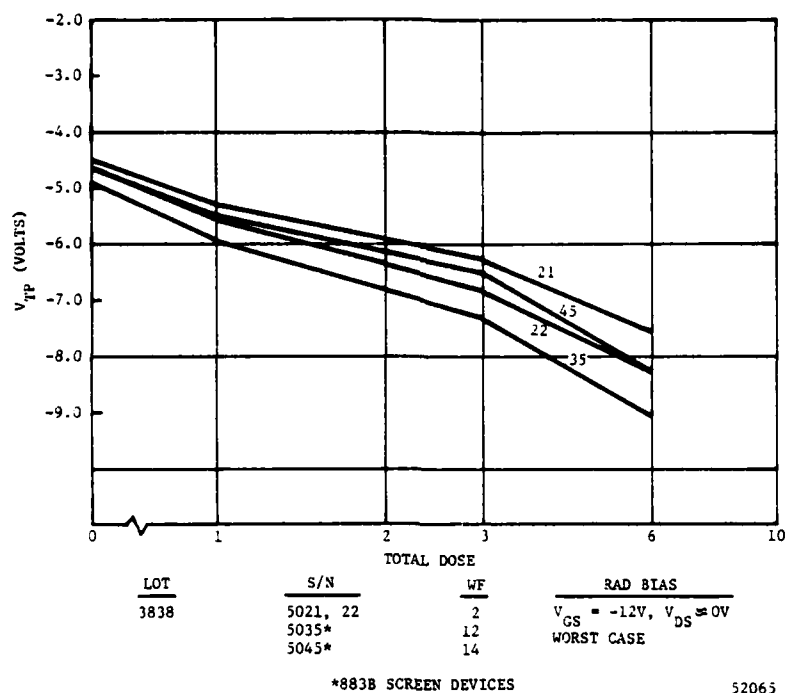


FIGURE 3.58 6023  $V_{TP}$  VS. TOTAL DOSE

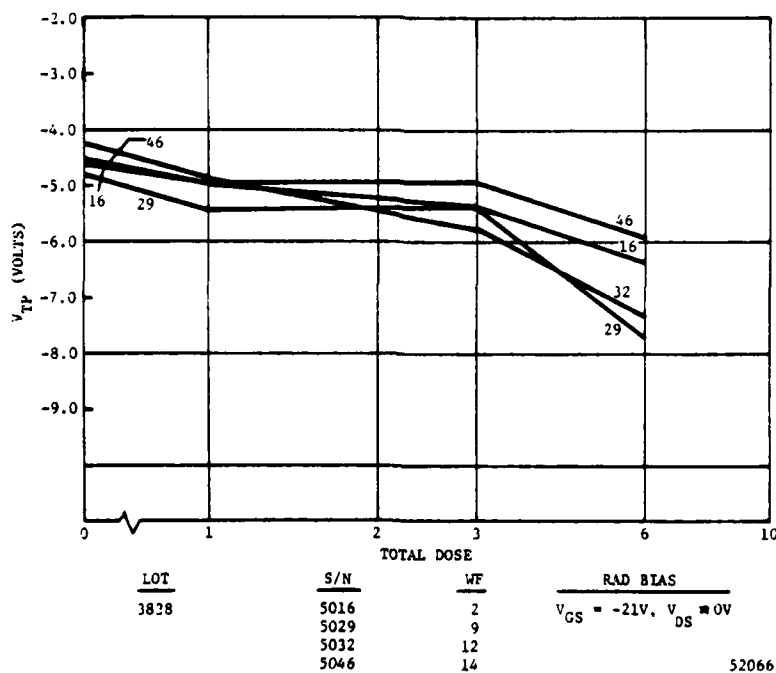
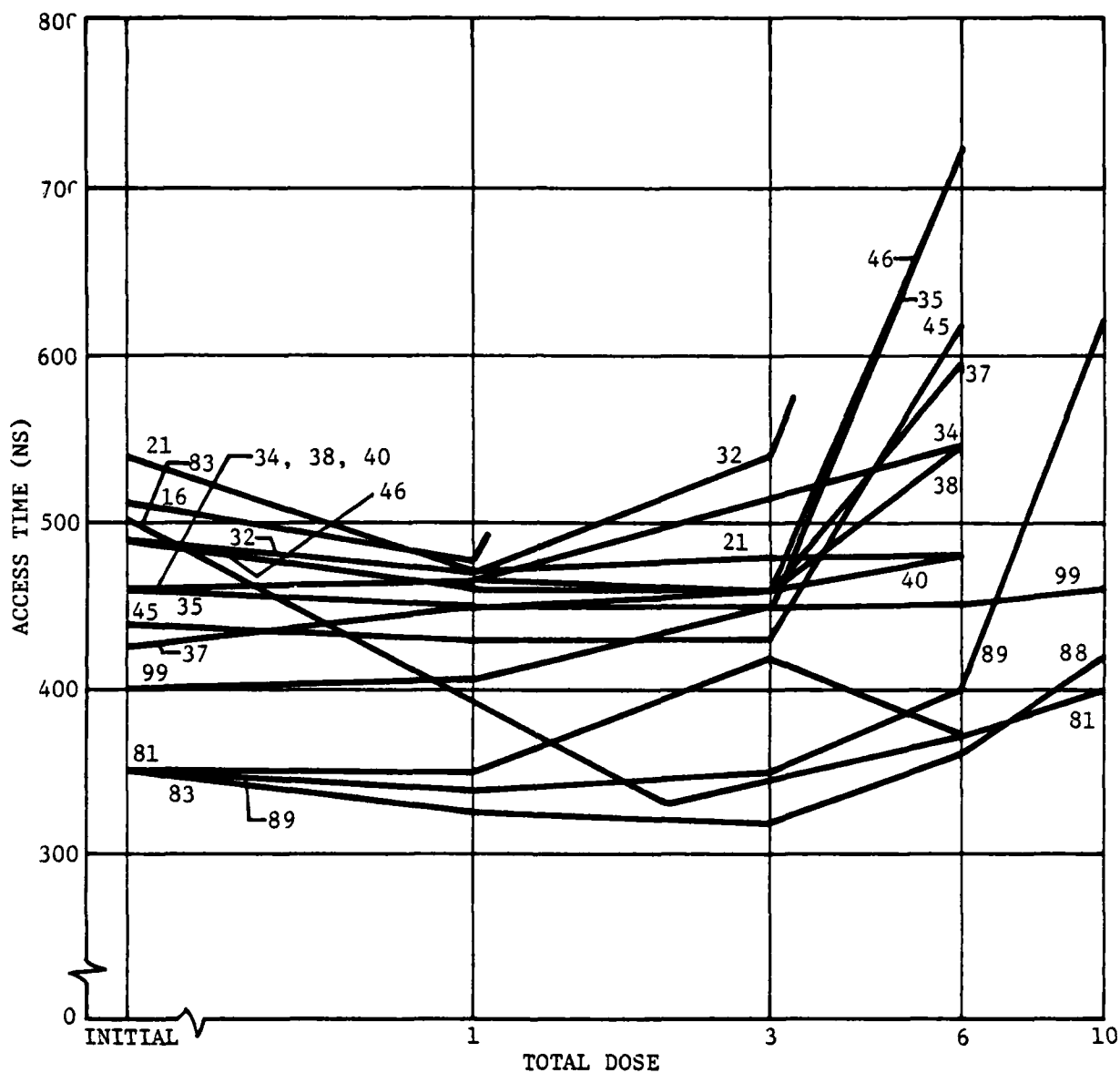


FIGURE 3.59 6023  $V_{TP}$  VS. TOTAL DOSE



LOT	WF	SERNO	RAD BIAS	TEST BIAS
3780	3	4781, 4783	STATIC DESELECT	NOMINAL SUPPLIES
	6	4789, 4788	NOMINAL SUPPLIES	& TIMING, WITH DR
	7	4799		
3756	11	4934, 4938		
		4940, 4937		
3838	2	5021, 5016		
	12	5032, 5035*		
	14	5045*, 5046		

\*SCREENED TO LEVEL B, '893

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FIGURE 3.60 PSM 6023: ACCESS TIME VS. TOTAL DOSE WORST-CAST OUPUT, PERFECT OUTPUTS

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dose level of "1" and in some cases to "3". This is due to the fact that the increase in  $I_{DSO}$  is overcompensating for an increase in  $V_{TP}$  magnitude and resulting in a faster access time. Access time post "3" and "6" tend to increase over the previous dose.

Access times after an exposure of "3" ranged from 320 - 540 nanoseconds, with the majority of parts having an access time of less than 475 nanoseconds. While the initial program goal was to achieve an access time of 370 nanoseconds after this total dose exposure, subsequent system architectural changes now allow a PSM access time of 500 nanoseconds while still meeting the overall MX computer system goal.

It should also be pointed out that functional operation of most parts exceeded the total dose goal with functional operation to "6" and "10" total dose levels. This extended operation greatly simplifies the hardness assurance aspects of advanced computer systems utilizing these devices.

### 3.1.12 PSM LSIC Endurance/Retention

Since the PSM LSIC is intended for main program storage applications, it should be capable of storing data for long periods of time after a relatively small number of write reversal cycles. In particular for this program, the PSM retention specification was for the array to maintain proper data storage for a period of not less than three years after  $10^4$  write reversals, and to show functionality after  $10^8$  write reversals.

In order to determine overall retention of a memory array, the memory window voltage (difference in threshold voltages of the two MNOS FET's which make up a cell) as a function of time must be known for all cells in order to determine the worst-case window which will ultimately limit the long term retention of the array. Previous designs had to rely on characteristics of a single test FET not in the array or to operate the array with nonstandard voltages and timing to arrive at a prediction of the long term retention of the array. Neither of these methods has proved to be satisfactory.

The 6013 and 6023 PSM LSIC's include a unique test circuit which allows direct analog measurement of memory window for all 1024 memory cells. This circuitry is described in detail in section 3.1.5.2.5 of this report.

#### 3.1.12.1 PSM Endurance/Retention Measurement Techniques

Initially 6013 and 6023 LSIC's were selected from several device lots, some of which underwent the '883 level B screen and some of which did not. Using the laboratory test set, selected groups of addressed cells underwent  $10^4$ ,  $10^6$ , and  $10^8$  write reversals. Some of the cells within each LSIC were not stressed at all. The standard set of stressed bits were: 40 bits from address 6C-93 received  $10^4$  reversals, 8 bits from address 7C-83 received  $10^6$  reversals and 3 bits from address 7E-80 received  $10^8$  reversals. All remaining bits were essentially unstressed.

Using the laboratory test set or MD-501 test system, memory windows of cells subjected to the various endurance stresses were measured at various points in time so that memory window as a function of time could be plotted.

#### 3.1.12.2 Test Results

In general the 6013 PSM LSIC was processed using atmospheric pressure chemical vapor deposition (APCVD) nitride and the 6023 using low pressure chemical vapor deposition (LPCVD) nitride, the latter of the two becoming the present baseline process.

Since this nitride composes part of the memory gate dielectric and determines in part the endurance/retention characteristics of the memory FET's, both 6013 (APCVD) and 6023 (LPCVD) PSM LSIC's were evaluated for endurance/retention characteristics using the built-in memory window test feature.

### 3.1.12.2.1 PSM 6013 (APCVD) Endurance/Retention Test Results

By measuring the memory window as a function of time, one can predict long term retention for the array. The sense amplifier within the array will cease to detect proper data when the memory window voltage is less than the detection sensitivity, which is 100mV for both the 6013 and 6023.

Figure 3.61 shows a plot of 6013 memory window voltage versus time for cells which have undergone  $10^4$ ,  $10^6$ , and  $10^8$  endurance reversals. Some basic observations can be made. The magnitude of the memory window decreases with an increasing number of write reversals and the decay rate or change in window voltage per decade of time increases with an increasing number of write reversals. Using this plot and extrapolating over a fraction of one decade, retention is predicted to be much more than 3 years ( $10^8$  seconds) after  $10^4$  write reversals, near 3 years after  $10^6$  reversals, and 3 months to 1 year after  $10^8$  reversals.

The effects of high temperature on storage capability is shown in figures 3.62 and 3.63. The parts were initially subjected to  $10^4$  and  $10^6$  reversals respectively and then stored under zero bias at  $125^\circ\text{C}$ . The memory window decay rate has increased slightly due to this high temperature storage from 0.25 V/decade in figure 3.61 ( $T = 25^\circ\text{C}$ ,  $R = 10^4$ ) to 0.3-0.4 V/decade in figure 3.62 ( $T = 125^\circ\text{C}$ ,  $R = 10^4$ ). The decay rate after  $10^6$  reversals and storage at  $125^\circ\text{C}$  is 0.35-0.6 V/decade as shown in figure 3.63. From these plots retention of greater than 3 years after  $10^4$  write reversals and 6 months to 1 year after  $10^6$  reversals is predicted with data storage at  $125^\circ\text{C}$ .

### 3.1.12.2.2 PSM 6023 (LPCVD) Endurance/Retention Test Results

Figure 3.64 shows a plot of the high and low conductance memory threshold voltage as a function of time and endurance stress for individual memory test FET's. While this data cannot be used to predict absolute retention of the entire LSIC array, it does give an indication of the endurance/retention qualities of the gate dielectric. This plot shows the memory window for both an unstressed device and one which has undergone  $10^4$  write reversals and indicates a retention period of greater than 3 years for the stressed device.

Actual memory window measurements, using the built-in test feature, were also measured on 6023 PSM LSIC's. Figure 3.65 shows memory window as a function of time for unstressed addresses ( $R=10$ ) and those with  $10^4$  write reversals. In either case the extrapolated retention is much greater than 3 years.

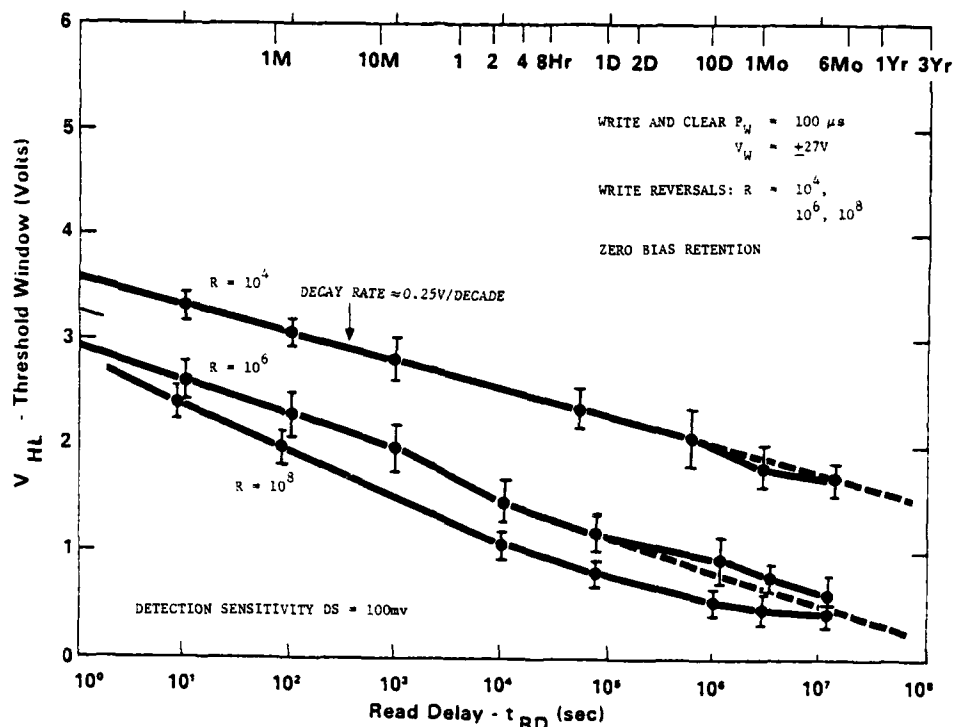


Figure 3.61. PSM: Pulse Response and Retention

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### 3.1.12.3 Summary

Using a unique built-in test feature, all 1024 memory windows of the actual PSM array have been measured. By extrapolating over approximately one decade, a retention period exceeding the MX program specification of 3 years has been predicted for data storage at both 25 and 125°C for 6013 PSM LSIC's with APCVD nitride and similar performance has been achieved on the 6023 utilizing an LPCVD memory gate nitride process.

### 3.1.13 PSM LSIC Design Verification

Exhaustive testing was performed on the 6013 to verify the design and operating characteristics of the PSM LSIC. The results of this testing, which include data provided from laboratory testing and automatic testing of the LSIC by both Westinghouse and Northrop, is detailed in CDRL item C006, Design Verification Test Report for MNOS/SOS Electrically Alterable Read-Only Memory, EAROM (Permanent Store Memory) (6013 PSM) dated August 1977.

### 3.1.14 PSM LSIC Developmental Tests

Developmental testing was performed on the 6013 LSIC and results of this testing, which are detailed in CDRL item C006, Development Test Report for MNOS/SOS Electrically Alterable Read-Only Memory, EAROM (Permanent Store Memory) (6013 PSM) dated August 1977, in conjunction with the design verification, screen, nuclear, and environmental/reliability test results indicate that the PSM LSIC meets the developmental objectives of the ACT program.

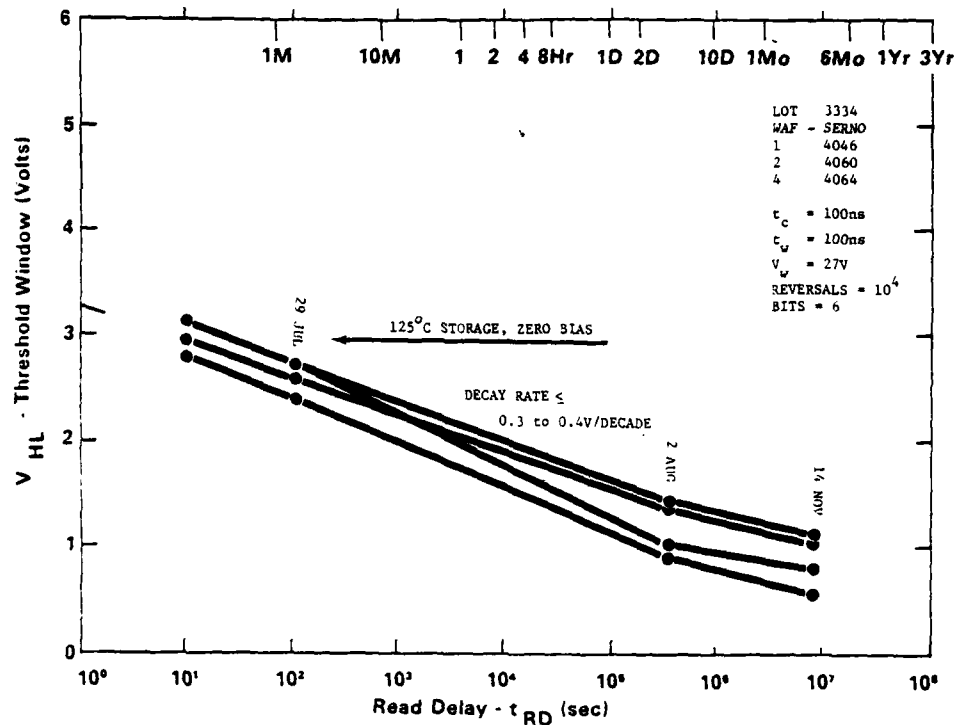


Figure 3.62. PSM: Pulse Response and Retention 125°C,  $R = 10^4$  52436

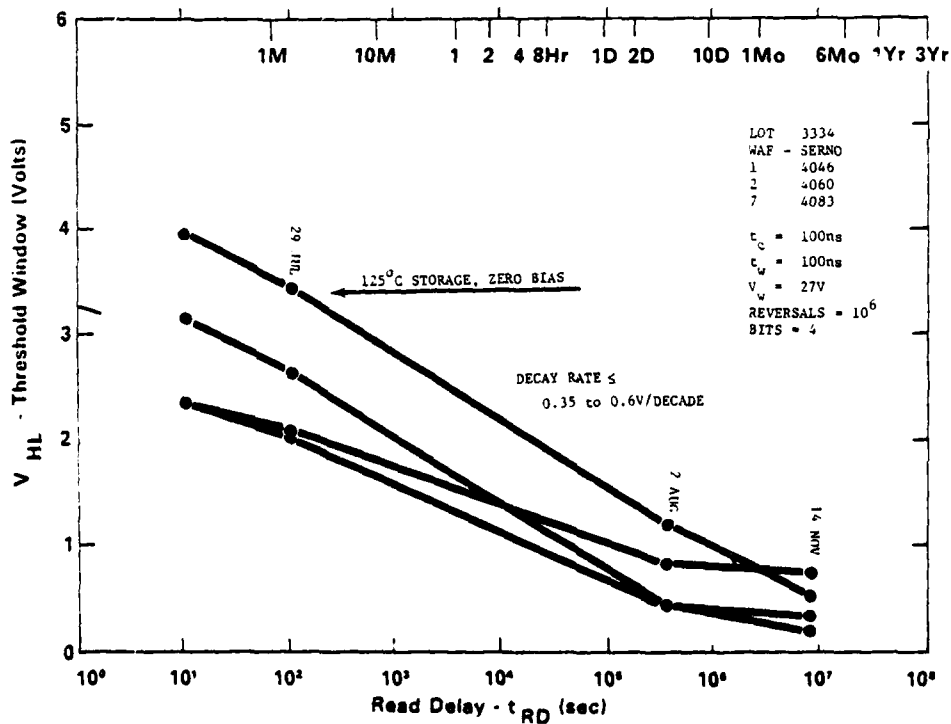


Figure 3.63. PSM: Pulse Response and Retention 125°C,  $R = 10^6$  52437

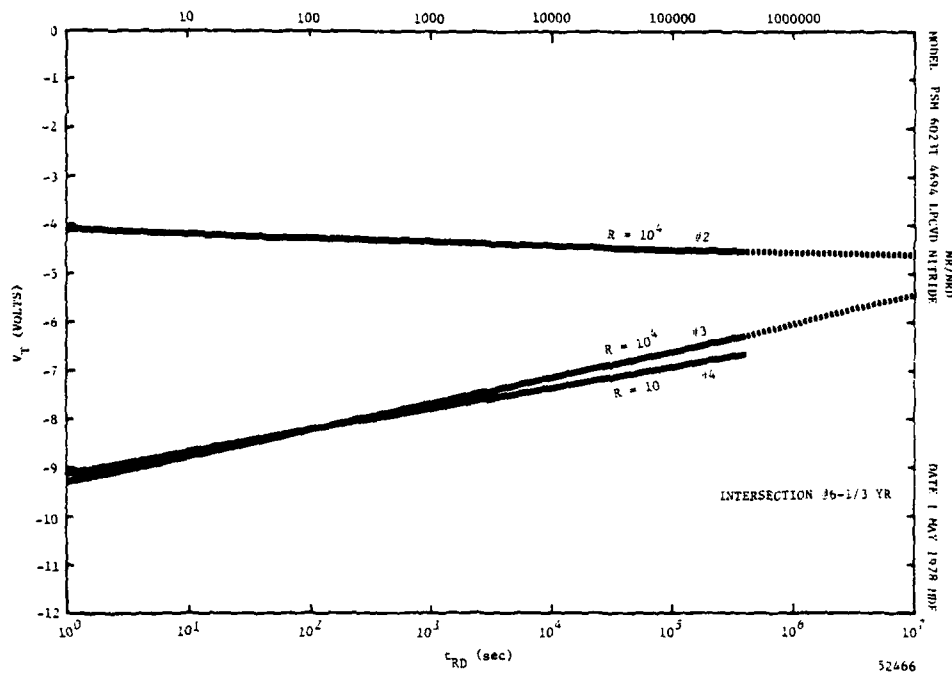


Figure 3.64. PSM  $\pm 27V$ , 100 $\mu$ sec Pulse Response from Saturation

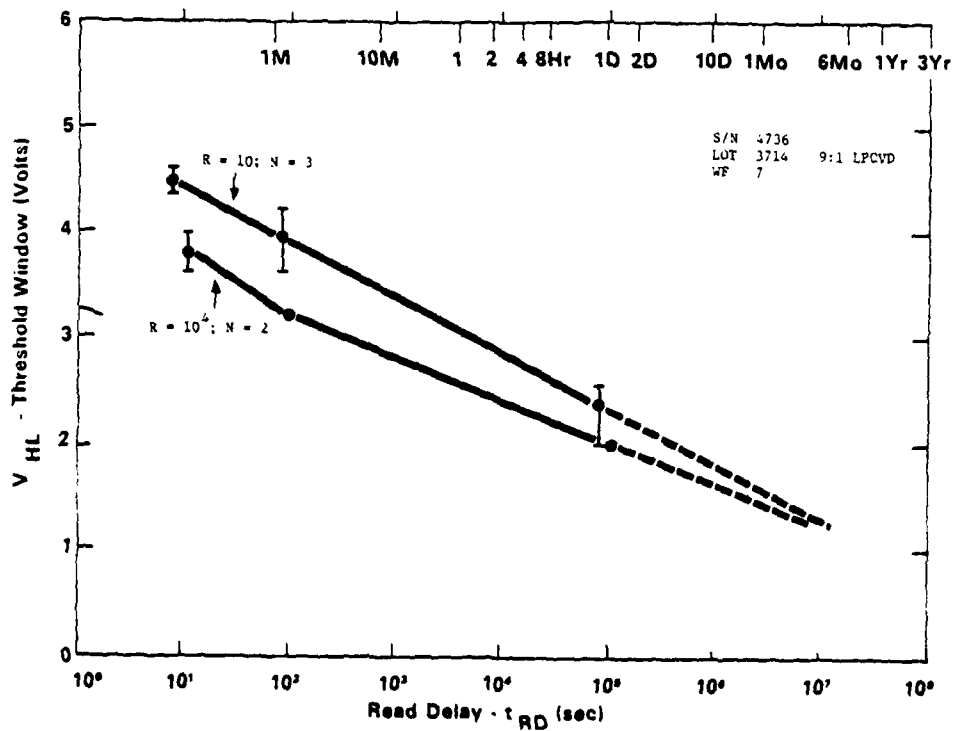


Figure 3.65. 6023 PSM: Pulse Response and Retention

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### 3.2 THE TEMPORARY STORE MEMORY, TSM & RAM

In order to meet the program goals for this extremely fast write, random access, nonvolatile memory, a novel approach was necessary in design. The goals were:

- 512-bit nonvolatile memory
- Write cycle time of 1.0  $\mu$ s
- Read cycle time of 1.0  $\mu$ s
- Read access time of 450 ns
- Retention of 48 hours after  $10^8$  data reversals
- Endurance of  $10^{12}$  reversals
- Low power
- Radiation hardness

#### 3.2.1 Technology and Design Approach

Achievement of writing MNOS memory transistors in one microsecond required two departures from the design used for slow-write, read-mostly nonvolatile memory. One was to write both transistors per bit at the same time, one to the high conductance state and one to the low state, rather than doing clear and write serial in time. The second departure was to prevent writing either transistor to saturation, which would prevent subsequent reversal of state with a one microsecond pulse. This was to be done by a compare of data to be written with data stored and then inhibit of write if the desired bit was already stored. These and other features of design are shown below:

- Balanced memory device pair per bit
- Simultaneous write of high and low state in memory device pair
- Saturated writing prevented by data comparator
- A single, 1 microsecond write period
- Column decoding - one detection circuit per input/output bit
- Row driver provides full 30V write signals to memory devices
- Write voltages not affected by threshold voltage shift

The differential write sequence with compare before write is listed below:

- Read out data stored (100 ns)
- Compare with input data (50 ns)
- If same inhibit write
- If different change state of column detection circuit
- Apply memory write voltage (1  $\mu$ sec)
- State of both memory transistors reversed

Note: For rewrite of data stored, the inhibit mode is deactivated.

Other design goals were added at the beginning. One was to limit the voltage swing of all inputs to a 10 to 12 V CMOS logic compatible signal swing, and to design for most inputs to swing between ground and +12V. Another was three-state outputs for application on memory buss organizations.

The circuitry chosen to implement the differential write with compare feature was CMOS, using p- and n-channel enhancement mode transistors (PEMT and NEMT), both low voltage and high voltage structures. To meet the radiation requirement, fabrication was on SOS wafers, hence MNOS-CMOS/SOS.

### 3.2.2 Layout Design Rules

The mask design rules for the TSM were substantially the same as those used for the PSM. Refer to subsection 3.1.2 for the salient rules.

### 3.2.3 Test Pattern

In order to meet the process and electrical evaluation objectives of the TSM, a test pattern was designed, fabricated and tested. For uniformity of test results and for economy of design effort, the PSM test pattern 6013T was also used for the TSM. The only exception to the description given for the PSM test pattern in paragraphs 3.1.3.1 and 3.1.3.2 was that the n-channel depletion mode transistors (NDMT) described therein become enhancement (NEMT) and some channel lengths were reduced. These changes result from a change in two mask levels to shorten channel lengths, omission of one mask level, and use of the TSM process sequence.

### 3.2.4 Test Vehicles and Results

A Temporary Store test vehicle was designed, fabricated and tested to substantiate the feasibility of the proposed differential write and compare method of operation. To obtain early confirmation, while the design of the IC TSTV was progressing, a breadboard simulator was quickly designed, built and used to test pairs of memory transistors in this mode of operation. In the paragraphs that follow, the breadboard and the test vehicle are described.

#### 3.2.4.1 TSM Breadboard Simulator

A breadboard circuit was designed, built and used to verify the technique of differential write done simultaneously on the pair of memory transistors representing each bit of stored data in the TSM device. It used MNOS transistors from the 6003T test pattern on the PSM Test Vehicle wafers. Two other MOS transistors from test patterns were used in combination with bipolar transistors and integrated circuits to provide the necessary timing, drive, and sensing. A block diagram of this simulator is shown in figure 3.66 and a schematic with voltages for each of the four steps in the test sequence is shown in figure 3.67.

Test results showed an acceptable memory window with the short 1.0 microsecond write pulse. After 60 Read cycles, the memory window was approaching a steady value of 2 volts, as shown in figure 3.68. Testing continued using 6003T MNOS transistors to evaluate process variables for this fast-write application.

#### 3.2.4.2 Temporary Store Test Vehicles (TSTV)

The 6006 and 6008 Temporary Store Test Vehicles (TSTV) are high speed, radiation hard, random access, nonvolatile memories organized to access eight 1-bit words and designed to simulate a larger 256-word by 2-bit Temporary Store Memory. In order to simulate junction leakage and capacitive loading encountered in the LSIC array, the TSTV incorporates a 32-row by 4-column memory transistor array (32-word by 2-bit array). All inputs to the TSTV are CMOS levels with necessary buffers and decoding included on-chip (except for DI and Y select signals which are unbuffered on the test vehicle but will be CMOS buffered in the LSIC array)

The TSTV is built on silicon on sapphire using n-channel deep depletion mode (load) devices and p-channel enhancement mode devices. The memory array utilizes drain-source protected MNOS devices for nonvolatile information storage.

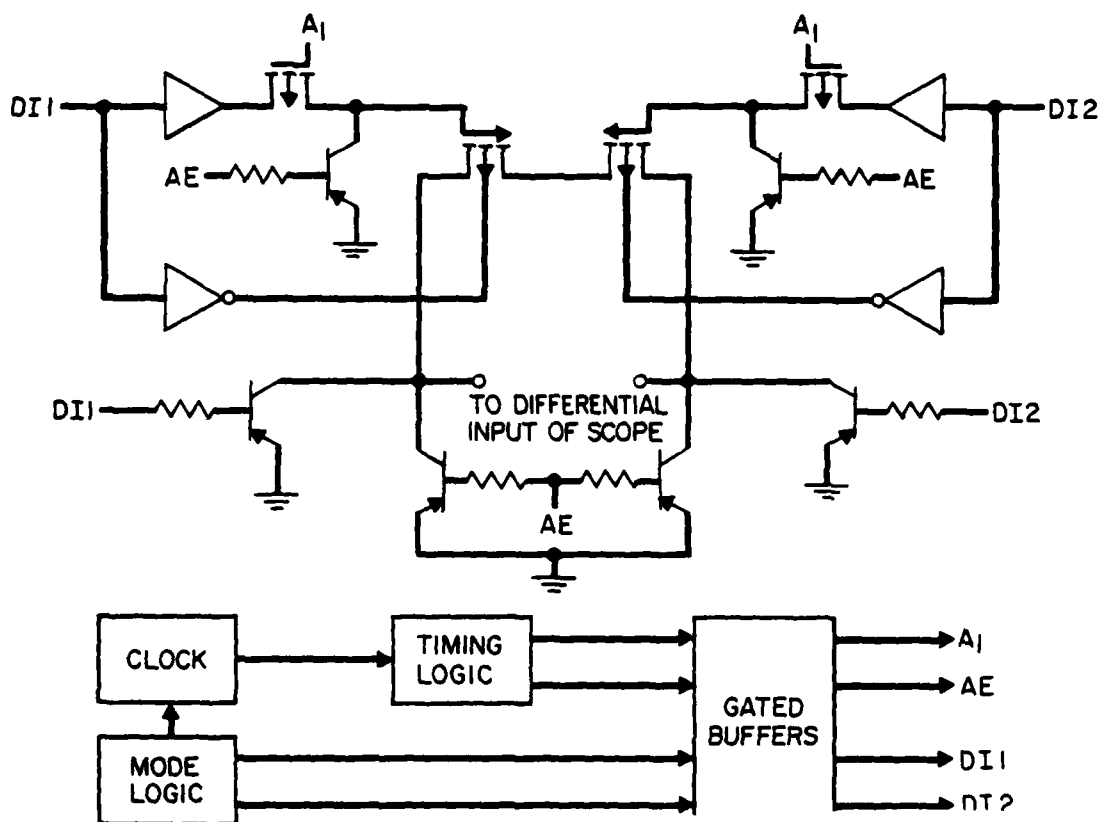


FIGURE 3.66 BLOCK DIAGRAM OF TSM BREADBOARD SIMULATOR

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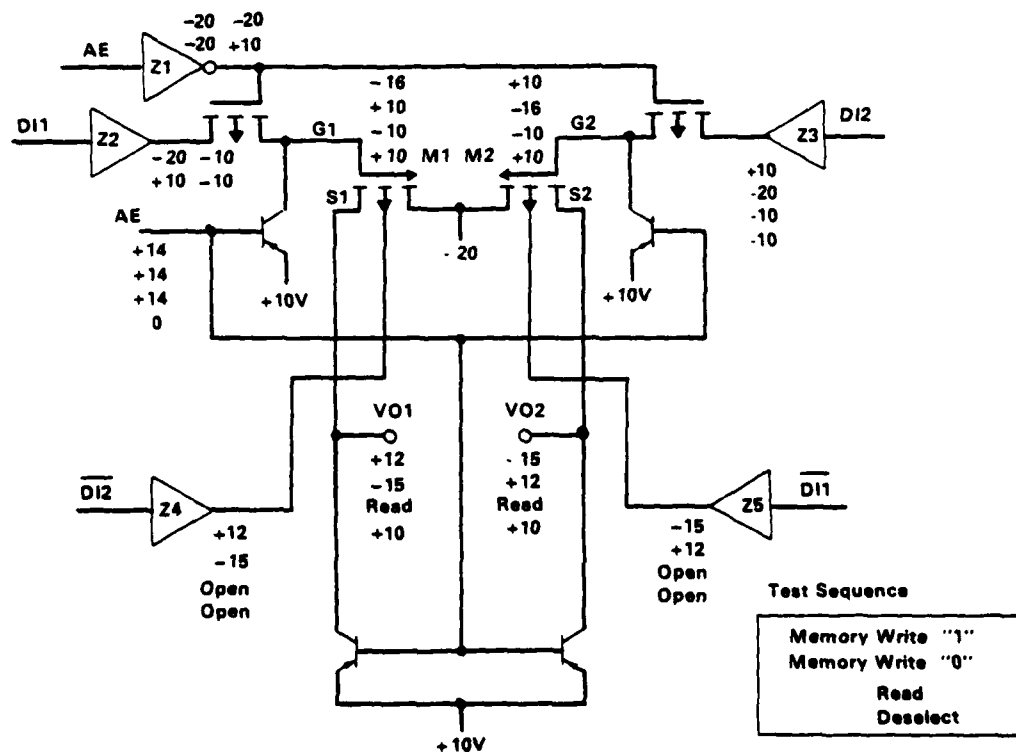
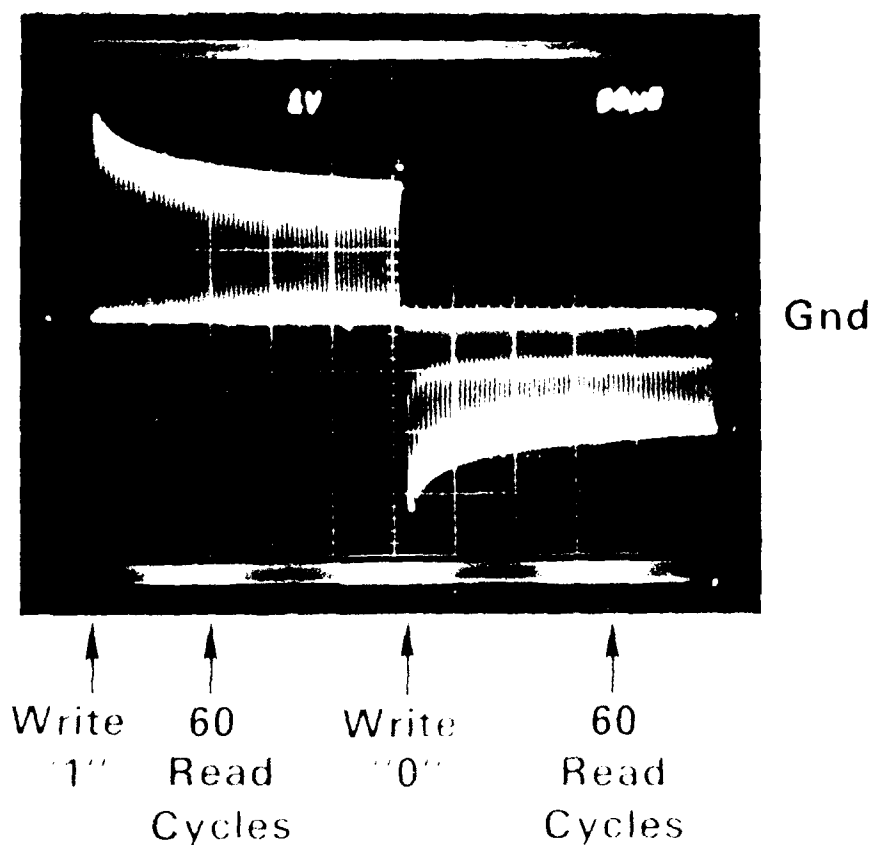


FIGURE 3.67 TSM BREADBOARD

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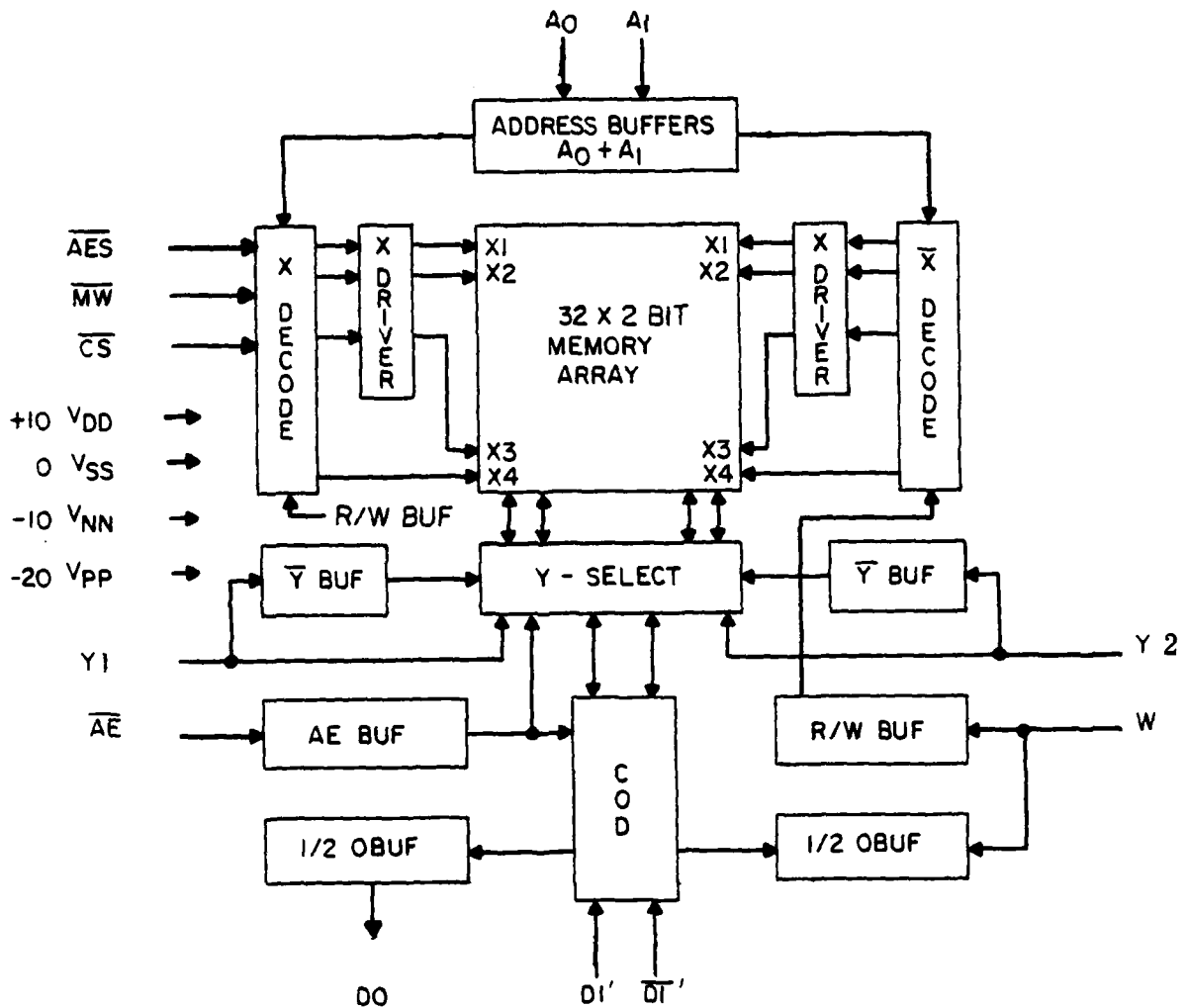


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FIGURE 3.68 MEMORY SOURCE VOLTAGE DIFFERENCE (V01-V02)

A simplified block diagram of the TSTV is shown in figure 3.69. All logic inputs are 10 volt CMOS levels except for DI,  $\overline{\text{DI}}$ , Y1, and Y2 which swing between +10 volts and -20 volts. Control buffers (AE, R/W, and Address) are included to generate internal control and timing signals. The circuit used for these buffers incorporates capacitive level shifting to allow push-pull operation using the n-channel depletion mode device.

The buffer is also chip select addressable so that when the chip is deselected only standby power is drawn.



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FIGURE 3.69 BLOCK DIAGRAM OF TSMTV

The I/O section of the TSTV is noninverting. A 3-state output buffer (O-BUF) is included on-chip and is designed to drive an output load of 30 pf.

A column detection circuit (COD) is provided for the one output bit. This circuit is a PMOS cross-coupled flip-flop which latches the data stored in the memory array during the read mode. The 6008 has a different COD intended to improve sensitivity and access time.

The memory array portion of the TSTV utilizes two drain-source protected memory FET's per bit and is designed to help predict the performance of the 256-word by 2-bit Temporary Store Memory. (The test vehicle array layout is 32 rows by 4 columns and the proposed layout of the larger array is 32 rows by 16 columns.) The differential read/write feature resulting from the two MNOS FET/bit configuration aids detection, making this circuit quite suitable for use in a radiation environment.

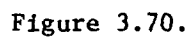
The two top rows of the TSTV memory array (which are geographically and electrically farthest from the detection circuitry) are decoded or accessed. For comparison, the two bottom rows of the array are also decoded. The other 28 rows of devices are held in the "OFF" state and used to simulate the actual junction and gate overlap capacitance which will be encountered in the larger array. In addition, the four rows which are accessed are loaded with additional capacitance, in the form of a buffer test point, which simulates the other 12 columns of the larger array. The metal interconnect pattern is shown in figure 3.70.

The X-decoder is a binary decode tree used to access the four addressed rows. Also included on each addressed row is an X-driver which greatly improves the speed of the decoder and also allows a maximum write voltage ( $\sim 30V$ ) to be applied to the memory gate during the write mode. This will provide for maximum threshold voltage shift of the MNOS device for the 1  $\mu$ sec short write cycles.

The buffered test points (not shown on block diagram) which have been included on the addressed rows of the memory consist of a p and n-channel pair operating push pull. These test points allow monitoring of the X-lines of the memory.

Additional test structures (not shown on block diagram) are included on chip which provide an indication of process variations and operation of individual elements. These structures include memory and nonmemory capacitors and transistors. The features of the TSTV are summarized here:

- Decoder cells
- I/O buffer cells
- Differential write MNOS memory cell arrays
- Buffered internal test points
- Drain-source protected P-channel MNOS transistors
- Depletion mode N-channel transistors
- Depletion mode CMOS cells
- In-line process control cells on test pattern



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**3-96**

Testing of 6006 wafers was accomplished on the Macrodata MD-154. Functional parts were identified for packaging to facilitate more thorough testing. Fast write performance with write pulse widths down to  $1.0 \mu\text{s}$  was obtained.

Test patterns from 6006 wafers were packaged and tested for radiation, total dose. Test transistors from 6006 and 6003 wafers were packaged and subjected to endurance stress. Subsequent testing with a Single Pulse Reversal Retention program have shown retention to well beyond 48 hours with  $10^8$  data reversals. Figure 3.71 shows retention extrapolated to beyond 48 hours ( $1.73 \times 10^5$  sec is 48 hours) for  $10^9$  data reversals.

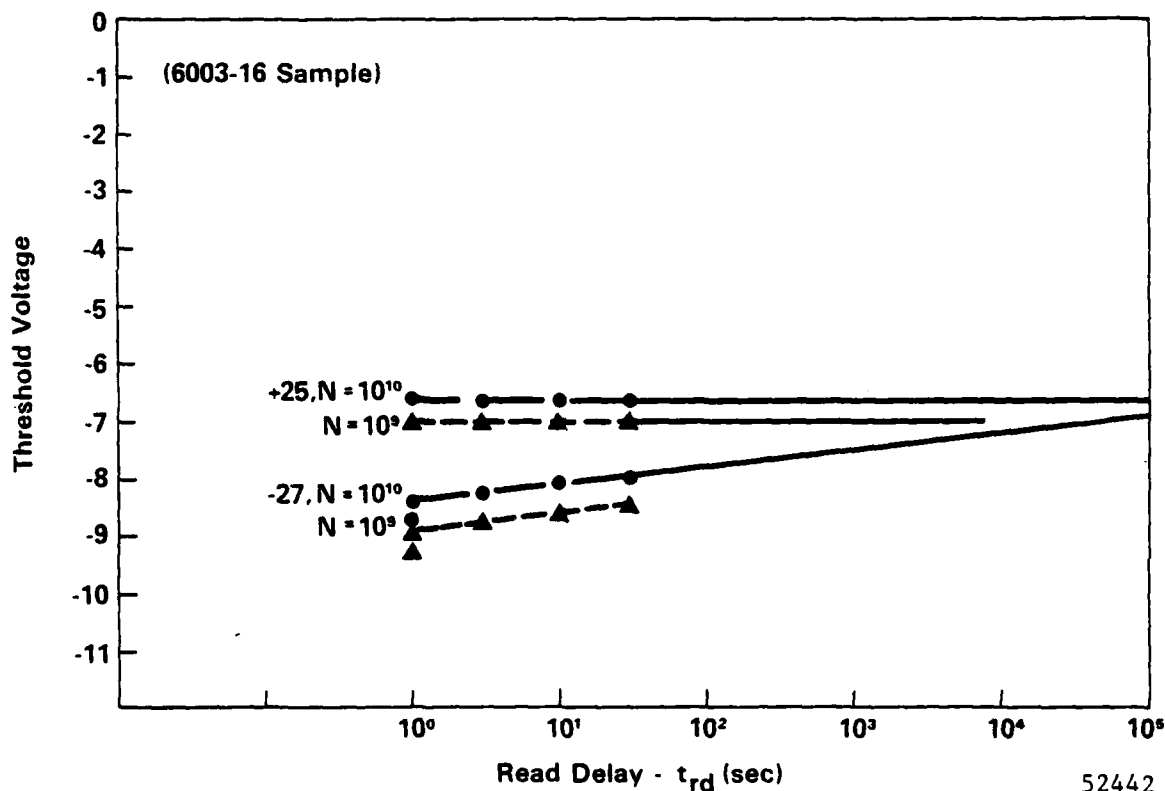


Figure 3.71. Single Pulse Reversal Retention (Pulse Width =  $1 \mu\text{sec}$ )

### 3.2.4.3 Test Vehicle Summary

In summary, both the TSM breadboard simulator and the TSTV provided hardware verification that the design approach was feasible. Simultaneous write of each transistor of the pair in a memory bit to an opposite threshold state was accomplished. Further, this differential write was executed or inhibited correctly as a result of the comparison of input data with stored data. Writing with  $1.0 \mu\text{s}$  pulses was shown to provide sufficient window for the desired retention time, verifying the MNOS process capability for fast-write performance. With the successful demonstration of this novel design approach, effort progressed to the design of the large scale integrated TSM device.

## 3.2.5 TSM 6012 LSIC Design

The TSM LSIC evolved as a 512 x 1 nonvolatile RAM with a block diagram as drawn in figure 3.72. It is packaged in a 40 pin DIP and the numbers on the block diagram indicate the DIP pin numbers. Initially the goal was to organize the chip as 256 x 2 but this would have required duplication of the row and column selection networks. After initial cell layout it became obvious that the 256 x 2 organization would give too large a chip size. A chip layout diagram is shown in figure 3.73.

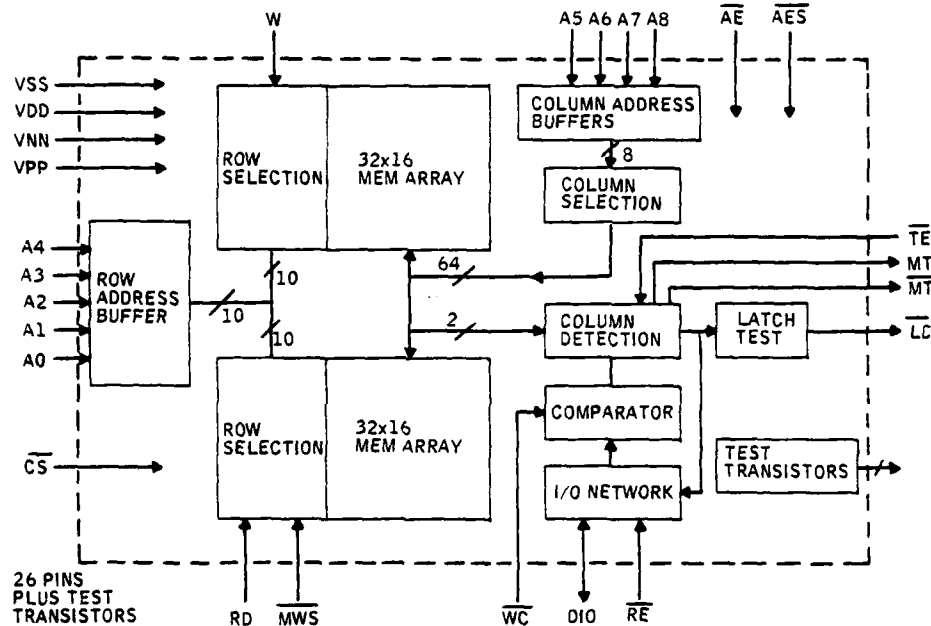


Figure 3.72. TSM: 512 x 1 Simplified Block Diagram MNOS/SOS

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From the block diagram and chip layout it can be seen that the memory array is physically separated into two mirrored halves. There are two transistors per bit with one transistor located in one of the halves and the other transistor in the other half. There are also two identical row selection networks. This separation resulted because the simultaneous write of the two memory transistors to opposite states requires propagating data to one memory transistor and data complement to the other transistor. There are 32 body buffers, even though only 2 are active during any cycle, to avoid threshold voltage drops. The full supply voltage is used for writing, no thresholds drops are suffered in the decode networks.

## 3.2.5.1 Design Approach

In the early design stages of the TSM LSIC, several crucial design decisions had to be made. One was the decision to do a compare before write whenever data was to be written into the memory. This is a consequence of the short write time (1  $\mu$ sec). This means that each write cycle begins with a read-compare during which stored data is compared with input data and an actual write internal to the chip occurs only if stored data and input data are different. This prevents multiple writes of the same data into any memory location, which might then preclude reversing the data in a subsequent single 1  $\mu$ sec write.

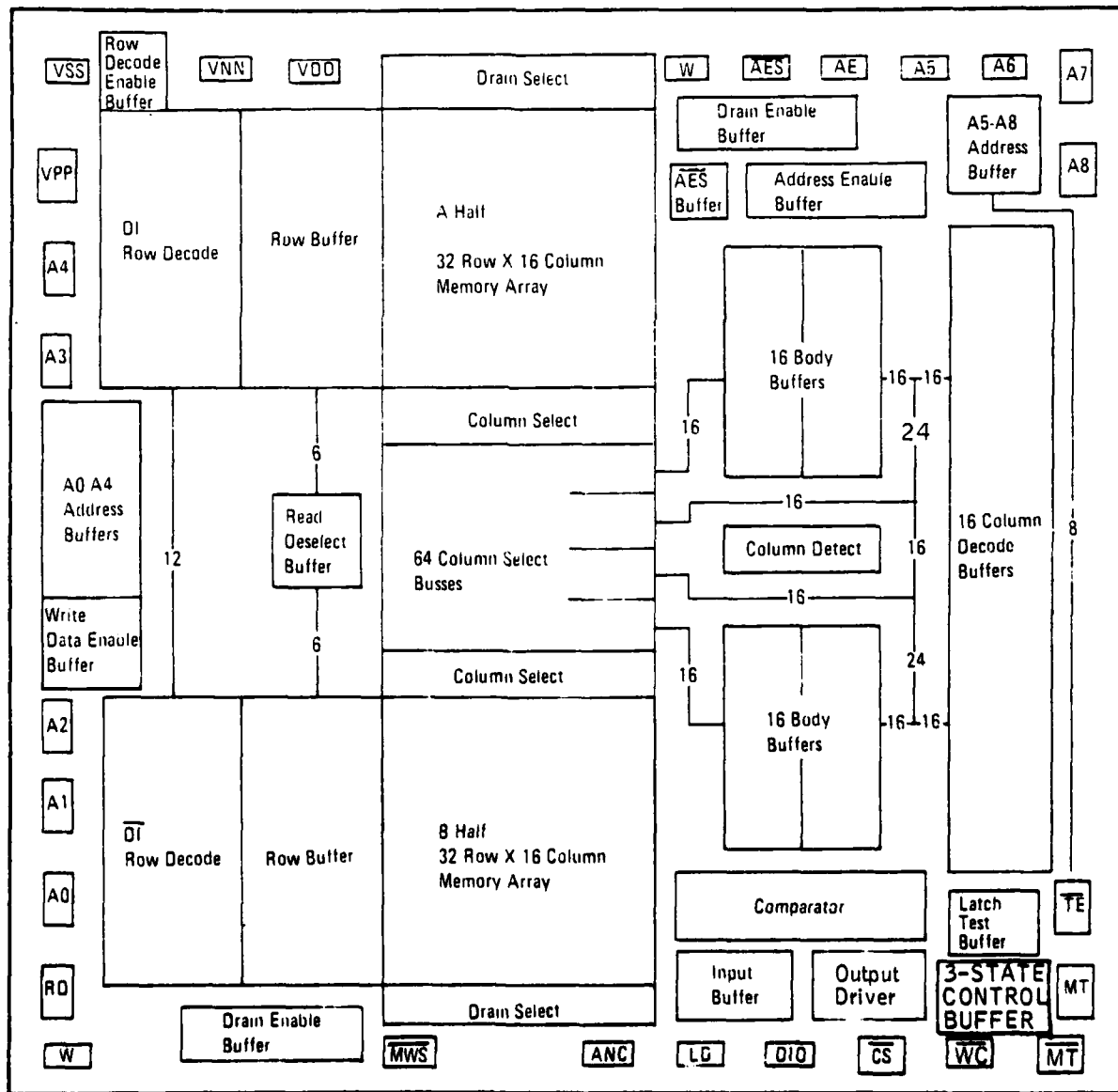


Figure 3.73. TSM: Layout Diagram

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Another consequence of the short write time was the decision to use a source follower type detection circuit where each memory transistor (two memory transistors per bit) drives a purely capacitive load. The detection circuit used is a modified cross-coupled NOR gate pair. This avoids read enhancement of the low conductance state such as occurs (and is often desirable) in EAROM type MNOS memories which use a simple cross-coupled transistor pair. Read enhancement is undesirable on the fast-write TSM because data would be enhanced by repeated reads to the point where the data would be difficult or impossible to reverse with a subsequent 1  $\mu$ sec write.

Another decision that was made was to do a simultaneous write of each memory transistor to opposite state rather than have a separate clear cycle followed by a write. The SOS technology readily allows isolation of the memory columns, which lends itself very well to the simultaneous write. The separate clear would add to cycle time and is more appropriate to bulk silicon or EAROM designs.

Considerable on-chip logic is required to implement the design. As a result high voltage CMOS/SOS technology is used on the TSM-LSIC to keep the power at an acceptable level. This is a departure from the 6006 test vehicle which used n-channel depletion loads and p-channel enhancement mode devices to demonstrate the MNOS-RAM concepts. For a detailed discussion of transistor models and the design techniques used see the "Report of Design and Simulation HVC MOS-MNOS/SOS Temporary Store Memory" dated 28 May 1976. The method of circuit simulation used for the TSM is the same as that described for the PSM, in sections 3.1.5.1 and 3.1.5.2 above.

### 3.2.5.2 Unique Features

The functions of most of the device pins can be understood from the preliminary specification which is included in this report.

Two unique features need some explanation, however. One is the memory test feature which allows measurement of the memory window or threshold difference between the two memory transistors. To use this feature the  $\overline{TE}$  signal is tied to the  $V_{pp}$  level. This enables observing the two waveforms at the MT &  $\overline{MT}$  terminals. During a read cycle the two waveforms present are the source follower waveforms from the two transistors for the particular bit being addressed. The difference in final value between these two waveforms can be observed on an oscilloscope and represents the threshold voltage difference for this bit. Every bit in the memory can be measured in this way. By measuring this difference immediately after writing and then again at selected intervals thereafter, the retention slope of the memory transistors can be determined.

Another unique feature is the restore feature which is enabled and disabled by the  $\overline{RE}$ . When  $\overline{RE}$  is at  $V_{ss}$  the restore feature is enabled. With restore enabled the internal circuitry and logic determines whether the internal memory window is above some minimum value. If during a write cycle stored

data equals input data and the window is below minimum, a write will be enabled and the window restored. This is accomplished by placing a controlled imbalance on the detection circuit which the memory devices must overcome. This imbalance can only be overcome if the  $\Delta V_T$  of the memory transistors is above the minimum.

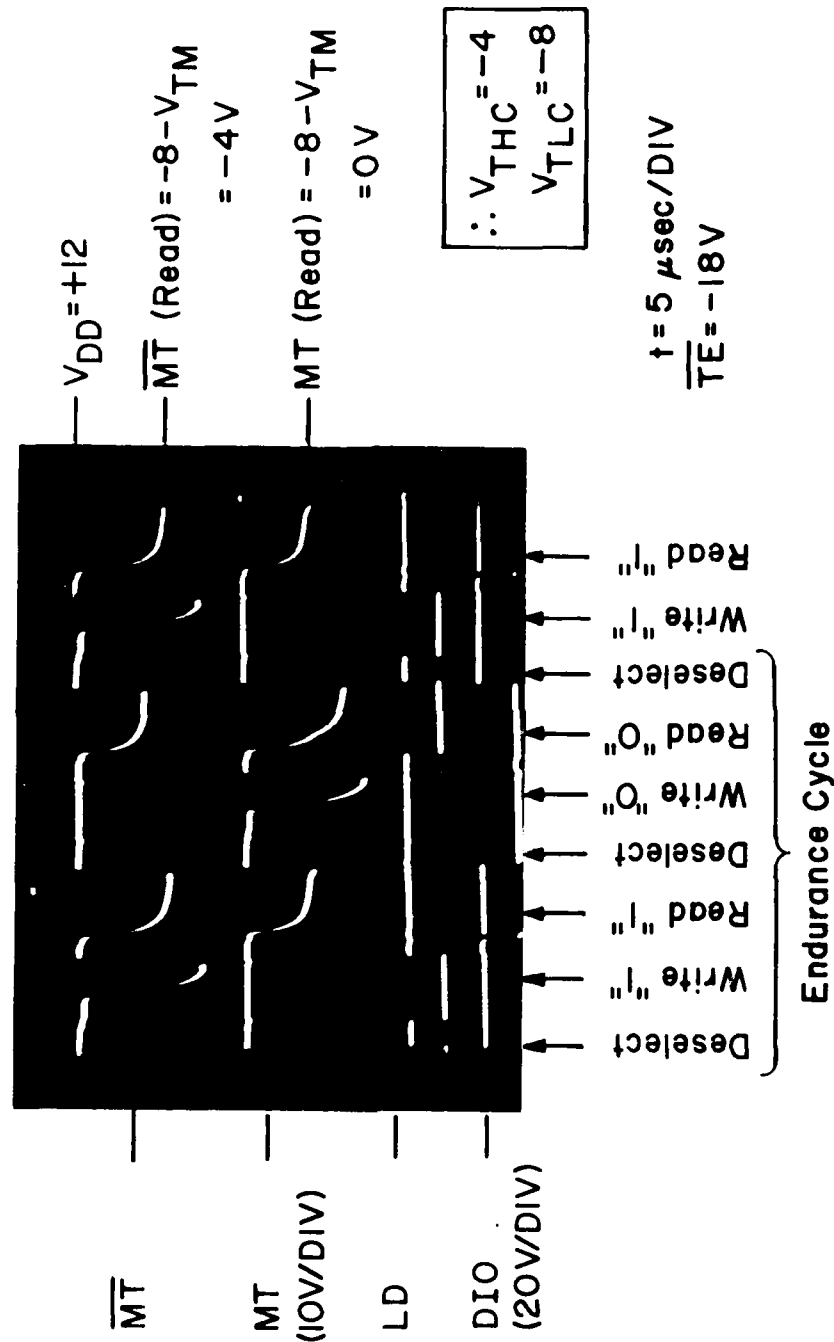
### 3.2.6 TSM 6012 Test Results

The TSM LSIC design has been implemented in two mask series: the original design designated the 6012 and one design revision designated the 6024. After initial debugging of the mask set the performance of the 6012 was thoroughly evaluated and tested before the design revisions were made.

#### 3.2.6.1 Memory Window Measurements

Figure 3.74 shows the waveforms which demonstrate the basic operation of the chip. This is an oscilloscope photograph of the waveforms for 1 bit (one address) taken while the device was continuously cycling on the TSM Laboratory Test Set. The mode is a test mode where the memory test feature is enabled and the test set is in a write/read mode. The data pattern is an endurance pattern which means that the data reverses with each write cycle. Therefore the cycle is as illustrated in the figure: a write/read of an alternating data pattern with a deselect or reset between each read or write.

# 6012 TSM: Memory Window Measurement and Latch Detect vs DIO Functions



52372

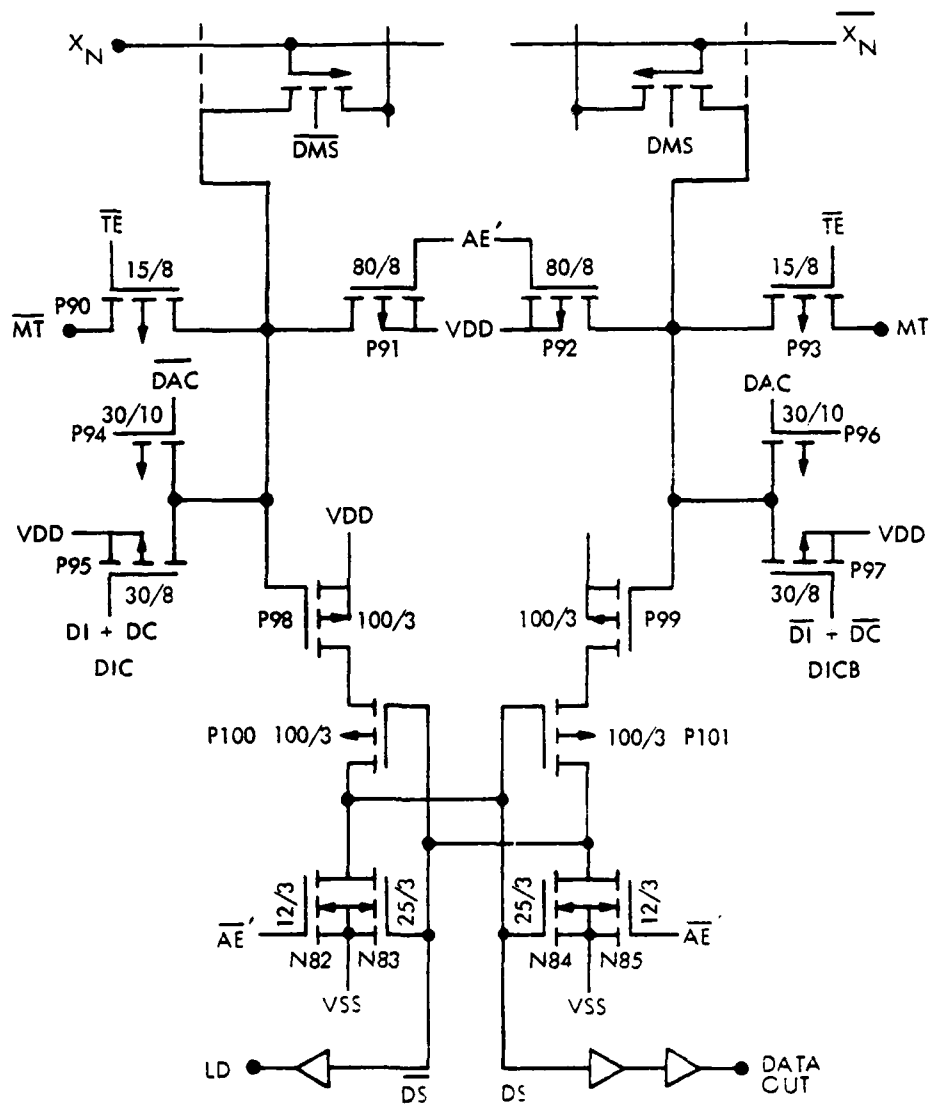
The top two waveforms in the figure are the MT and  $\overline{MT}$  waveforms. During the read portion the difference in final values is the memory window. During the write portion one of these waveforms is clamped to  $V_{DD}$  while the other is driven negative toward  $V_{pp}$ . The side that's clamped to  $V_{DD}$  corresponds to the memory transistor whose gate is driven to  $V_{pp}$  and is being written to the low conductance state. The side that's driven negative corresponds to the memory transistor whose gate is at  $V_{DD}$  and whose body (and therefore source and drain) is driven to  $V_{pp}$  and is being written to the high conductance state. The LD (latch detect) waveform is another test waveform which displays the stored data. The DIO waveform is the data which is driven by the input data (the test set or other data source) during write and by the internal output data buffer during read. During each write cycle this mode of the test set guarantees input data not equal to stored data, which enables a write. With these four waveforms the operation of the chip is verified and the size of the memory window measured a few microseconds after being written.

Figure 3.75 shows the column detection circuit which supplies these waveforms.  $X_N$  and  $\overline{X}_N$  are the addressed (row) memory gates corresponding to one bit. Transistors P98 through P101 and N82 through N85 comprise the modified crosscoupled NOR detection circuit. Transistors P90 and P93 comprise the memory test feature; P91 and P92 are reset transistors. P94 and P96 are p-channel varactors which add the imbalance for the restore feature and P95 and P97 are the input data devices for writing. Not shown is the low voltage CMOS logic which supplies the control signals for this circuit and the column decode network which selects one of 16 columns of memory.

The 6012 has been characterized with respect to the memory window size and retention. For a 1  $\mu$ sec write pulse width, figures 3.76 and 3.77 give the memory window as a function of time for a stored "1" and a stored "0". This data was taken on a sample of parts after  $10^8$  write reversals. The spread in predicted retention is from several hours to several days. The first data point was taken 3  $\mu$ sec after writing. The next convenient measurement point was ten seconds, then 100 seconds, then 1000 seconds. These measurements were single sweep read mode measurements made with the laboratory test set and a storage oscilloscope. With an optimized memory dielectric the retention can be improved. The two retention slopes indicated represent the spread in slope that was observed.

### 3.2.6.2 Detection Measurements

From the testing of the 6012 it was soon learned that data retention as measured at the DIO port was very short (minutes) and therefore inconsistent with measurements made of the memory window. This was due to the manner in which the detect circuit was being timed.



52446

FIGURE 3.75 COLUMN DETECTION CIRCUIT

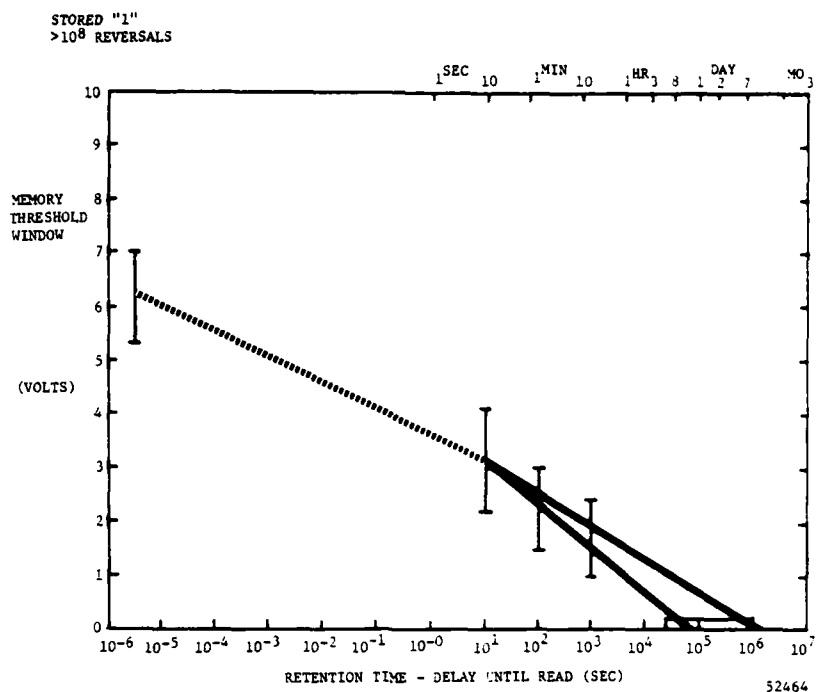


FIGURE 3.76 TSM: RETENTION FOR FAST-WRITE MNOS  
WRITE PULSE WIDTH 1.0  $\mu$ s, VOLTAGE 30.V

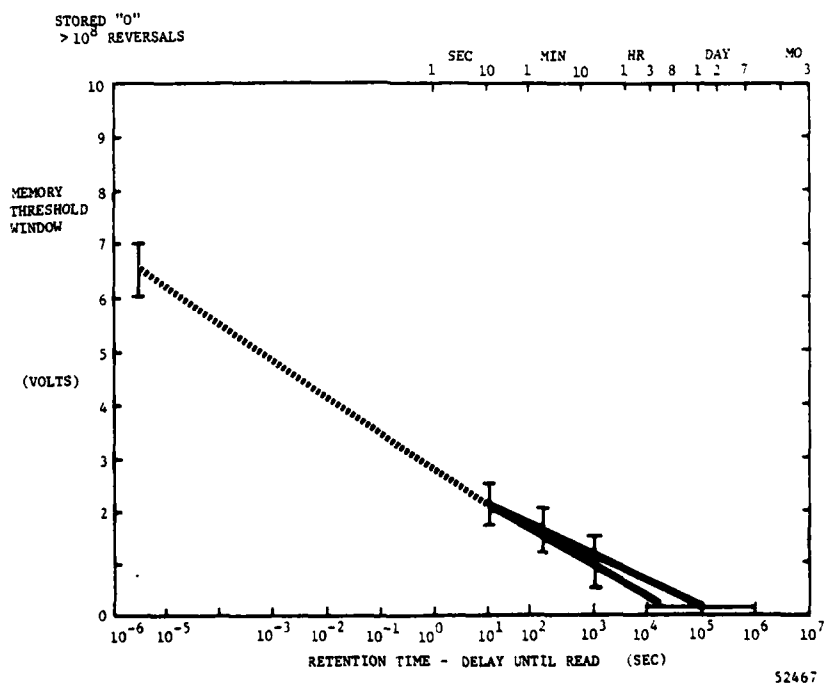
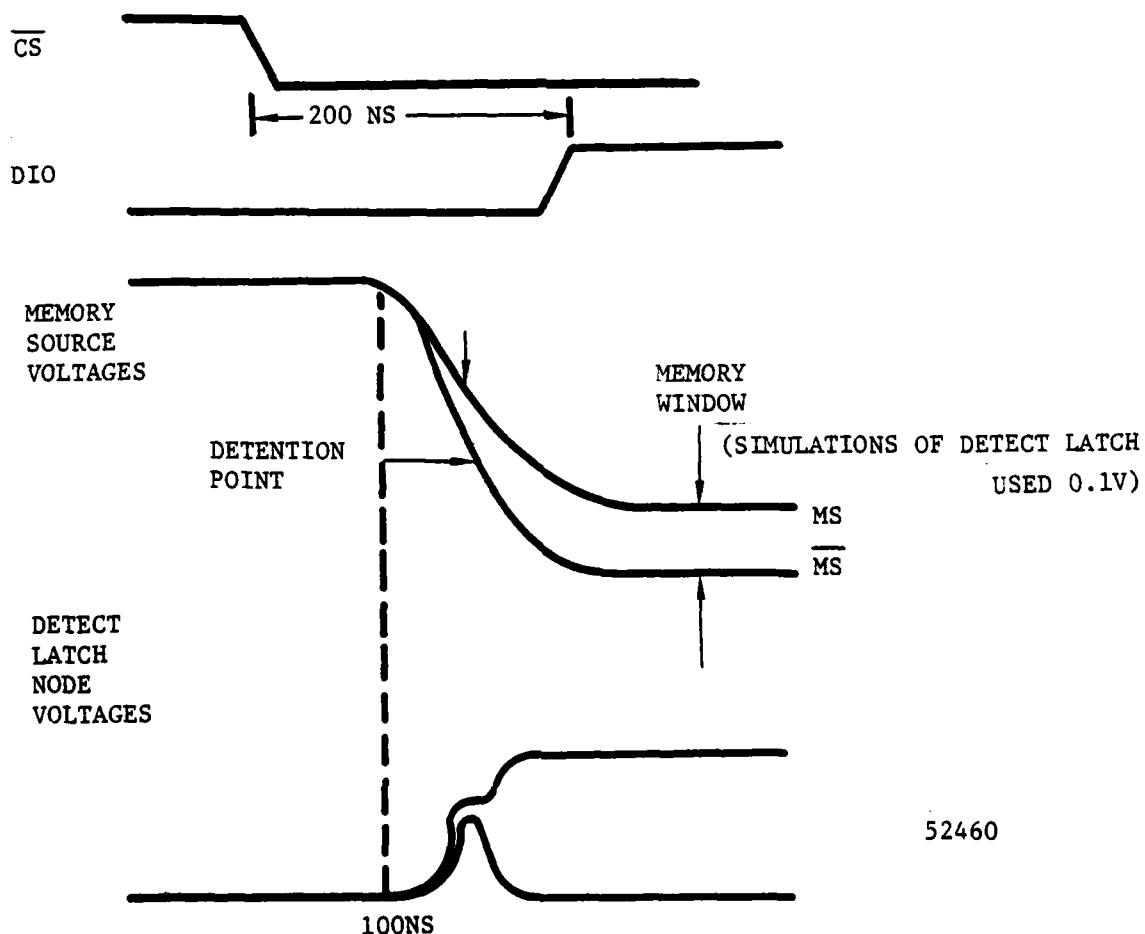


FIGURE 3.77. RETENTION FOR FAST-WRITE MNOS WRITE  
PULSE WIDTH 1.0 $\mu$ s, VOLTAGE 30V.

Figure 3.78 shows the  $\overline{CS}$  and  $\overline{DIO}$  waveforms at the beginning of a read cycle. The two waveforms  $\overline{DMS}$  and  $\overline{DMS}$  are the internal decoded memory source waveforms which correspond to MT and  $\overline{MT}$ . Notice that the detection point, i.e., the point at which the detection circuit makes its decision, is located in time at a point where the  $\overline{DMS}$  and  $\overline{DMS}$  waveforms are still changing. Also, notice that the maximum difference (memory window) is not developed until later in time. It was concluded that with a 1  $\mu$ sec write after several minutes the early difference between the two waveforms became too small to detect even though a significant memory window remained. This is because the initial voltage difference is due primarily to the difference in source current between the two memory transistors as they drive the two equal capacitances on the detection nodes. Later, as the source follower action nears completion and the source currents decrease, the difference is due to the difference in threshold voltage between the two memory transistors. From this it became apparent that if detection were delayed somewhat the memory window could be detected and the data retention would approach the window retention.



52460

FIGURE 3.78 TSM: DETECTION PROCESS/MEMORY WINDOW

In addition to the detect circuit timing there were certain other timing margins and minor control logic situations which needed improvement. As a result of this analysis a design iteration was done; the resulting revised masks series is numbered the 6024. The following sections discuss the 6024 design and test results.

### 3.2.6.3 Fabrication of TSM 6012

Six lots were run with the TSM 6012 mask set. These permitted diagnostic test of the first lot and subsequent lots and introduction of corrections and improvements to the design. Most lots provided about 20 dice which displayed significant functionality. Over all, the lots gave a 5% yield of partially and fully functional dice at wafer test. The test results from these lots are summarized here:

#### TSM STATUS

- Wafer test yield - 5% show some function
- Packaged parts from lot 3459 (corrected mask set and timing):
  - 5 fully functional for 8  $\mu$ sec write pulse
  - 2 fully functional for 1  $\mu$ sec write pulse
  - and 21 partially functional
- Retention at data output: greater than 24 hours for 8  $\mu$ sec  
about 1 minute for 1  $\mu$ sec
- Retention by memory window measurement:
  - 2 hours to 8 days for 1  $\mu$ sec
- Modification of detection timing and circuitry is necessary
- Total dose tests indicate both low and high voltage CMOS/SOS address and decode circuits will operate through 2Y

This fabrication and test activity on the TSM 6012 gave further verification beyond the test vehicle data for the feasibility of this approach to fast-write, nonvolatile memory. A sufficient quantity of LSIC parts were produced to demonstrate that fast-write memory arrays could be designed and built. Careful and thorough testing revealed the problems and clarified the needed changes. This activity established the foundation for a next step, a design modification with clearly understood goals and reasonable expectation of success.

## 3.2.7 6024 LSIC Design Modification

The following list summarizes the changes to the original 6012 incorporated into the 6024.

- 1) Delayed RD signal has been incorporated by an on-chip R-C network.
- 2) Timing signal for the row Decode Enable buffer has been changed from CSB to AEBP to eliminate a timing conflict.
- 3)  $\overline{\text{MWS}}$  line has been re-routed to eliminate series resistance.
- 4) Input buffer has been redesigned to allow broadcast of RD signal.
- 5) Column detection latch has been redesigned with new device sizes and with delayed control signals to optimize detection.
- 6) New input protect networks identical to the new networks on the PSM were incorporated. The output protect network was changed to be nearly the same as the new networks on the PSM.
- 7) Power supply crossunder resistances were minimized, especially in paths to input protection networks.
- 8) A high voltage input protect was used for Test Enable (TE) to allow more accurate measurement of memory array threshold voltages.

The first two changes improve timing margins in the row buffer and row decode enable buffer. The timing situation is illustrated by the row decode enable buffer schematic shown in figure 3.79. This buffer illustrates the level shifting circuits which are used extensively on the TSM. The inputs CS, W, and AES are CMOS swings ( $V_{DD}$  to  $V_{SS}$  for CS and W,  $V_{NN}$  to  $V_{PP}$  for AES).

The output is an internal signal  $W'_X$  which is required to have a  $V_{DD}$  to  $V_{PP}$  swing (nominally 30 volts). The circuit works by precharging the gates of P65 and N56 thru N53 and N55 respectively during the deselect period. This corresponds to N53, N55 on and P63 off. At the beginning of a cycle AES switches low turning N53 off; N55 is also supposed to go off and then CS switches low turning P63 on. Let's assume W is low keeping P64 on and N54 off. As CS switches low the gate of P65 goes negative turning P65 on and N65 off by coupling thru the capacitor C1. The output signal  $W'_X$  then switches from  $V_{DD}$  to  $V_{PP}$ .

In this circuit the gate of N55 is driven by an internal signal CS + RD which is somewhat delayed from CS. This means that N55 is "slow" going off compared to CS switching negative. Under certain conditions this circuit has failed to operate because the full voltage swing cannot be coupled thru C1 to the gate of N56 if N55 is partially on. The solution to this is to delay P63 coming on by driving its gate with a delayed internal signal AE which is logically equivalent to CS. A similar situation existed in the row buffer and is corrected by delaying RD internally. The margins were poorest at the lower p-channel threshold present before radiation. The margins actually improve post radiation due to the higher p-channel thresholds since this delays the p-channels turning on.

Changes 3, 4, 6, 7, and 8 in the foregoing list are generally self explanatory. These are refinements that were not absolutely necessary but were done because they are desirable and convenient to make since other changes to the mask set were being made anyway.

Change number 5 in the list was necessary in order to provide data retention consistent with the memory window. In figure 3.75 of the previous section the AE' signal has been separated and renamed DE (detection enable). Independent control of this signal combined with an increase in size of N82 and N85 allows delaying the setting of the detect latch until a greater voltage difference develops on the gates of P98 and P99 during read. Latch transistor sizes were changed to increase sensitivity and to allow more control in delaying detection. An inverter pair with capacitor was added to internally delay the DE signal. Additional delay can be achieved by controlling the DE signal from an external pad. This

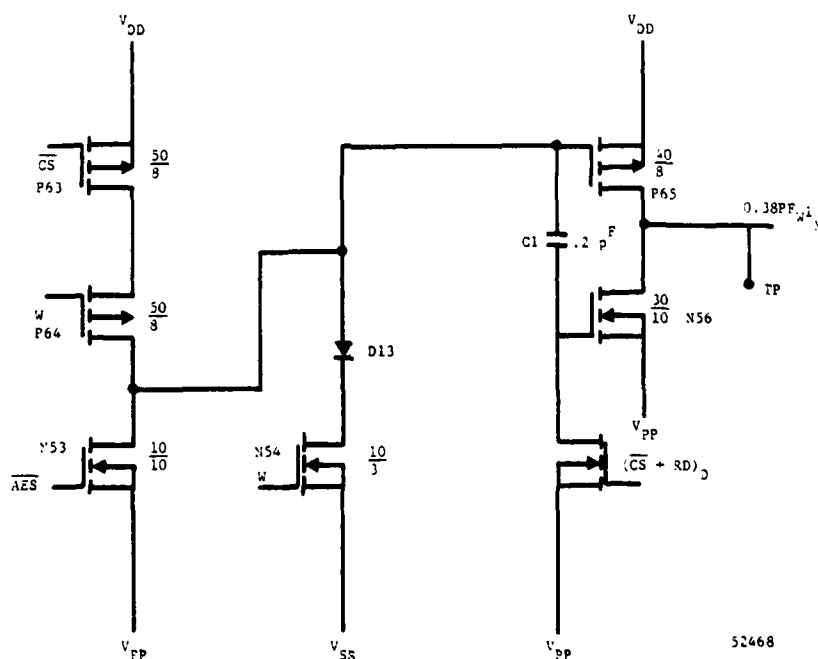


FIGURE 3.79 LOW DECODE ENABLE BUFFER

pad is located at the chip periphery and has an input protection network incorporated. Another inverter pair and capacitor was added to delay the release of the latch reset signal AE' which drives the gates of P91 and P92. This delay prevents release of the reset signal until current begins to flow thru the memory transistors. As a result the latch nodes are never left floating and are, therefore, less susceptible to transient radiation effects.

Figure 3.80 shows the computer simulation results for the detection circuit. Plotted are the detect latch node voltages (DS & DS in figure 3.75 versus time for three cases corresponding to different transistor widths. Waveforms are shown for the original 6012 design, the modified 6024 design, and a third case. The transistor sizing shown for the 6024 was chosen because of the minimum peak at the set point of the latch for the node that eventually sets to ground. This minimizes the bias on the n-channel transistors and provides more positive setting with minimum delay.

To aid in the evaluation of the detection latch of the TSM, 6012 devices were fabricated with a Detect Enable pad (DE) added to allow independent control of latch timing. The intent was to use DE to hold the latch in the reset mode until a differential voltage indicative of the memory window was

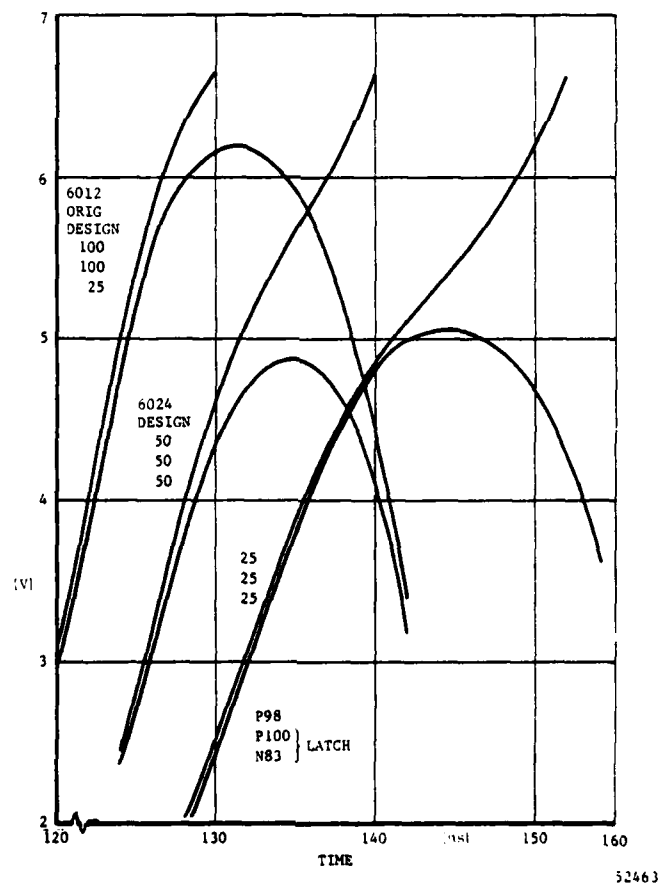


FIGURE 3.80 TSM DETECT LATCH NODE VOLTAGES DS AND  $\overline{DS}$

present at the latch inputs. Tests indicated that under normal operating conditions, the DE signal could only affect a small delay in the latching of the detection circuit. Computer simulation of the circuit verified that only minimal delay could be achieved with present device sizes. In addition to size changes in the DE transistors (N82 & N85), the latch transistors themselves were evaluated (N83, N84, P100 & P101). Table 3.6 shows a summary of results. With the DE transistors N82 & N85 increased in size from 12/3 to 25/3 ( $\mu\text{m}$  length/ $\mu\text{m}$  width of channel) and the p-channel latch transistors (P100 & P101) decreased from 100/3 to either 25/3 or 50/3, the latch can be held reset indefinitely by DE. As the latch transistors decrease in size, detection time and access time increase.

TABLE 3.6 DETECTION SIMULATION RESULTS

TRANSISTOR P98 & 99	WIDTHS P100 & 101	DETECTION* TIME CHANGES	DETECTION VOLTAGES DS      DS	DATA DELAY* REF. TO T1	DESIGN REFERENCE
<u>PRE-RAD, 25<sup>0</sup>C</u>					
100 μm	100 μm	T1 ns	6.20V 6.78V	25 ns	6012
50	50	6	5.64 6.24	39	6024
50	25	13	4.77 5.33	49	
25	25	13.5	5.05 5.64	55	
<u>POST-RAD, 125<sup>0</sup>C</u>					
100	100	40 ns		91 ns	
50	25	61		139	

\*These are delta changes in timing, referenced to T1.

The design modifications to the 6012 to provide the new 6024 mask set are very briefly summarized below. Testing of parts fabricated with this modified mask set has verified the effectiveness of these modifications. Test results are given in section 3.2.10

#### TSM Mask Design Changes

- Deselect the input circuit and comparator to reduce power
- Minimize resistance in MWS path to row buffers
- Replace external detect enable (DE) requirement by an internal delay using two inverters, so that detection is delayed, to improve retention
- Modify column detection circuitry by adjusting transistor channel widths.

### 3.2.8 TSM LSIC Test Equipment and Programs

To test the TSM LSIC in a cost-effective and thorough manner, automated test equipment is highly desirable. At Westinghouse, ATL, two such test systems are available. There are the Macrodata MD-154 and MD-501. The newer model, MD-501, was programmed for testing the TSM in wafer and package form. Both automatic, programmable test systems are described in the PSM section, see paragraphs 3.1.7.1 and 3.1.7.2.

In addition to the MD-501, a laboratory test set of custom design was used extensively for engineering diagnostics and characterization of packaged TSM LSIC parts. It was also used, in conjunction with wafer probe equipment, for some wafer testing when the easy and quick flexibility of the laboratory test set was preferred.

#### 3.2.8.1 TSM Laboratory Test Set

The TSM lab test set shown in figure 3.81 has been used extensively to functionally operate both the original 6012 TSM and the modified 6024 TSM. Write, read and write/read modes may be run for single cycle, continuous or a preset number of cycles. All, single or a preset number of addresses may be cycled in any mode. In the read mode, data comparison can be made. The tester can run continuously indicating a fault or can stop on fault displaying the address of the wrong bit, the proper data and the actual data read at that address. Eight data patterns can be written into the part and used to compare readout. These eight include all ZERO's, all ONE's, alternating 010101..., alternating complement 101010..., endurance 010101... or endurance complement 101010..., and an address verification pattern in a PROM. This pattern is shown in figure 3.82; each row is unique to identify decode errors.

There is also a read test mode. This enables the analog measurement of memory window.

There are many front panel adjustments which facilitate characterization of electrical performance. Adjustments are included for all input signal pulse widths and cycle times for all modes of operation. All supply voltages may be varied several volts for margin testing. Supply current jacks permit monitoring TSM power dissipation in the various modes.

#### 3.2.8.2 TSM LSIC Test Programs

One basic test program was developed to measure parametric and functional performance. Selection was made of certain parts for wafer test. The entire program is intended for package test.

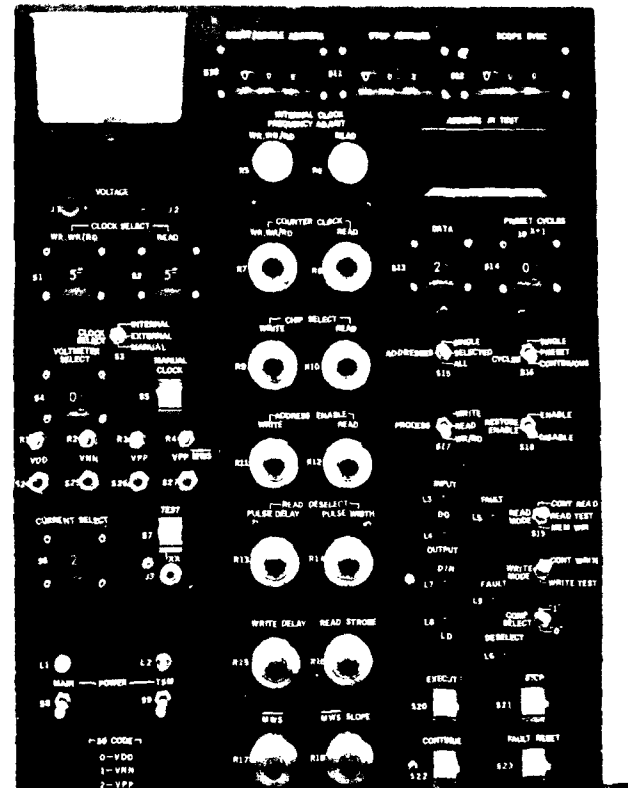
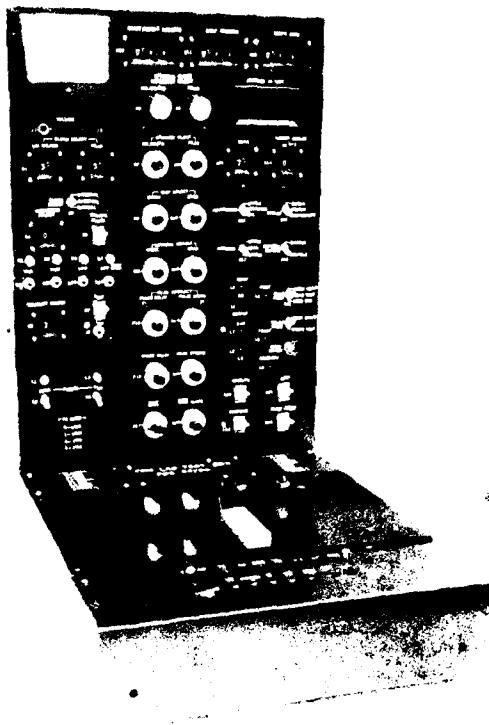


FIGURE A-1

LABORATORY

for the

IBM 6012 AND 6014

PROCESSORS

and writes, frequency, and amplitude of the clock signal, and a number of other functions. The Advanced Technology Corporation

COLUMN															ROW
480	448	416	384	352	320	288	256	224	192	160	128	96	64	32	
1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0
0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	2
0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	3
0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	4
0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	5
0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	6
0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	7
0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	8
0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	9
0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	10
0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	11
0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	12
0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	13
0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	14
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	15
1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	16
1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	17
1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	18
1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	19
1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	20
1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	21
1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	22
1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	23
1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	24
1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	25
1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	26
1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	27
1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	28
1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	29
1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	30
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	31

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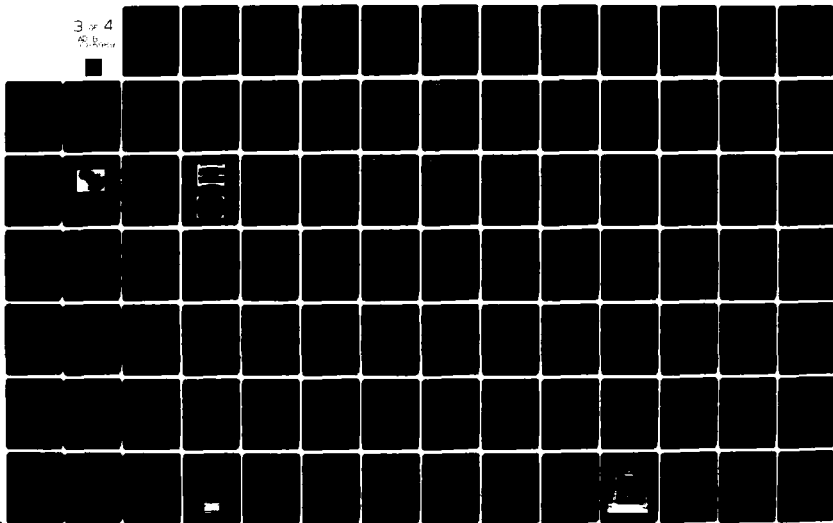
FIGURE 3.82 TSM: TOPOLOGICAL MEMORY MAP STANDARD TEST PATTERN

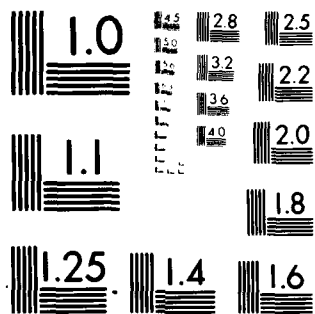
AD-A085 969 NORTHROP CORP PALOS VERDES PENINSULA CALIF ELECTRONICS DIV. F/G 9/2  
ADVANCED COMPUTER TECHNOLOGY-I (ACT I)  
01 MAY 80 F04704-75-C-0006 NL

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MICROCOPY RESOLUTION TEST CHART

NATIONAL BUREAU OF STANDARDS-1963-A

# NORTHROP

Electronics Division

## 3.2.8.2.1 Wafer Test Program

Initially the TSM devices are tested in wafer form on the MD-501, to identify good dice for packaging. The program begins with continuity tests at all inputs, making use of the input protect diode forward current paths to ensure that each probe is in good contact with the bonding pad. There follow a series of threshold voltage (at 10 ua) and leakage current (at 13 or 31 volts) measurements on the test transistors: a memory transistor written to high conductance state by +20V on the gate (gate leakage ILMH, low threshold voltage VTL) and to low conductance state by -20V on the gate (gate leakage ILML, high threshold voltage VTH), and four nonmemory transistors: low voltage p-channel (LVP), low voltage n-channel (LVN) high voltage p (HVP), and high voltage n (HVN). These are shown in figure 3.83, with the continuity tests shown (and passed) on the first two lines. Next the functionality of the TSM-LSIC memory array is checked. This is shown in figure 3.84, for an open socket. It is done in quadrants of 128 bits each. The address verification pattern is written into the first 128 bits, then read and compared with the pattern. Addresses of the first eight bit errors, if any, are printed. This continues through each quadrant and then prints the total number of errors by quadrant. This is repeated with the complement of that pattern (C).

***** 6024 *****			
TEST : CONTINUITY TO VSS & VPP			
TEST : CONTINUITY TO VDD & VNN			
TEST : ILMH			UNITS
ILMH = -.3000001E-02 (0)	ua		TEST TRANSISTOR
TEST : VTL			MEMORY
VTL = -4.62001 (0)	V		
TEST : ILML			
ILML = .2500001E-02 (0)	ua		
TEST : VTH			
VTH = -10.2 (0)	V		
TEST : VTLVP			NONMEMORY
VTLVP = -4.18001 (0)	V		
TEST : VTLVN			
VTLVN = 1.15501 (0)	V		
TEST : VTHVP			
VTHVP = -3.97001 (0)	V		
TEST : VTHVN			
VTHVN = 1.62001 (0)	V		
TEST : ILLVP			
ILLVP = .1 (0)	ua		
TEST : ILLVN			
ILLVN = -.15 (0)	ua		
TEST : ILHVP			
ILHVP = .1 (0)	ua		
TEST : ILHVN			
ILHVN = -.35 (0)	ua		

FIGURE 3.83 TSM WAFER TEST PARAMETRICS

# NORTHROP

Electronics Division

## TEST : ADDRESS VERIFICATION BY QUADRANTS (T)

FAILURE AT ADDRESS = 0  
FAILURE AT ADDRESS = 1  
FAILURE AT ADDRESS = 2  
FAILURE AT ADDRESS = 3  
FAILURE AT ADDRESS = 4  
FAILURE AT ADDRESS = 5  
FAILURE AT ADDRESS = 6  
FAILURE AT ADDRESS = 7  
FAILURE AT ADDRESS = 120  
FAILURE AT ADDRESS = 129  
FAILURE AT ADDRESS = 130  
FAILURE AT ADDRESS = 131  
FAILURE AT ADDRESS = 132  
FAILURE AT ADDRESS = 133  
FAILURE AT ADDRESS = 134  
FAILURE AT ADDRESS = 135  
FAILURE AT ADDRESS = 256  
FAILURE AT ADDRESS = 257  
FAILURE AT ADDRESS = 258  
FAILURE AT ADDRESS = 259  
FAILURE AT ADDRESS = 260  
FAILURE AT ADDRESS = 261  
FAILURE AT ADDRESS = 262  
FAILURE AT ADDRESS = 263  
FAILURE AT ADDRESS = 384  
FAILURE AT ADDRESS = 385  
FAILURE AT ADDRESS = 386  
FAILURE AT ADDRESS = 387  
FAILURE AT ADDRESS = 400  
FAILURE AT ADDRESS = 401  
FAILURE AT ADDRESS = 402  
FAILURE AT ADDRESS = 403

\*\*\* TOTAL FAILURES BY QUADRANT = 64 64 64 64 \*\*\*

## TEST : ADDRESS VERIFICATION BY QUADRANTS (C)

FAILURE AT ADDRESS = 16  
FAILURE AT ADDRESS = 17  
FAILURE AT ADDRESS = 18  
FAILURE AT ADDRESS = 19  
FAILURE AT ADDRESS = 20  
FAILURE AT ADDRESS = 21  
FAILURE AT ADDRESS = 22  
FAILURE AT ADDRESS = 23  
FAILURE AT ADDRESS = 140  
FAILURE AT ADDRESS = 141  
FAILURE AT ADDRESS = 142  
FAILURE AT ADDRESS = 143  
FAILURE AT ADDRESS = 148  
FAILURE AT ADDRESS = 149  
FAILURE AT ADDRESS = 150  
FAILURE AT ADDRESS = 151  
FAILURE AT ADDRESS = 264  
FAILURE AT ADDRESS = 265  
FAILURE AT ADDRESS = 266  
FAILURE AT ADDRESS = 267  
FAILURE AT ADDRESS = 268  
FAILURE AT ADDRESS = 269  
FAILURE AT ADDRESS = 270  
FAILURE AT ADDRESS = 271  
FAILURE AT ADDRESS = 388  
FAILURE AT ADDRESS = 389  
FAILURE AT ADDRESS = 390  
FAILURE AT ADDRESS = 391  
FAILURE AT ADDRESS = 392  
FAILURE AT ADDRESS = 393  
FAILURE AT ADDRESS = 394  
FAILURE AT ADDRESS = 395

\*\*\* TOTAL FAILURES BY QUADRANT = 64 64 64 64 \*\*\*

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FIGURE 3.84 TSM WAFER TEST FUNCTIONAL PRINTOUT EMPTY SOCKET

### 3.2.8.2.2 Package Test Program

The wafer test program above is used for package test when test transistor parametrics and array function are the only tests of interest. A modification of this program especially for packaged array mapping prints the addresses of all bit errors rather than of only the first eight errors. The printout is the same as that shown in the figure, except up to sixteen times longer.

For parametric measurements of the TSM LSIC and access times, the package test program is used. It includes all that was illustrated for the wafer test program. In addition, it includes the following. Leakage is measured at 18 input pins, the input protect diode-resistor characteristics, the DIO buffer leakage in deselected state, and the worst-case (slowest address) access time for each quadrant of memory. A printout of these parametric tests is shown in Figure 3.85.

### 3.2.9 TSM LSIC Radiation Test Results

During the ACT 1 Program, TSM LSIC's and test vehicles were subjected to total dose radiation. These tests were to determine device characteristics and part performance following a radiation event. Inputs were also tested for EMP stress.

#### 3.2.9.1 Total Dose Test Results

Total dose testing was performed on the 6012 TSM LSIC parts. Threshold voltages of the four test transistors in each part were measured before and immediately after each successive total dose exposure. These are low voltage and high voltage structures of p-channel and n-channel enhancement mode transistors (PEMT and NEMT).

##### 3.2.9.1.1 Total Dose Effects on NEMT

The NEMT's in the TSM are subjected to several bias conditions. The two chosen for bias under radiation are  $V_{GS} = +13V$  and  $-10V$ . As can be seen in Figure 3.86 and 3.87, the thresholds shift smaller as total dose exposure increases. The  $V_{GS} = +13V$  is the worst bias condition, with shifts of about 1V to 2V worst-case.

## TEST : CURRENTS AT STANDRY

AT DEVICE PIN NO. = 32	CURRENT = .150001E-01	(0)	I55	48
AT DEVICE PIN NO. = 39	CURRENT = -.150001E-01	(0)	IDD	48
AT DEVICE PIN NO. = 3	CURRENT = .300001E-01	(0)	IPP	48
AT DEVICE PIN NO. = 4	CURRENT = -.500001E-02	(16)	IMWS*	48
AT DEVICE PIN NO. = 6	CURRENT = .250001E-01	(16)	INN	48

TEST : Deselected Buffer Leakage with Output HI  
CURRENT = -.150001E-01 (48)

TEST : Deselected Buffer Leakage with Output LO  
CURRENT = .200001E-01 (48)

TEST : WORST CASE ACCESS TIME PER QUADRANT  
( MAXIMUM = 4096 )

ADDRESS =	0	128	256	384
ACCESS =	4096	4096	4096	4096

TEST : OUTPUT RESISTANCE WITH SIGNAL LO

NO LOAD VOLTAGE = .200001E-02

LOADED VOLTAGE = .200001E-02

TEST : OUTPUT RESISTANCE WITH SIGNAL HI

NO LOAD VOLTAGE = .200001E-02

LOADED VOLTAGE = .200001E-02

TEST : ILMH

ILMH = -.1E-02 (0)

TEST : VTL

VTL = -10.24 (16)

TEST : ILMH

ILMH = .500001E-03 (0)

TEST : VTH

VTH = -12.85 (0)

TEST : VTLVP

VTLVP = -8.94501 (16)

TEST : VTLVN

VTLVN = 6.06001 (32)

TEST : VTHVP

VTHVP = -8.94001 (16)

TEST : VTHVN

VTHVN = 6.06001 (32)

TEST : ILLVP

ILLVP = -.5E-01 (0)

TEST : ILLVN

ILLVN = .1 (0)

TEST : ILHVP

ILHVP = -.5E-01 (0)

TEST : ILHVN

ILHVN = .1 (0)

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FIGURE 3.85 TSM PACKAGE TEST PROGRAM PARAMETRICS

The shift will cause the NEMT's to switch OFF later and ON sooner generally speeding response of the circuitry. It also reduces noise margin. With higher dose, a shift to zero threshold would be near to stopping TSM operation because the NEMT could not be switched OFF. The shifts shown, out to "3", are within operational range and indicate that the TSM should operate beyond that dose level.

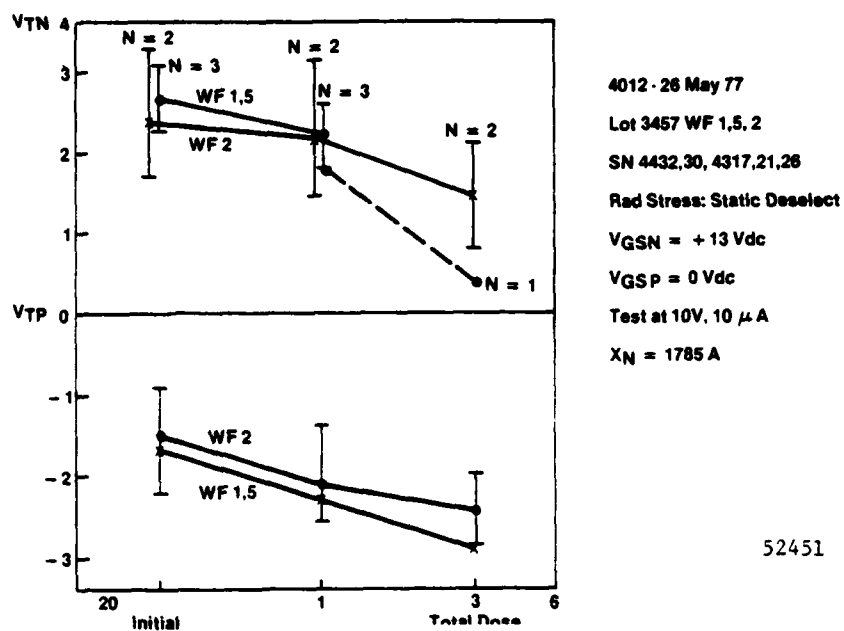
### 3.2.9.1.2 Total Dose Effects on PEMT

The PEMT's in the TSM are subjected to a range of bias conditions from  $V_{GS} = 0V$  to  $-31V$ . These two extreme values are those chosen for bias under radiation. As seen in figure 3.86 and 3.87, the threshold shifts are opposite under the two bias conditions. With  $V_{GS} = 0V$ , the threshold becomes larger in magnitude, by about  $1-1/2V$ .

This change is within design limit and will cause some slowing of circuit switching speed. With  $V_{GS} = -31V$ , the shift is about  $2V$  in the other direction, resulting in a zero threshold voltage. With this shift the PEMT becomes depletion mode (PDMT) and may prevent the TSM circuitry from operating properly. A change in processing to increase the initial threshold voltage in magnitude is a solution shown in the next two figures, figures 3.88 and 3.89. For these parts, the nitride thickness is  $515\text{\AA}$  greater than in the first two figures. As a result, the PEMT initial threshold voltage is larger in magnitude. With  $V_{GS} = -31V$ , decrease in threshold to zero is held off until a dose of "2". Additional process development later in the program provided additional improvement, with shifts remaining within design limits beyond a dose of "3".

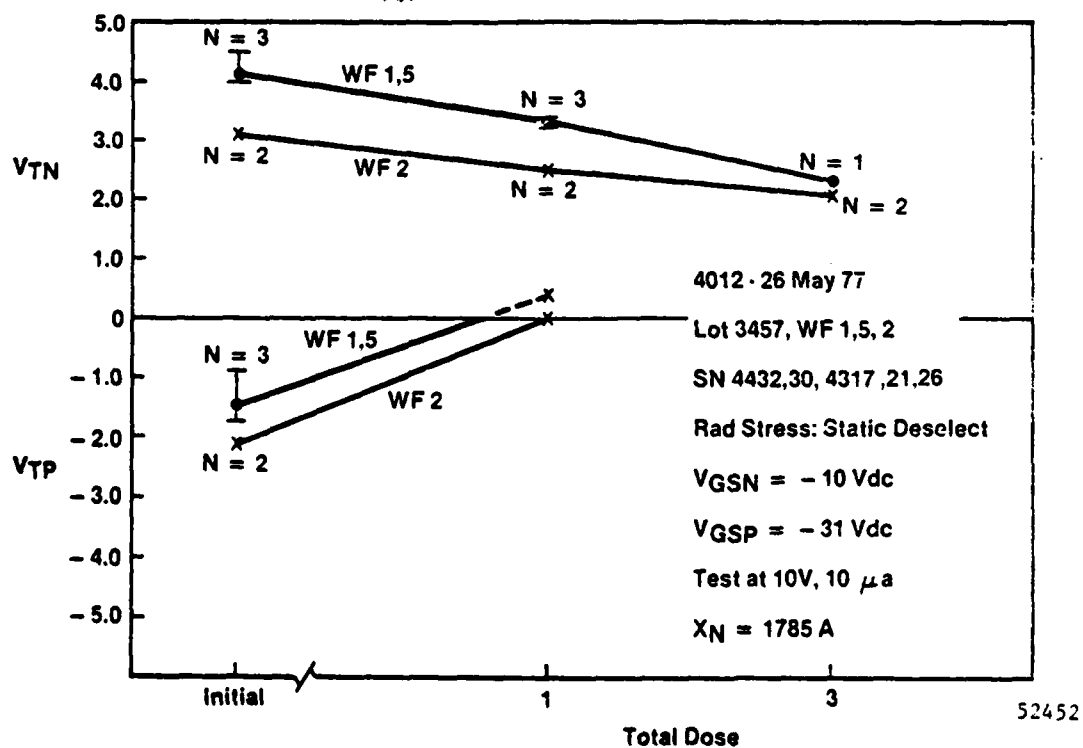
### 3.2.9.1.3 Total Dose Effects on TSM Access Time

A 6012 TSM of lot 3457, one of those shown in the first two figures, was evaluated for access time. Initial access time ranged from 205 to 230 ns with a 220 ns average. After a total dose exposure of "1", access time increased by only about 9% to a range of 218 to 260 ns with a 240 ns average. At an exposure of "2" the part was not functional, primarily because the PEMT's with  $V_{GS} = -31V$  had shifted to depletion. Process development later in the program enhanced the transistor hardness and was expected to ensure TSM performance to an exposure of "3". Additional TSM parts were not fabricated later in the ACT 1 program, so improved hardness data was not obtained for the TSM. Substantial improvements in hardness for the PSM were demonstrated.



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FIGURE 3.86 TSM: THRESHOLD VOLTAGE VS TOTAL DOSE



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FIGURE 3.87 TSM: HIGH VOLTAGE THRESHOLD VS TOTAL DOSE

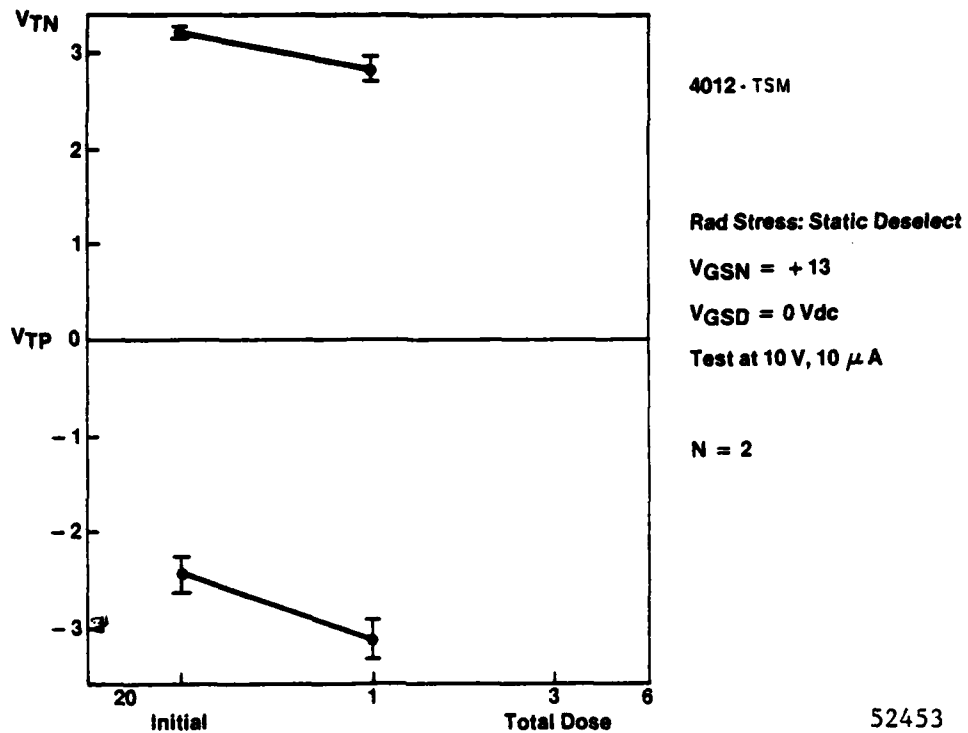


Figure 3.88. TSM: Threshold Voltage vs Total Dose

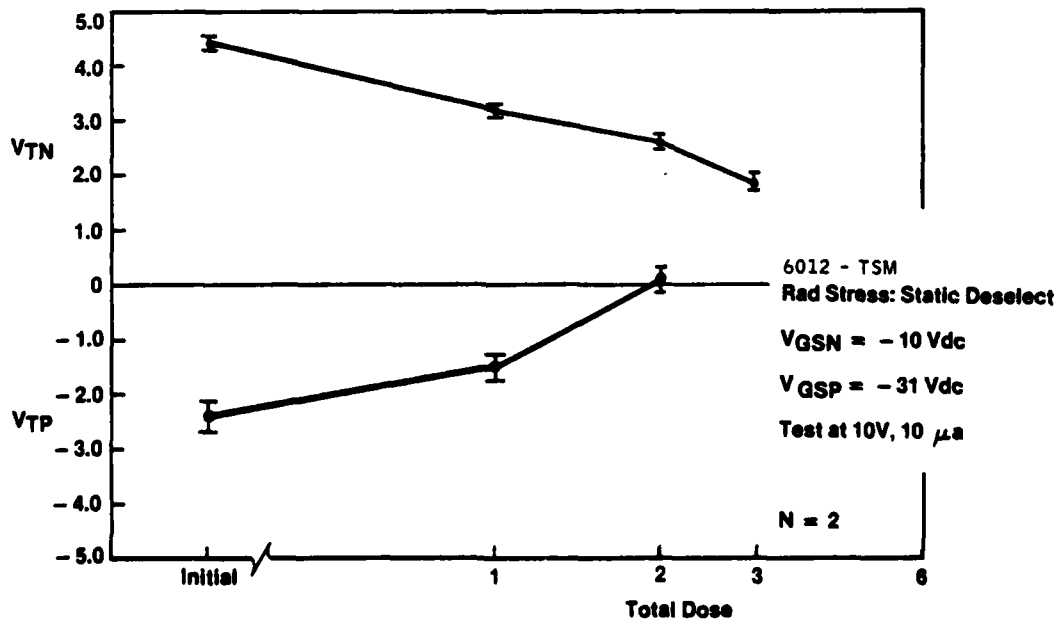


Figure 3.89. TSM: High Voltage Threshold vs Total Dose

### 3.2.10 TSM 6024 Test Results

Substantial progress has been made on development of the fast-write, MNOS-CMOS/SOS nonvolatile, hardened 512 bit Temporary Store Memory (TSM). The design modification of the original 6012 design to provide a 6024 mask set was completed in early 1978 under this MX ACT 1 program, see 3.2.7 above. Lot fabrication with this mask set and testing of resulting parts was supported on another program: The Spaceborne Computer TSM Program, Raytheon Subcontract 52-0075-52-02255, funded by SAMSO/YAD under contract No. 04701-75-C00149. Some of the test results supported by that contract and extracted from reports to Raytheon are reported here for completeness. Testing of fabricated parts shows good function and promise of reaching the performance goals.

Wafer test for three lots of TSM supported by the SCTSM program showed about 60 dice to have significant write/read function. This is about 6% of the potential dice available at wafer test. Of thirty-five (35) packaged and tested parts, there are four (4) fully functional parts, which correctly read at all 512 addresses for patterns written into the part. Ten (10) additional parts have over 75% of the bit locations functional, with only one or two rows or columns of the memory array inoperative. Many parts have had at least 40 hours of burn-in at 125C with dynamic bias; no parts failed and only minor changes in supply currents or in the map of memory array function were detected. Twenty-one (21) more dice are to be packaged for test.

Retention test of 96 bits on two parts show over 80% of the bits retained stored data beyond 20 hours. Tests of single addresses on several other parts support this data.

These functions and retention test have been run with a 10 microsecond write pulse width. The goal for the TSM is writing with a 1.0 microsecond pulse, and some data has been taken at that pulse width. Some of the parts which are fully functional when written at 10 microseconds seem to be fully functional at 1.0 microseconds also. Other useful testing has been done with 2.5 and 5.0 microsecond write pulses. Some tests of retention after an endurance stress of 10 data reversals have been run. Little degradation of retention slope has been noted, but more data is needed before any conclusions can be made.

The TSM device is now functioning essentially as originally intended. The complex write cycle requires: 1) read store contents, 2) compare with data to be written, 3) inhibit write if same, 4) write if different, and 5) write so that the thresholds of the two memory transistors per bit are shifted in opposite directions simultaneously. The present parts are executing this complex write cycle reasonably well.

### 3.2.11 TSM Summary

The TSM 6024 design modification was successful. A small quantity of parts with fast-write functionality have been produced. Limited characterization testing reveals variations in performance from part to part.

## 3.3 THE MNOS/SOS PROCESS

The following sections describe the process sequences and device structures developed for the Permanent Store Memory (PSM) and the Temporary Store Memory (TSM).

### 3.3.1 NMOS Nonvolatile Memory Technology

#### 3.3.1.1 The Basic MNOS Memory Transistor Structure

The metal nitride oxide semiconductor (MNOS) memory transistor is a device similar to other insulated gate field effect transistors (IGFET's). The major difference is that the gate insulator is composed of two insulator layers. The first layer is an oxide, typically 20Å thick at the silicon interface. The second insulator layer on top of that is a relatively thick silicon nitride film, typically 300 to 500Å.

A simplified cross section of a p-channel MNOS transistor is shown in figure 3.3-1. Note that the surface current that flows laterally between the source and drain in the surface inversion layer is controlled by the gate electrode. An applied negative gate to source bias ( $V_{gs}$ ) which just initiates current flow between the drain and source is called the threshold voltage  $V_T$ . In MNOS transistors, it is possible to alter the threshold of surface conduction ( $V_T$ ) by electrically altering the amount of charge per unit area,  $Q_I$ , stored near the nitride-oxide interface.

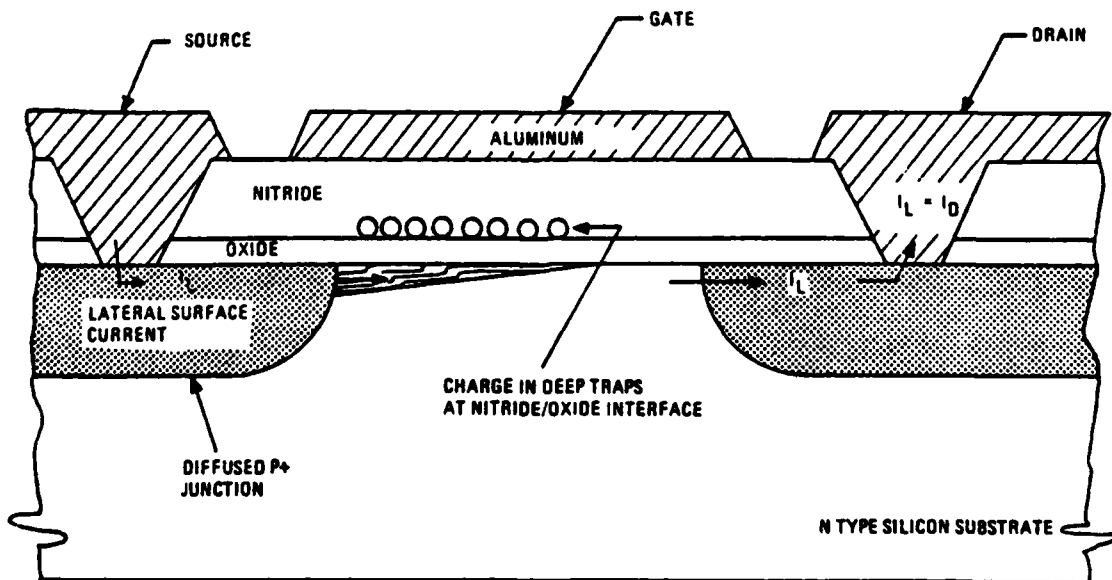


FIGURE 3.3-1 SIMPLIFIED CROSS SECTION OF MNOS MEMORY TRANSISTOR

The charge density stored near the nitride-oxide interface ( $Q_I$ ) can be electrically altered by applying a large voltage across the gate insulator. For a sufficiently large voltage, called the memory write voltage, charges are transported by tunneling through the thin oxide to the nitride-oxide interface. The nitride is an order of magnitude thicker than the oxide, so the current flow in the nitride is usually negligible. Thus, most of the charge transported through the oxide is available to fill charge trapping centers near the nitride-oxide interface. It is important to note that charge storage in trapping centers is a much different phenomenon than molecular dipole orientation as in ferroelectric materials.

The charge versus electric field tunneling properties of the thin memory gate oxide are affected significantly by processing parameters. In general, thick oxides (25-35Å) require longer pulsewidths than thin oxides (15-25Å) to achieve the same amount of stored charge for a given electric field strength. However, significant tunneling differences may even occur for the same oxide thickness because of oxidation parameter differences.

The basic method of reading the memory is to measure the threshold of lateral surface conduction  $V_T$ . A small negative voltage is applied to the gate of the MNOS transistor until a small drain current is sensed. This gate voltage  $V_T$  is directly proportional to the amount of charge stored at the nitride-oxide interface (i.e.,  $V_T \sim -q N_I$ ).

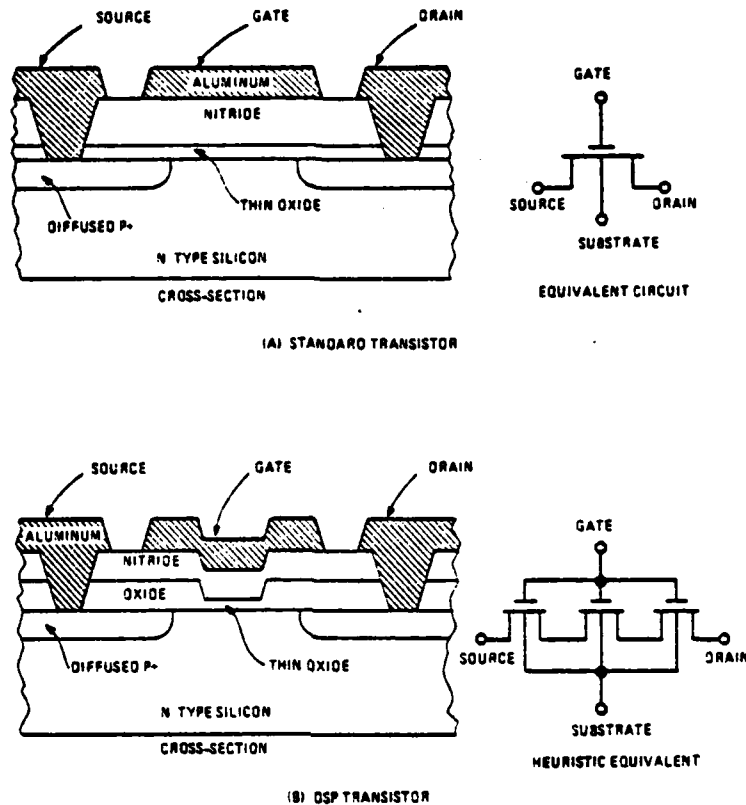
Nondestructive readout (NDRO) of the memory device is achieved because the read voltage amplitude and pulsewidth are made to be small compared to the amplitude and pulsewidth required to change the amount of charge stored.

The period of charge retention in the traps at the nitride-oxide interface has been measured to be more than 3 years for some types of MNOS structures. This long period of charge retention is related to the relatively large amount of energy required to lift the charges out of the charge traps or to tunnel the charge back out of the traps to the semiconductor.

The basic structure shown in figure 3.3-1 has been modified to provide drain-source protection. A thick oxide ( $X_{ox} > 100\text{\AA}$ ) region over the source and drain junction isolates the thin planar memory gate oxide region from the diffused source and drain regions and provides a number of advantages.

These two types of memory transistor structures have been used in previous MNOS work at Westinghouse. These are illustrated in figure 3.3-2 as an unprotected memory transistor and as the Drain-Source Protected Memory Transistor (DSPT). The major difference in their structure is that the thin 15-25 Å tunneling oxide does not overlap the diffusions in the protected structure. The drain source protected memory structure has been used in all major MNOS chips at Westinghouse including the NOVRAM array.

There are several advantages in addition to more reliable operation after many clear/write cycles accrued from the use of the Drain-Source Protected memory element. One is that the lower limit of the threshold voltage is determined by the thick oxide and limits device operation to the enhancement mode only. This eliminates parasitic current paths in large arrays of these devices and thus ensures reliable readout of the memory device. Another advantage



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FIGURE 3.3-2 COMPARISON BETWEEN PROTECTED AND UNPROTECTED TRANSISTOR STRUCTURES

is that the gate-to-drain breakdown is determined by the thick oxide portion of the gate. Thus, the junction field cannot add to the thick oxide field to cause localized oxide overstress. Also, this extra oxide protection between the gate and source-drain junctions allows one to apply a positive voltage ( $V_G = +25$  V) to the gate to clear the device while the drain remains biased at  $V_{DD} = -25$  V without causing gate insulator breakdown.

The advantages of this Drain-Source Protected MNOS memory element are summarized as follows:

- a. Reliable memory operation for many clear/write cycles.
- b. Memory read operation limited to the enhancement mode only, thus allowing parallel connection of many memory devices in large arrays and providing a reliable read operation.
- c. The drain or source to gate breakdown voltage approaches 80 V, which is similar to conventional MOS transistors.
- d. The DSP memory gate capacitance is reduced to only 25 percent of the gate capacitance of a conventional memory device with thin oxide across the entire source/drain regions. This means 4 times as many can be driven in parallel with an equivalent response time.
- e. The gate-to-source capacitance is greatly reduced, thus reducing the proportion of the address voltage fed through to the memory detection circuitry.

**3.3.1.2 Radiation Effects in Silicon Nitride/Silicon Dioxide Gates**

The theory of radiation effects in silicon nitride/silicon dioxide gate insulators has been discussed in several significant technical publications. These references are tabulated in Table 3.3-1 along with technical papers that were a direct result of the ACT 1 program. The latter papers are included in Appendix A for convenience.

TABLE 3.3-1  
SILICON NITRIDE REFERENCES

**A. MNOS Memory and Nitride Radiation Effects**

- 1) A. G. Stanley, "Comparison of MOS and Metal-Nitride-Semiconductor IGFETS Under Electron Irradiation," IEEE Transactions on Nuclear Science, NS-13, No.6, pp. 248-254, Dec. 1966.
- 2) C. W. Perkins, K. G. Aubuchon and H. G. Dill, "Radiation Effects and Electrical Stability of Metal-Nitride-Oxide-Silicon Structures," Applied Physics Letters, Vol. 12, 385-387, 1 June 1968.
- 3) P. A. Newman, H. A. R. Wegener, "Effects of Electron Radiation on Silicon Nitride Insulated Gate Field Effect Transistors," Trans. on Nuclear Science, pp. 293, Vol. NS-14, No. 6, Dec. 1967.
- 4) J. R. Cricchi, F. C. Blaha, M. D. Fitzpatrick, "The Drain-Source Protected MNOS Memory Device and Memory Endurance," IEEE Int. Electron Devices Digest, pp. 157-162, Dec. 1973.
- 5) J. R. Cricchi, F. C. Blaha, M. D. Fitzpatrick, F. M. Sciulli, "Semiconductor Memory Research," Tech. Rpt. AFAL-TR-75-233, pp. 109-127, Dec. 1975.
- 6) R. S. Ronen, et. al., "High Voltage SOS/MOS Devices and Circuit Elements: Design, Fabrication and Performance," JSSC, 11, 431-42, August, 1976.
- 7) P. C. Arnett and D. J. Di Maria, "Contact Currents in Silicon Nitride," J. Appl. Phys. Vol. 47, 2092-2097, May 1976.
- 8) D. J. Di Maria and P. C. Arnett, "Conduction Studies in Silicon Nitride: Dark Currents and Photocurrents," IBM, J. Res. Develop., pp. 227-244, May 1977.
- 9) C. M. Svensson, "The Conduction Mechanism in Silicon Nitride Films," J. Appl. Phys. Vol. 48, No. 1, pp. 329-335, Jan. 1977.
- 10) H. A. R. Wegener, M. B. Doig, P. Marrifino and B. Robinson, "Radiation Resistant MNOS Memories," IEEE Trans. on Nuclear Science, NS-19, p. 291, Dec. 1972.
- 11) N. S. Saks, "Response of MNOS Capacitors at 80°K," IEEE Trans. on Nuclear Science, NS-25, No. 6, pp. 1226, Dec. 1978

TABLE 3.3-1 (continued)

## B. ACT-1 Related Publications (See Appendix A)

- 1) M. D. Fitzpatrick, F. M. Sciulli, F. C. Blaha, J. R. Cricchi, "MNOS/SOS Memory Using High Voltage Depletion Mode CMOS Logic, 1976 GOMAC, Nov. 1976.
- 2) "Radiation Hardened CMNOS/SOS Mask-Programmable ROM and General Processor Unit", J. R. Cricchi, D. A. Barth, H. G. Oehler, R. C. Lyman, J. M. Shipley and B. T. Ahlport, (IEEE Annual Conference on Nuclear and Space Radiation Effects, Williamsburg, VA, July 1977) IEEE Trans. Nucl. Sci., NS-24, No. 6, Dec. 1977.
- 3) "Hardened MNOS/SOS Electrically Reprogrammable Non-Volatile Memory", J. R. Cricchi, M. D. Fitzpatrick, F. C. Blaha and B. T. Ahlport, (IEEE Annual Conference on Nuclear and Space Radiation Effects, Williamsburg, VA, July 1977) IEEE Trans. Nucl. Sci., NS-24, No. 6, P. 2185, Dec. 1977.
- 4) "MNOS/SOS Devices for Radiation Hardened Computers", J. R. Cricchi, M. D. Fitzpatrick, D. W. Williams, 1977 IEEE Non-Volatile Semiconductor Memory Workshop, Vail, Colorado, August 1977.
- 5) "Voltage Translation Devices and Circuits Using SOS Technology", J. R. Cricchi, M. D. Fitzpatrick, F. C. Blaha, H. G. Oehler, 1977 IEEE SOS Technology Workshop, Vail, Colorado, Sept. 1977.
- 6) "Hardened Silicon Gate CMOS/SOS Structures", J. G. Oehler, D. A. Barth, H. Neal, J. R. Cricchi, 1977 IEEE SOS Technology Workshop, Vail, Colorado, Sept. 1977.
- 7) B. T. Ahlport, J. R. Cricchi, D. A. Barth, "CMOS/SOS LSI Input/Output Protection Networks", IEEE Trans. on Electron Devices, Vol. ED-25, No. 8, pp. 933-938, August 1978.
- 8) "Radiation Hardened MNOS-CMNOS/SOS Fast Write RAM", J. R. Cricchi, D. W. Williams, J. L. Fagan, F. C. Blaha, B. G. Stamps, R. C. Lyman, B. T. Ahlport, IEEE Annual Conference on Nuclear and Space Radiation Effects, July 1978.
- 9) M. D. Fitzpatrick, J. R. Cricchi, B. G. Stamps, "Built-In Memory Cell Test Feature for a Radiation Hardened 1024-bit MNOS/SOS Electrically Programmable Nonvolatile Memory", 1978 GOMAC, Nov. 1978.

### 3.3.2 MNOS/SOS Process For The PSM

The PSM process was based on MNOS/SOS developments which occurred during the SAMSO and Air Force Avionics Laboratory sponsored "Semiconductor Memory Research" program. Ref A "Semiconductor Memory Research" AFAL-TR-75-233, Contract F33615-73-C-1093-P00005, Final Report for Period of July 1973 to June 1975, Report Date July 1976. This previous development included the 6003 Nonvolatile Random Access Memory (NOVRAM) test vehicle and the NR/NRD process sequence. Both the radiation hardened and stable CMOS/SOS process and the MNOS/SOS process were improved during the ACT 1 Basic Parts activities (75 Feb. thru 75 Oct.). During the concepts Phase and LSI Parts Design Phase (75 Oct. thru 76 May) the MNOS/SOS process for both the PSM and TSM continued to evolve. The CMNOS/SOS and CMNOS-MNOS/SOS device data baseline for LSI design was presented at the ACT 1 PARTS DESIGN REVIEW II on 3 June 1976. This baseline process is described in paragraph 3.3.2.1. After the LSI Fabrication and Test phases were completed it became obvious that process refinement was needed to provide more reproducible characteristics. A Processes Refinement phase was carried out from October 1977 thru October 1978. This latter phase is described in Para. 3.3.2.2.

#### 3.3.2.1 Baseline Process

The baseline process sequences and device structures described at PDR II on 3 June 1976 were maintained thru June 1977, which was the period in which all four LSI parts were fabricated and tested. Key features of the SOS processing sequences are summarized in Table 3.3.-2. Note that the MNOS/SOS process for both the PSM and TSM MNOS memories are extensions of the baseline CMOS/SOS process. The baseline CMOS/SOS process is described in Section 3.3.4.

The baseline process for the MNOS/SOS PSM is different from the CMOS/SOS process in that steps to form a high voltage N Depletion mode transistor (NDMT) are added. Also the MNOS memory gate window and nitride deposition steps are added. The PSM MNOS/SOS baseline process is shown in Table 3.3-3. This is called the nitride removal/nitride redeposition (NR/NRD) process. Cross-sections of the Drain-source protected memory transistor and the implanted N depletion mode transistor formed with the PSM MNOS/SOS baseline process are shown in Figure 3.3.-3.

The baseline process for the MNOS-CMOS/SOS TSM is different from the PSM process in that the Boron implant mask is altered from the CMOS/SOS baseline to form high voltage N enhancement mode transistor (HV-NEMT) and normal NEMT. The ion implant levels are identical to the CMOS/SOS baseline. Also the memory device is formed as for the PSM process. The TSM MNOS-CMOS/SOS baseline process is shown in Table 3.3-4. The cross-section of the HV-NEMT is shown in Figure 3.3-4.

TABLE 3.3-2 SOS PROCESSING SEQUENCES

Basic CMOS/SOS processing; N & P enhancement (NEMT, PENT) (9 Masks)

- o BORON implant to control  $V_{TN}$
- o Boron implant to control back channel leakage
- o Low temperature - time cycle times
- o Low temperature CVD layers, APCVD Silicon Nitride

MNOS/SOS processing is a variation of baseline CMOS/SOS process

- o PSM: N Depletion, P enhancement, Protected Memory Transistors (NDMT, PENT, PMT) (11 Masks)
  - : Phosphorous implant to control  $I_{DSO}$
  - : Boron implant to control back channel leakage
- o TSM: High Voltage N enhancement, p enhancement, protected memory (HVNEMT, HVPENT, PMT) (10 Masks)
  - : Boron implants to set HVNEMT levels & Back Channel Leakage

Single layer metal - aluminum

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Silox passivation

TABLE 3.3-3 PSM: MNOS/SOS NR/NRD PROCESS SEQUENCE

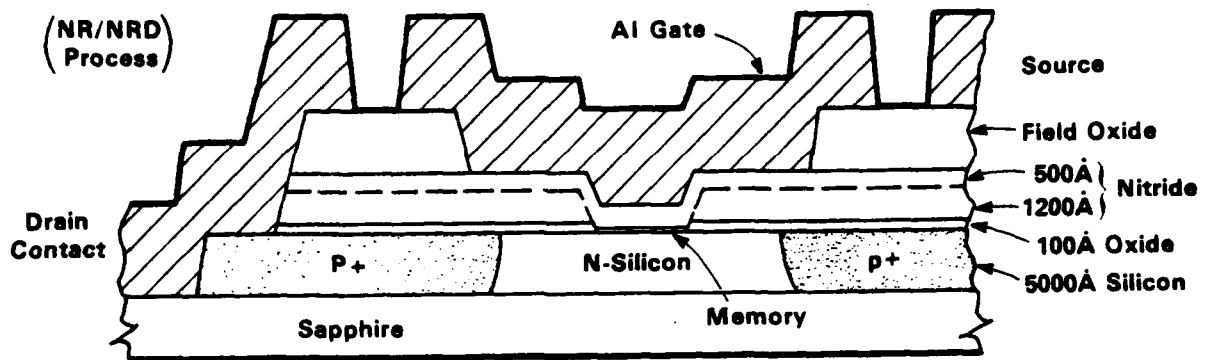
Silicon island	- Mask #1	Memory Nitride Deposition	
Phosphorus Implant, NDMT	- Mask #2	Field Silox Deposition	
Gate Nitride Protect	- Mask #3	Contact Window	- Mask #8
Phosphorus N+ Diffusion	- Mask #4	Gate Window	- Mask #9
Boron Implant, NDMT	- Mask #5	Aluminum Deposition	
Boron (P+) Diffusion	- Mask #6	Metal Interconnect	- Mask #10
Gate Oxidation & Anneal		Sinter	
Gate Nitride Deposition & Anneal		Silox Deposition	
Memory Gate Window	- Mask #7	Bonding Pad Window	- Mask #11

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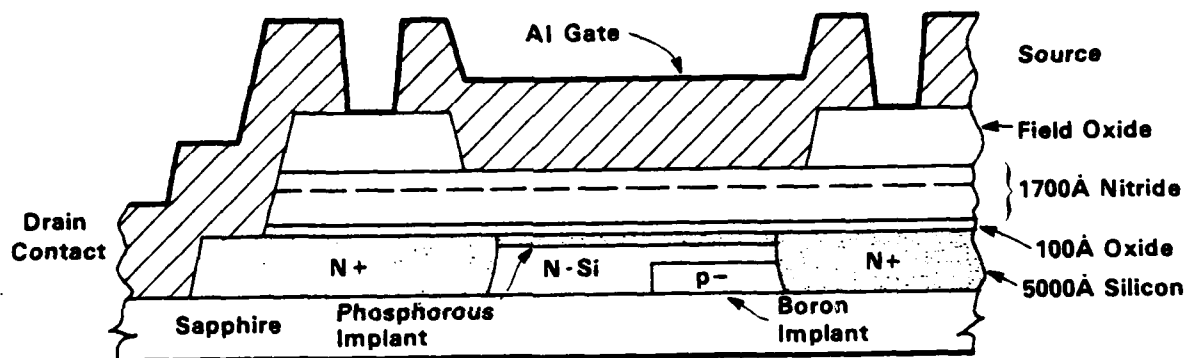
TABLE 3.3-4 TSM: MNOS/SOS NR/NRD PROCESS SEQUENCE

Silicon island	- Mask #1	Memory Nitride Deposition	
Gate Nitride Protect	- Mask #2	Field Silox Deposition	
Phosphorus (N+) Diffusion	- Mask #3	Contact Window	- Mask #7
Boron Implant NEMT	- Mask #4	Gate Window	- Mask #8
Boron (P+) Diffusion	- Mask #5	Aluminum Deposition	
Gate Oxidation & Anneal		Metal Interconnect	- Mask #9
Gate Nitride Deposition & Anneal		Sinter	
Memory Gate Window	- Mask #6	Silox Deposition	
		Bonding Pad Window	- Mask #10

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## Implanted N-Depletion Mode SOS IGFET



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FIGURE 3.3-3 DRAIN SOURCE PROTECTED MNOS/SOS MEMORY X-SECTION

## Cross-Section of High Voltage N-Channel Enhancement Mode Transistor with BORON Implant to Reduce Channel Leakage

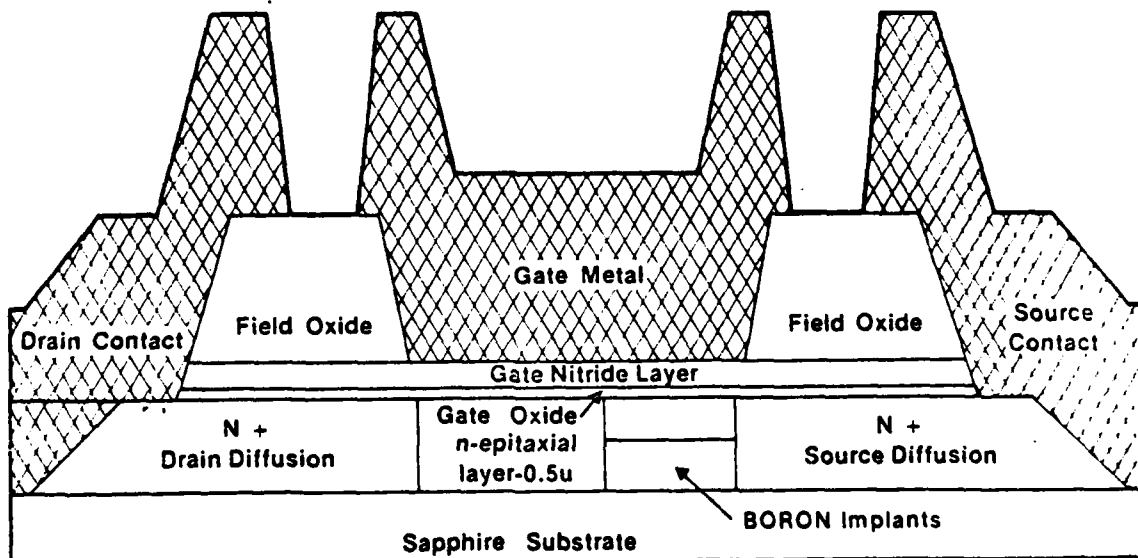


FIGURE 3.3-4 TSM: MNOS/SOS

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The CMOS/SOS N channel devices have a unique end geometry to prevent silicon island edge leakage currents (Post-rad) and to make contact to the p-type body region of the NEMT. The latter is done to minimize n channel "kink" effects and prevent electron injection from the source region by keeping the body-source bias to zero volts. The layout of the N channel end geometry is shown in Figure 3.3-5. This was considered a safe approach for a radiation hardened design and worth the additional area required for these 1976 designs. An additional feature of the end geometry is that it provided a deposited nitride and silox layer (10K) over the silicon island edge. This gave very reliable high breakdown voltage coverage of the silicon island edge. A cross-section of the metal crossing the island edge is shown in Figure 3.3.-6.

The layout design rules for the CMOS, TSM and PSM baseline process are shown in Table 3.3-5. These conservative design rules were used to insure safe operation even with radiation effects. Considerable area reduction is possible by computer aided shrinkage and sizing with the existing LSI design CALMA data base.

TABLE 3.3-5 LAYOUT/DESIGN RULES

	<u>CMOS</u>	<u>TSM</u>	<u>PSM</u>
Minimum N <sup>+</sup> - P <sup>+</sup> Space Along Silicon Edge	12	12	12
Gate Width 10V	4	5	
20V	-	9(HVNEMT)	7(PEMT)
30V	-	11(HVNEMT)	9(PEMT)
Boron Overlap of HVNEMT 20V		4	
30V		5	
Gate Metal Overlap of Gate Protect	1	1	1
Metal: Gate Width	6	7	8
Min. Interconnect Width	8	8	8
Min. Metal-Metal Space	8	8	8
Minimum Contact Window	6 x 6	6 x 6	6 x 6
Maximum Body Contact Spacing N-channel	40	40	40
P-channel	100	100	100

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DIMENSIONS AFTER PROCESSING (IN MICRONS)

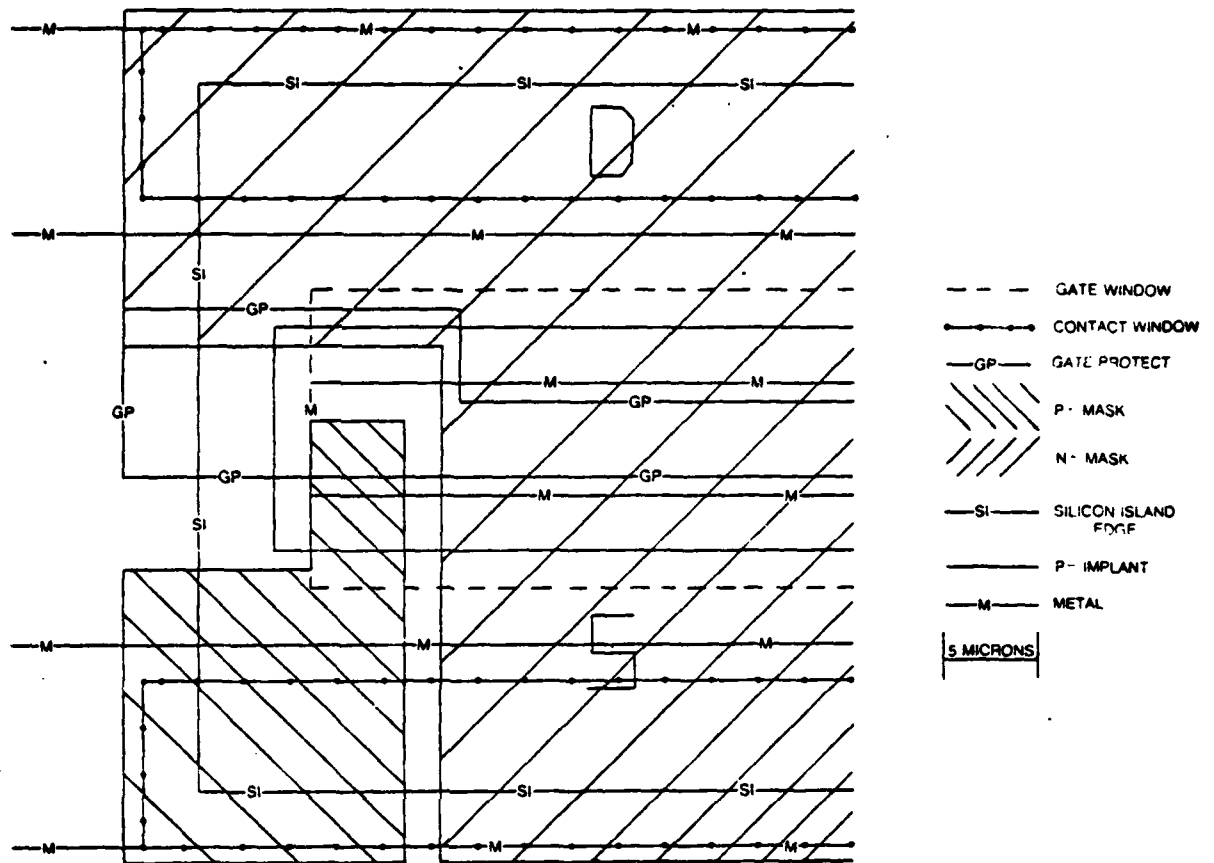


FIGURE 3.3-5 CMOS N CHANNEL END GEOMETRY

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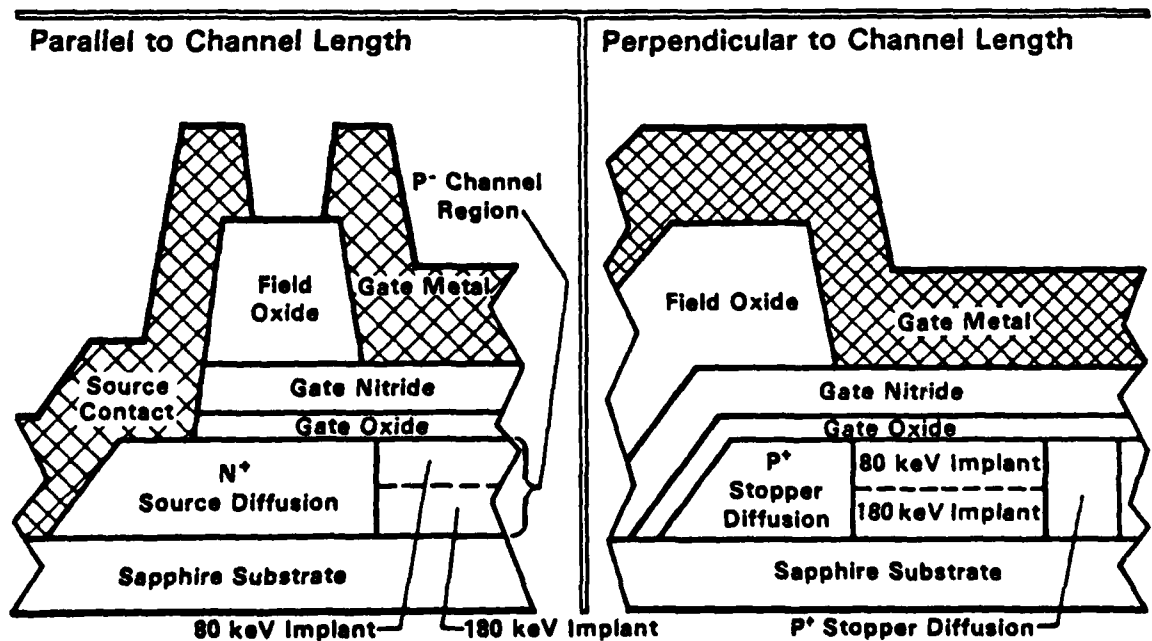


FIGURE 3.3-6 CMOS/SOS: CROSS-SECTION OF N-CHANNEL ENHANCEMENT MODE TRANSISTOR WITH TWO-LEVEL BORON IMPLANT AND CHANNEL STOPS TO REDUCE CHANNEL LEAKAGE

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## 3.3.2.2 MNOS/SOS Process Refinement

Processing for MNOS memory was resumed in October 1977. The scope of work focused on refining the fabrication sequence to optimize electrical performance and insure process repeatability. The process sequence from earlier phases of the program served as a baseline, but additional experimental data mandated specific alterations in order to optimize temperature-bias-stress (TBS) stability and radiation hardness. Thus, the objectives of electrical performance, process repeatability, TBS stability, and radiation hardness dictated the direction of process development during this phase.

At the outset a lot 6013 wafers, fabricated with the then current process, was run to verify previous results and provide data for further process development. The baseline process sequence was used for that lot, see Table 3.3-6.

### 3.3.2.2.1 Gate Dielectric

Specific objectives were then established. They were:

- o Reduce magnitude and range of initial  $V_T$ .
- o Reduce  $\Delta V_T$  caused by radiation.
- o Reduce effects of gate bias on radiation induced  $\Delta V_T$ .
- o Reduce back channel leakage magnitude and range.
- o Reduce drain leakage current on HV parts.
- o Assure TBS stability.
- o Improve retention-endurance performance.

A matrix of fabrication alternatives which impact the desired parameters was drawn up and used to define initial experiments. Many alternatives involved changes in the dielectric structure; their impact was verified using capacitor dots on bulk silicon. Initial capacitor experiments centered on the following process alternatives:

- |   |  |
|---|--|
| <ul style="list-style-type: none"> <li>o Gate oxidation                             <ul style="list-style-type: none"> <li>deposition conditions</li> <li>heat treatments</li> <li>thickness</li> </ul> </li> </ul>   | <ul style="list-style-type: none"> <li>800°C wet vs. 900°C dry</li> <li>anneal vs. no anneal</li> <li>75A to 135A</li> </ul>   |
| <ul style="list-style-type: none"> <li>o Gate nitride                             <ul style="list-style-type: none"> <li>deposition method</li> <li>deposition temperature</li> <li>ammonia/silane</li> <li>heat treatments</li> <li>deposition cycles</li> </ul> </li> </ul> | <ul style="list-style-type: none"> <li>APCVD vs. LPCVD</li> <li>700C vs. 750C</li> <li>1.5:1 vs. 9:1</li> <li>anneal vs. no anneal</li> <li>1 step vs. 2 step</li> </ul> |

TABLE 3.3-6  
BASELINE MNOS/SOS PROCESS SEQUENCE FOR THE PSM

PC-1	SI ISLAND	
PC-3	GP	
PC-5	N+ DIFFUSION	
	PHOS DIFFUSION	
	STRIP SILOX	BUF 10:1HF
	SILOX DEP	$10K\Omega \pm 1K$
PC-5	P-IMPLANT	
	ETCH SILOX	BUF 10:1HF
	ETCH NITRIDE	$H_3PO_4$
	ION IMPLANT B 180KeV $3.5 \times 10^{12}$	
	STRIP SILOX	BUF 10:1HF
	SILOX DEP	$7K \pm 1K\Omega$
PC-7	P+ DIFFUSION	
	ETCH SILOX	BUF 10:1HF
	BORON DIFFUSION	
	STRIP BORON GLASS	$HF_4$
	STRIP SILOX	BUF 10:1HF
	GROW OXIDE	400A @ 900C
	STRIP GP NITRIDE	$H_3PO_4$
	STRIP OXIDE	BUF 10:1HF
	DEP SILOX	$7K \pm 1KA$
PC-2	N-IMPLANT	
	ETCH SILOX	BUF 10:1HF
	ION IMPLANT P 100KeV $0.6 \times 10^{12}$	
	STRIP RESIST	
	STRIP-SILOX	BUF 10:1HF
	SILOX DEP	$5K \pm 1KA$
	IMPLANT ANNEAL	30 MIN $N_2$ @ 900C
	STRIP SILOX	BUF 10:1HF
	GATE DIELECTRIC	
PC-8	MEMORY GATE WINDOW	
PC-9	CONTACT WINDOW	
PC-13	GATE AND CONTACT WINDOW	
PC-11	METAL	
PC-12	VIA	

a) Gate Nitride: Each parameter was incorporated into a controlled capacitor experiment and evaluated for effect on nonmemory and memory performance as well as retention, endurance, TBS stability, and radiation hardness. It was evident very early that nitrides deposited by low pressure chemical vapor deposition (LPCVD) were desirable for their uniformity and repeatability. In addition, all showed good TBS stability as demonstrated by the C-V curve shown in Figure 3.3-7. Further, LPCVD nitrides contributed to achieving the objectives of reduced range of initial  $V_T$  and p-channel  $\Delta V_T$  caused by radiation. Some early radiation data corroborating the decision to use LPCVD nitrides for both memory and nonmemory nitrides is given in Figure 3.3-8. Because no significant improvements in the direction of program goals were seen by varying deposition temperature or ammonia-silane ratio ( $\text{NH}_3/\text{SiH}_2\text{Cl}_2$ ), the production standard settings were agreed upon. All subsequent nitride depositions were done at 750°C with  $\text{NH}_3/\text{SiH}_2\text{Cl}_2 = 9/1$  and demonstrated the advantages of uniformity and repeatability in fabrication.

b) Gate Oxide: Focus then shifted to the gate oxidation process and the choice of temperature, thickness, and heat treatments. The following summary of capacitor data substantiates the conclusions of several oxidation experiments:

- o  $\Delta V_{TP}$  caused by radiation is reduced by reducing oxide thickness.
- o  $\Delta V_{TP}$  is very sensitive to 800C  $\text{H}_2+\text{O}_2$  oxides compared to 900C dry oxides and is thus harder to control.

Figure 3.3-9 and 3.3-10 contrast the  $\Delta V_{TP}(\Delta V_{FB})$  dependence upon bias and thickness for 800C vs. 900C oxides. The results shown in Figures 9 and 10, and the fact that 800 C anneals were ineffective, while 900C anneals showed some indication of being less stable, led to the choice of an 80Å oxide grown at 900 C in oxygen with no anneal except that done in situ as the standard process.

c) Device Processing: In parallel with capacitor experiments, some 4007 CMOS/SOS triple inverter devices were fabricated to get some transistor data as support for what was shown on capacitors. The devices also provided samples for TBS and radiation testing. Following the choice of gate dielectric for new PSM parts, a few lots were fabricated, with only these changes to the baseline process. Several problems manifested themselves in the first PSM lots, principally  $I_{DSO}$  control and silicon island and sapphire thinning. Earlier these phenomenon had been masked, but with other process improvements these became visible and had an impact on yield, performance, and producibility. Each will be discussed in turn.

## 3.3.2.2.2 N-Depletion Mode Transistor (NDMT) Control

The first 6023 PSM lots fabricated showed nonuniform  $I_{DSO}$  across a wafer and from wafer-to-wafer within a lot. Introduction of the LPCVD nitride for other reasons lowers positive charge in the gate and increases  $I_{DSO}$  sensitivity to  $Q_{BULK}$ . In the earlier process several thermal cycles occurring after the depletion mode implant showed up the nonuniform vertical diffusion constant in SOS. Attempts were made to control  $I_{DSO}$  by adjusting the level of the phosphorus

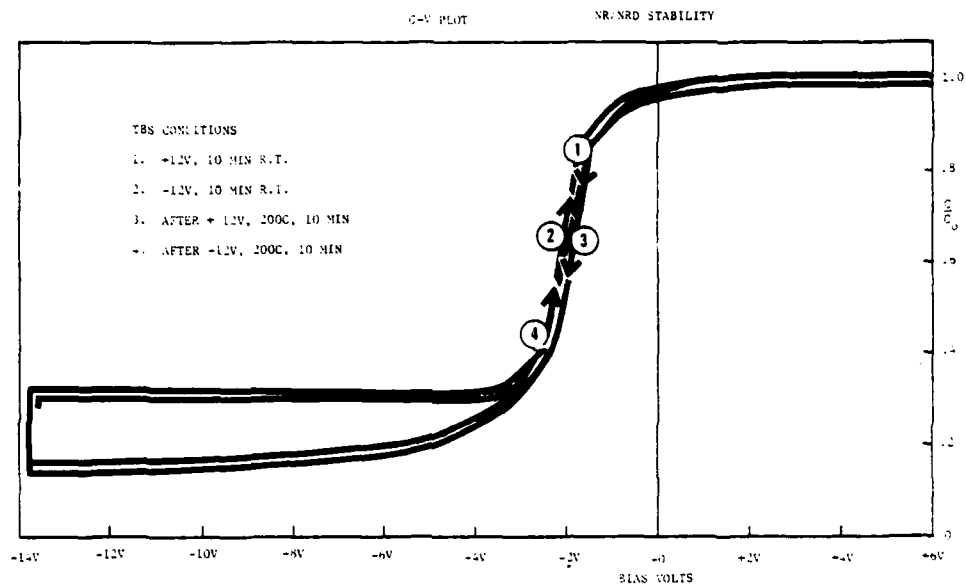


FIGURE 3.3-7 C-V PLOT FOR LPCVD NITRIDE

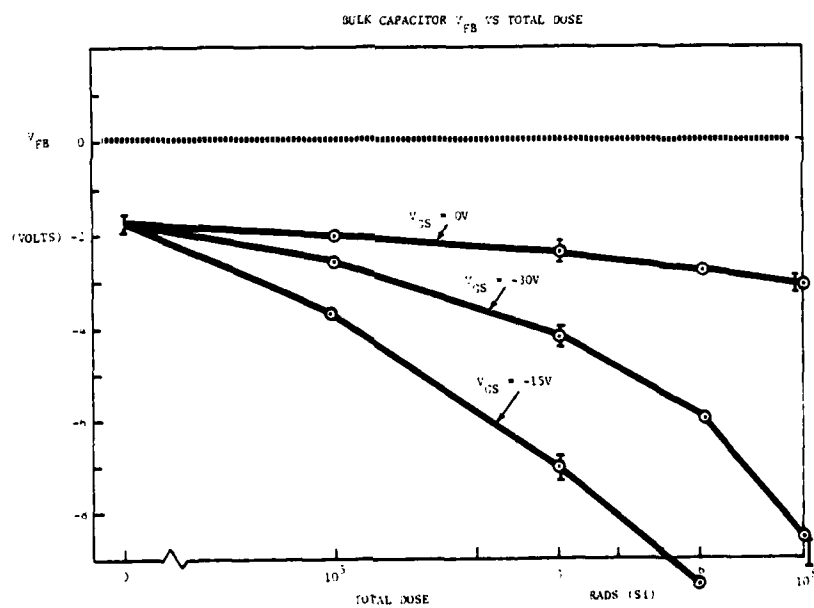


FIGURE 3.3-8 RADIATION PERFORMANCE FOR LPCVD NITRIDE

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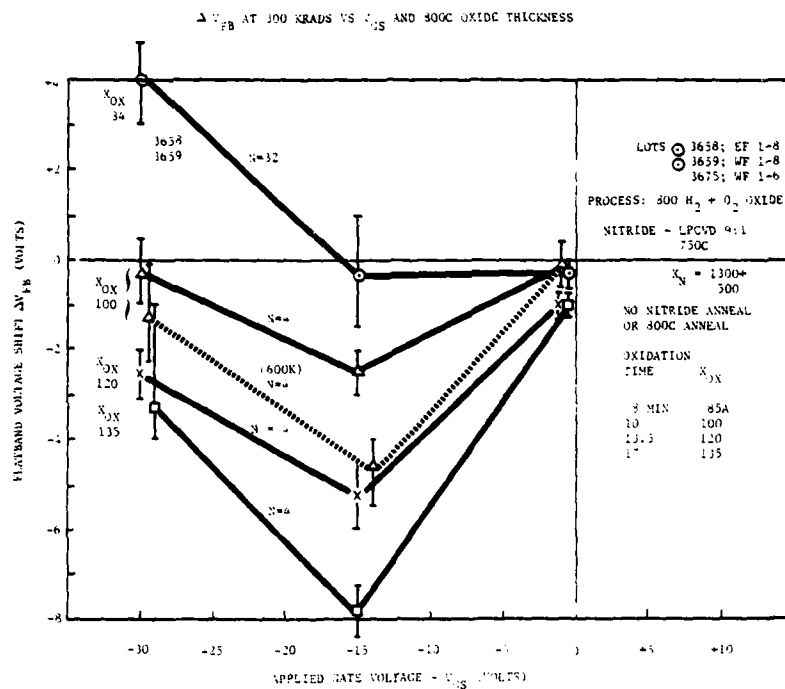


FIGURE 3.3-9 RADIATION-INDUCED  $\Delta V_{FB}$  FOR 800C  $H_2+O_2$  OXIDE

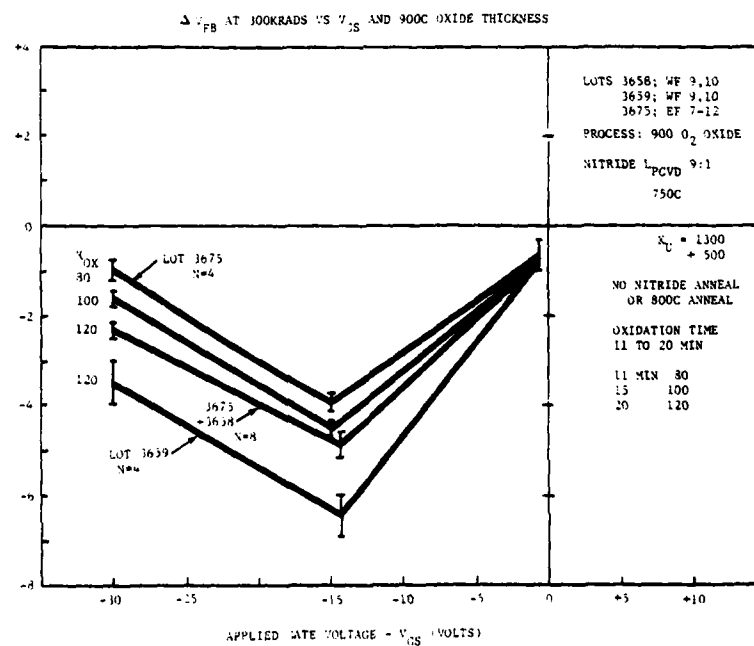


FIGURE 3.3-10 RADIATION-INDUCED  $\Delta V_{FB}$  FOR 900C DRY OXIDE

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implant (n-) to account for vertical diffusion. Arsenic (As) depletion mode implants were also tried on an experimental basis. Both gave stable CV characteristics and controlled  $I_{DSO}$  before further thermal cycling but showed non-uniformities when other temperature cycles had been completed. A solution was found by changing the process sequence to perform both ion implants after all other thermal cycles with the exception of the gate oxidation. The elimination of gate anneals further improved the uniformity by again minimizing the time at high temperature after implants. The depletion mode implant level was then adjusted to its current level of  $0.8 \times 10^{12}$  ions/cm<sup>2</sup> with good results.

### 3.3.2.2.3 Thinning of Silicon and Sapphire

Careful inspection of the first modified PSM lots for mask defects and the like revealed another yield impacting phenomenon. Silicon islands that had been diffused n+ and the sapphire which had been doped around them was being thinned by further processing, particularly etch cycles. The n+ diffusion occurs early in the fabrication sequence and thereby sees several subsequent etching cycles for other layers. No effort has been made to protect the islands from these etches because silicon island thinning was not anticipated. The most serious impact came from one long 10:1 HF cycle used to strip densified silox after the diffusion and a nitride stripping cycle in hot H<sub>3</sub>PO<sub>4</sub> (160-165C) used to remove the gate protect nitride. The primary result of removing the top layer of heavily doped n+ silicon was a lower concentration, higher sheet resistivity silicon which slows the part. It can result in nonlinear contacts because a thin island offers little barrier to reflection from the sapphire and contact windows become shrunken and distorted, if not closed altogether. To alleviate the observed thinning, cumulative etch cycles were minimized and where possible, a thin oxide was grown to protect silicon during nitride stripping procedures. These measures eliminated contact window shrinkage and aided the sheet  $\rho$  but did not eliminate all sapphire attack.

An alternative solution was proposed and verified experimentally but not incorporated into the final process. The alternative involved replacing the n+ diffusion by an arsenic (As) implant to form the source-drain regions. The sheet  $\rho$  obtained by the implant was not as low as with the phosphorous diffusion but did eliminate all sapphire attack. Because the solution discussed earlier was adequate and much more radiation and TBS data were available for phosphorous diffusion (n+), it was retained as the standard process. Some transistors fabricated with the As implanted source-drains showed TBS instability but lots run later, where As was implanted through a thin sacrificial oxide, do not show instability. TBS data beyond 1000 hours is now available and proves As implant to be a viable alternative, provided a much higher dose is used to obtain the desired sheet resistivity.

### 3.3.2.2.4 Contact Window Structure

Not only were process improvements made by introducing low pressure CVD gate nitrides and altering the fabrication sequence to do implants as late as

possible, but yield was also enhanced by introducing a new contact window structure. A sloped contact window in silox combined with Al-Si metallization achieved goals of reproducible and reliable metal step coverage and much improved contact integrity. The two processes for defining contact windows may be contrasted for the quality of sloped contact window and for their producibility.

The first (or baseline) process used the fabrication sequence shown in Figure 3.3-11. It gave the cross sections shown in the same Figure. With this process 10-12kÅ of Al had to cover an 11.9kÅ step which was only sloped for 1/3 of its height. It also depended on lightly doped silox which required a special operator setting to be done precisely. More than one lot showed metal step coverage problems that resulted from the step noted above. A typical SEM from the process outlined above is shown in Figure 3.3-12.

To eliminate step coverage as a yield impact factor, a new sloped contact window process was instituted. It makes use of standard production doping levels and therefore requires no special settings or operator control. Uniformity and reproducibility have been demonstrated for this process. The fabrication sequence proceeds as shown in Figure 3.3-13. Cross sections for this sequence are shown in the same Figure. Using this modified process, 12-13K Al-Si must cover an 11.9K step which is sloped for 85% of the step height. SEMs of devices fabricated with the modified process have verified repeatedly good step coverage over several production lots. A typical picture of step coverage is given by the SEMs from two different PSM lots, shown in Figure 3.3-14.

#### 3.3.2.2.5 Modified MNOS/SOS Process Sequence

The end product of all process alternatives reviewed during the activity led to a redefinition of the fabrication sequence recommended and used for the production of memory parts. This process is summarized in Table 3.3-7.

In summary, alterations in the PSM process sequence were made to enhance the objectives of a producible part with demonstrated performance, TBS stability, and radiation hardness. Improvements were principally in three areas: low pressure chemical vapor deposition without anneals, implants moved to later in the process after high temperature diffusions, and sloped silox windows with Al-Si metallization. The result is a common process sequence, suitable for CMOS/SOS logic and MNOS/SOS memory parts.

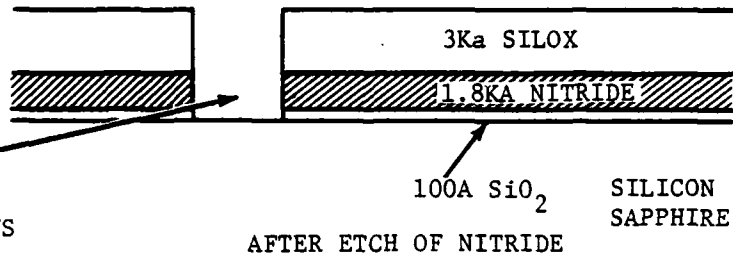
TABLE 3.3-7  
MODIFIED MNOS/SOS PROCESS SEQUENCE FOR THE PSM

PC-1	SI ISLAND	
PC-3	GP	
PC-5	N+ DIFFUSION	
	PHOS DIFFUSION	
	STRIP SILOX	BUF 10:1HF
	SILOX DEP	$7K \pm 1K\text{\AA}$
PC-7	P+ DIFFUSION	
	ETCH SILOX	BUF 10:1HF
	BORON DIFFUSION	
	STRIP BORON GLASS	$\text{HBF}_4$
	STRIP SILOX	BUF 10:1HF
	GROW OXIDE	400A @ 900C
	STRIP GP NITRIDE	$\text{H}_3\text{PO}_4$
	STRIP OXIDE	BUF 10:1HF
	GROW OXIDE	400A @ 900C
PC-6	P-IMPLANT	
	ION IMPLANT B	
	180KeV $3.5 \times 10^{12}$	
	STRIP PHOTORESIST	
PC-2	N-IMPLANT	
	ION IMPLANT P	
	100KeV $0.6 \times 10^{12}$	
	STRIP RESIST	
	STRIP OXIDE	BUF 10:1HF
	SILOX DEP	$5K \pm 1K$
	IMPLANT ANNEAL	30 MIN $\text{N}_2$ @ 900C
	STRIP SILOX	
	GATE DIELECTRIC	BUF 10:1HF
PC-8	MEMORY GATE WINDOW	
PC-9	CONTACT WINDOW	
PC-13	GATE AND CONTACT WINDOW	
PC-11	METAL	
PC-12	VIA	

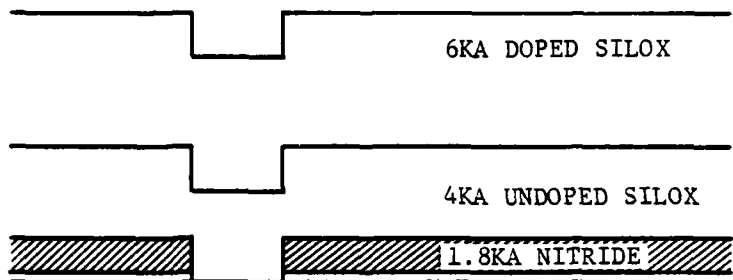
# PROCESS SEQUENCE

## CROSS-SECTION

DEPOSIT 3KA UNDOPED SILOX  
 PHOTO 6023-9 CONTACT WINDOWS  
 ETCH SILOX (3KA)  
 STRIP PHOTO RESIST  
 ETCH NITRIDE (1.8KA)  
 STRIP SILOX



DEPOSIT 4KA UNDOPED SILOX  
 DEPOSIT 6KA LIGHTLY DOPED  
 SILOX (2%)

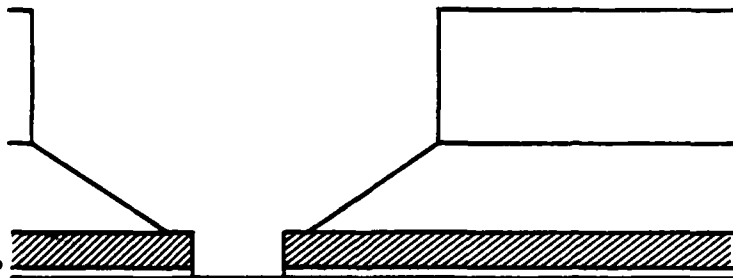


AFTER DEPOSITION OF UNDOPED AND DOPED SILOX

PHOTO 6023-12 GATE AND  
 CONTACT WINDOW

ETCH SILOX (10KA)

PREMETAL CLEAN  
 INCLUDES 10SEC 100: 1HF DIP



AFTER ETCH OF SILOX

METALLIZATION 10-12KA A1

52338

FIGURE 3.3-11 BASELINE CONTACT WINDOW PROCESS SEQUENCE



METAL OVER SILOX INTO CONTACT WINDOW AT MT

SEM AT 15,000X

PSM LOT-WF: 3756-9, 8-10-78

52492

CONTACT WINDOW BY BASELINE PROCESS

FIGURE 3.3-12

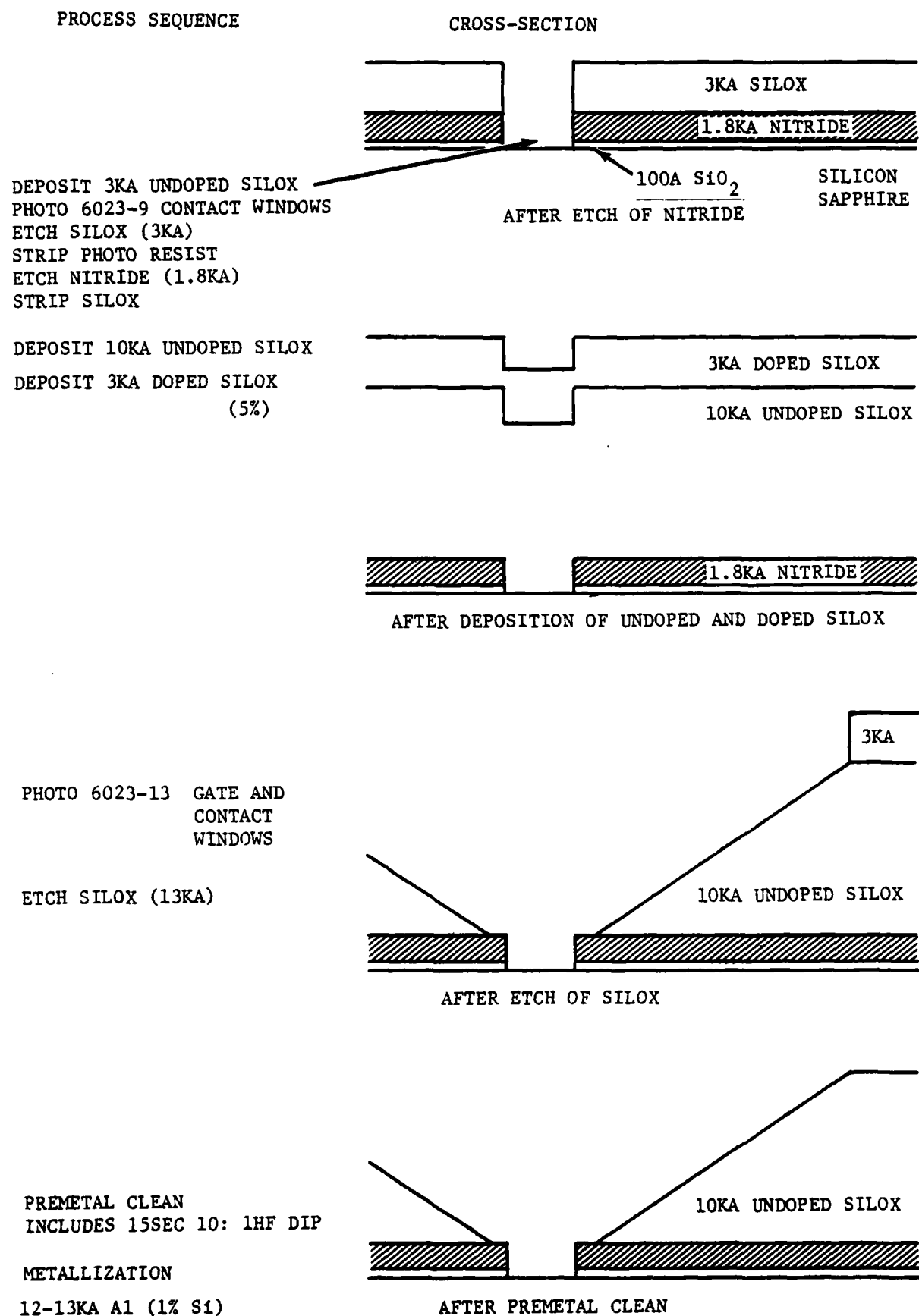
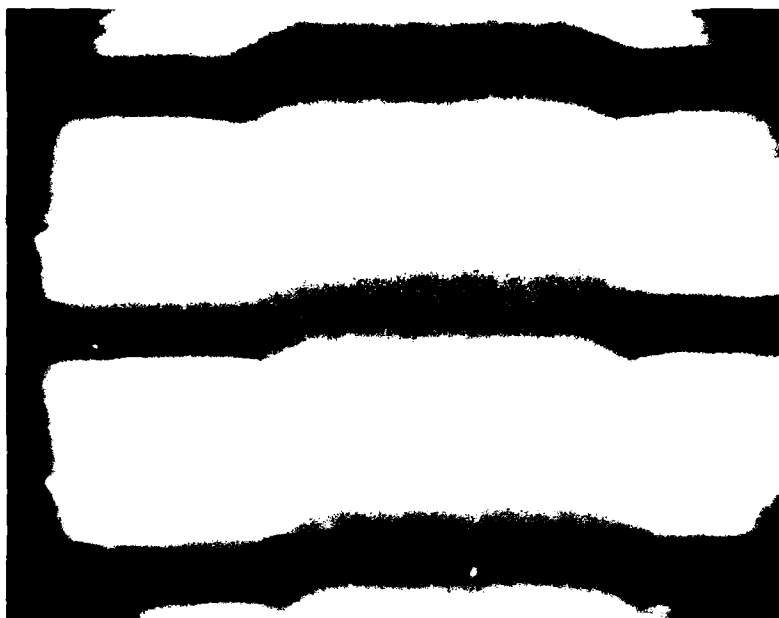


FIGURE 3.3-13 MODIFIED CONTACT WINDOW PROCESS SEQUENCE

52339

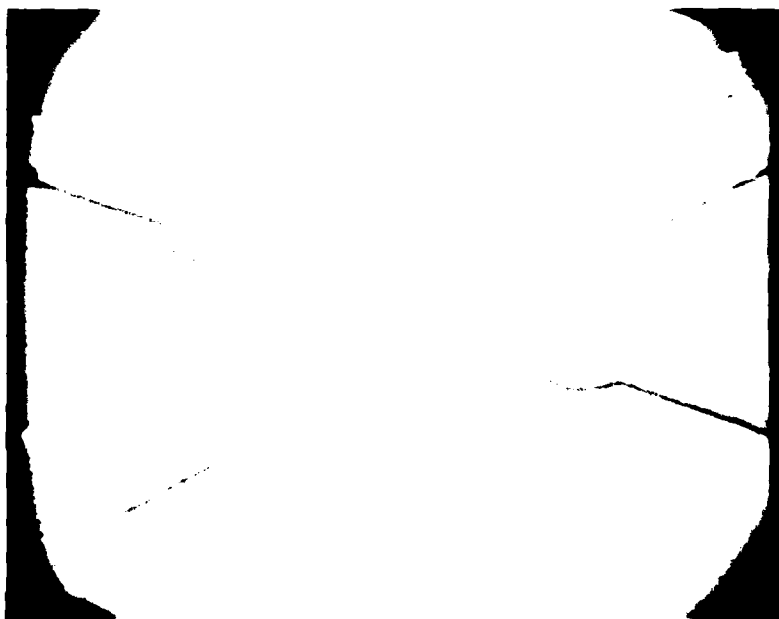
**NORTHROP**

Electronics Division



METAL OVER OXIDE BETWEEN GATE WINDOW, MI/GW TEST PATTERN  
SEM AT 5000X

PSM LOT-WF: 3888-7, 11-17-78



CONTACT WINDOWS BY NEW STANDARD PROCESS

FIGURE 3.3-14

52493

## 3.3.3 MNOS-CMOS/SOS Process for TSM

### 3.3.3.1 MNOS-CMOS/SOS Process Refinement

Desire for a compatible MNOS-CMOS/SOS process for all memory and logic devices served as an overriding goal for all process development described above. The requirements of the TSM were kept in mind during all process definition for the PSM. The TSM uses CMOS circuitry in addition to the MNOS memory transistors. Hence p-channel enhancement mode and n-channel enhancement mode (PEMT and NEMT) transistors are required. This contrasts with PSM requirements for p-channel enhancement mode and n-channel depletion mode (PEMT and NDMT) transistors.

As a result of this effort, the process developed and described for providing the PEMT and NDMT of the PSM can also be used to provide the NEMT of the TSM and any CMOS nonmemory logic devices.

### 3.3.3.2 MNOS-CMOS/SOS Process Sequence

The modified process sequence shown above for the PSM provides PEMT and NEMT for the TSM by the omission of the masking step (PC-2) and subsequent n-(depletion load) implant that shifts the  $V_{TN}$  for the PSM. Table 3.3.-8 compares the essential steps of each process sequence.

TABLE 3.3.-8 MX ACT 1 MNOS-CMOS/SOS PROCESS SEQUENCE

MODIFIED SEQUENCE	MNOS PSM	MNOS-CMOS TSM	CMOS LOGIC
N+ by P Diff 950C	✓	✓	✓
P+ by B Diff 980C	✓	✓	✓
Strip GP Nitride $H_3PO_4$	✓	✓	✓
P- By B Implant 180KeV	✓	✓	✓
80 KeV	x	✓	✓
N- By P Implant 100KeV	✓	x	x
Anneal Implant 900C	✓	✓	✓
Gate Oxide 80A	✓	✓	✓
Nonmemory Nitride 1300A	✓	✓	✓
Etch Nonmemory Nitride	✓	✓	x
Memory Nitride 510A	✓	✓	x
Masking Steps	11	10	9

This process has been proven out by the fabrication of several lots of TSM devices on a related contract:

Spaceborne Computer Temporary Store Memory Program,  
Raytheon Subcontract 53-0075-SZ-02255, SAMSO/YAD

Contract No. F04071-75-C-0149.

### 3.3.4 CMOS/SOS Process Sequence

As shown in Table 3.3-8 above, by omission of the depletion load implant Mask (PC-2) and subsequent phosphorus (n-) implant as well as the memory window mask (PC-8) and memory nitride deposition, non-memory CMOS devices can be produced. The non-memory nitride thickness is not increased in this CMOS process to the sum of the nonmemory plus memory thickness that occurs in PSM nonmemory devices. Increasing the thickness becomes unnecessary because CMOS devices operate on a single and lower voltage (+12V) supply and so have less field stress than some nonmemory transistors in the PSM and TSM which are subjected to 30V.

## 4.0 Transient Radiation Test Results

This section summarizes transient radiation testing conducted on ACT I devices. Results of total dose ( $CO^{60}$ ) and neutron testing is addressed in sections 2 and 3 of this report. Figure 4-1 identifies the device types exposed to transient radiation on this program. Due to funding constraints, only the MPROM and PSM were tested in these environments.

Figure 4-1 ACT I Transient Radiation Tests

	<u>UPSET</u>	<u>SURVIVAL</u>
MPROM	Section 4.1-1	Section 4.1.2
GPU	Not Tested	Not Tested
PSM	Section 4.2.1	Not Tested
TSM	Not Tested	Not Tested

## 4.1 MPROM Transient Results

### 4.1.1 Upset Level

Upset radiation test (short pulse) were conducted at Northrop's Febetron 705 FXR. Measurements used Northrop's Radiation Test System comprised of the Mustang, HSDAS (High Speed Data Acquisition System), a cassette and Alpha 16 minicomputer.

MPROM devices were operated at a 500 nsec cycle time and exposed to the 30 nsec radiation pulse at critical areas in its cycle. Tests were run at minimum and maximum  $V_{dd}$  (10 volts and 13 volts). Address of the first cycle was changed to include the four values for predicted worst case "0" in each output, and four values for worst case "1". Response was recorded off the first ten words on scope. Part was then cycled through eight repeating addresses and address cycle expanded to 16, 32, 64 and all 256 words.

Fourteen (14) MPR0M's from two lots were tested with upset levels observed at 5-7 times requirement and 2-3 times predicted level. Parts which had received a prior total dose performed similar to "virgin" parts. Upset thresholds also were independent of changes in  $V_{dd}$ . Figures 4.2-4.7 provide additional information.

Wide pulse tests were conducted at the EGG LINAC on seventeen (17) MPR0M's from four lots. The majority of these parts upset in the range of 2-5 times requirement, although two parts from one lot were inferior. These devices integrated the usec pulse and blocked. Analysis showed that this lot originated from a different boule epi and exhibited excessive initial leakage (100X).

SN	LOT CODE	PRE CONDITION	NO. ADDRESSES TESTED	NO. TESTS
3625	3172	Co60	1	3
3634	3172	New	3	22
3635	3172	New	3	32
3637	3172	New	4	29
3638	3172	New	4	52
3640	3172	New	3	23
3648	3172	New	3	23
3636	3172	New	8	40
3673	3169	New	8	28
3655	3169	Co60	8	29
3657	3169	New	1	3
3658	3169	New	1	3
3666	3169	New	1	3
3678	3169	New	1	3
TOTALS	14 Parts			293

FIGURE 4.2 MPROM FLASH X-RAY TEST - PART SUMMARY

S/N 3638 ADDRESS 000

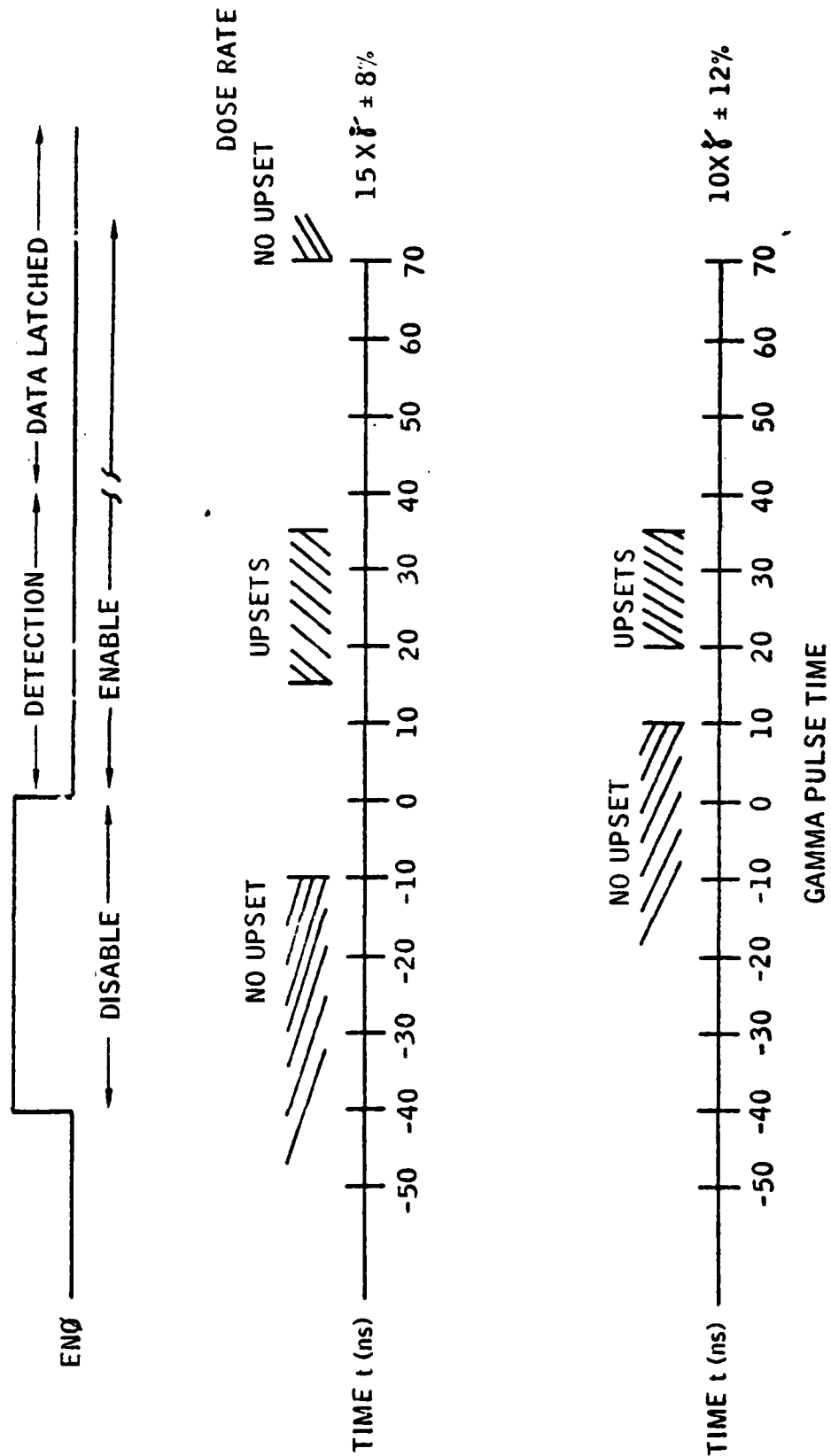


FIGURE 4.3 ROM UPSET WINDOW VS. DOSE RATE

## MINIMUM UPSET LEVEL DISTRIBUTION

10 PARTS UPSET  
4 PARTS NO UPSET (LOT CODES: 2-3169; 2-3172) <20 $\dot{\gamma}$

$V_{DD} = 10V$  (PREDICTED WORST CASE)

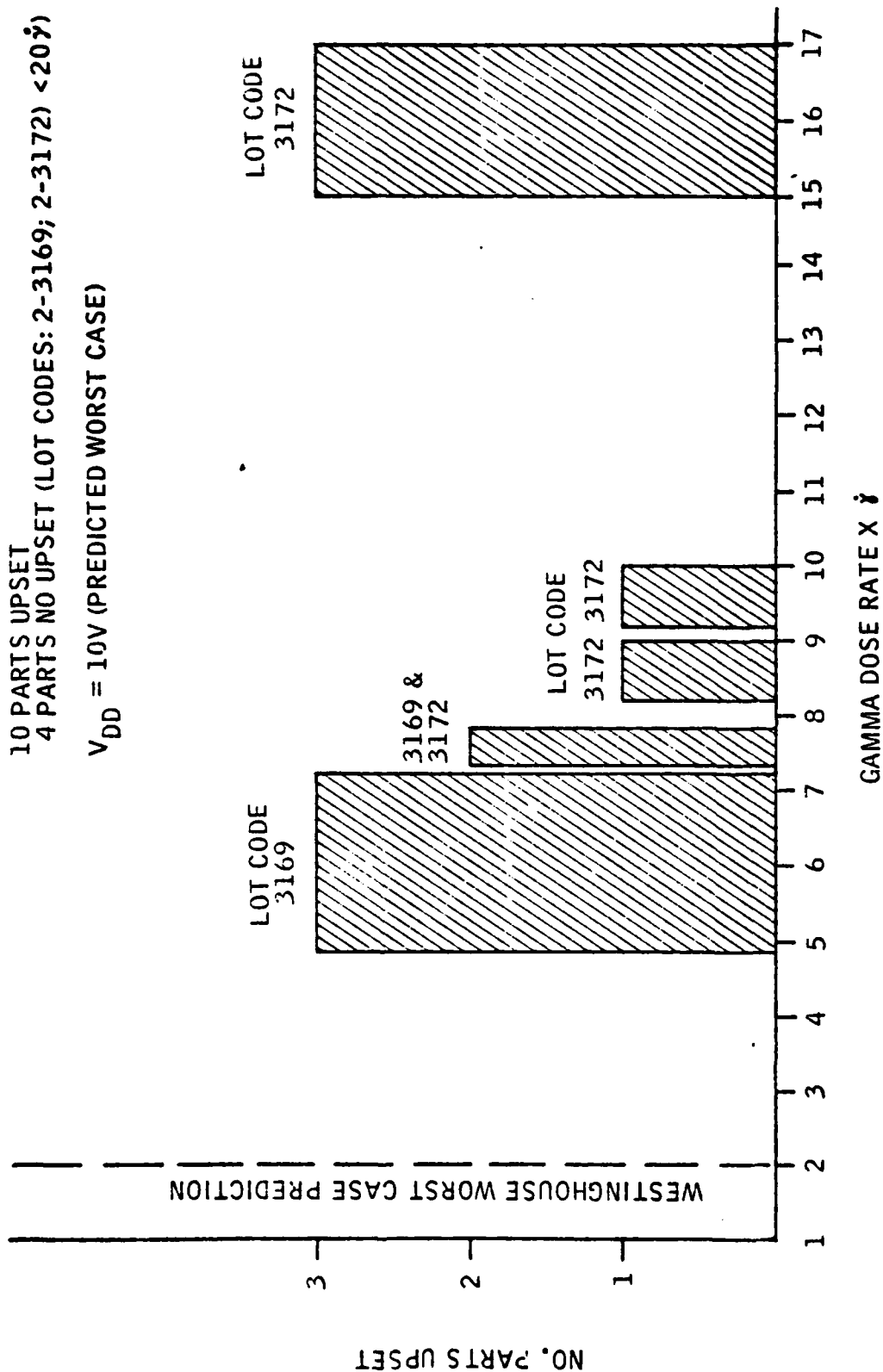
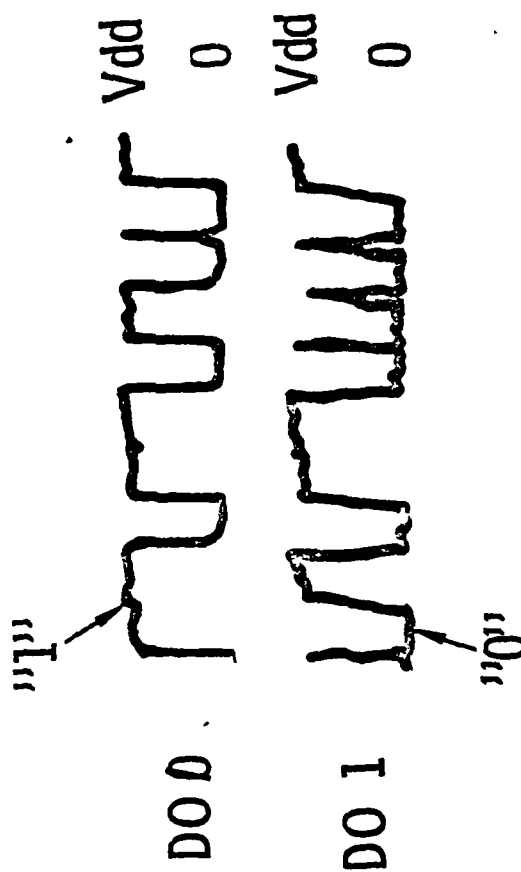


FIGURE 4.4 MP/ROM FLASH X-RAY

30 ns flash x-ray pulse, timed at  $t=20$  ns  
 Shot 2, Level 33  $\hat{y}$ , S/N 3638 Lot 3172 WF7



D0 0 has "1" in first address, upset from expected "0"

FIGURE 4.5 TYPICAL MP/ROM UPSET

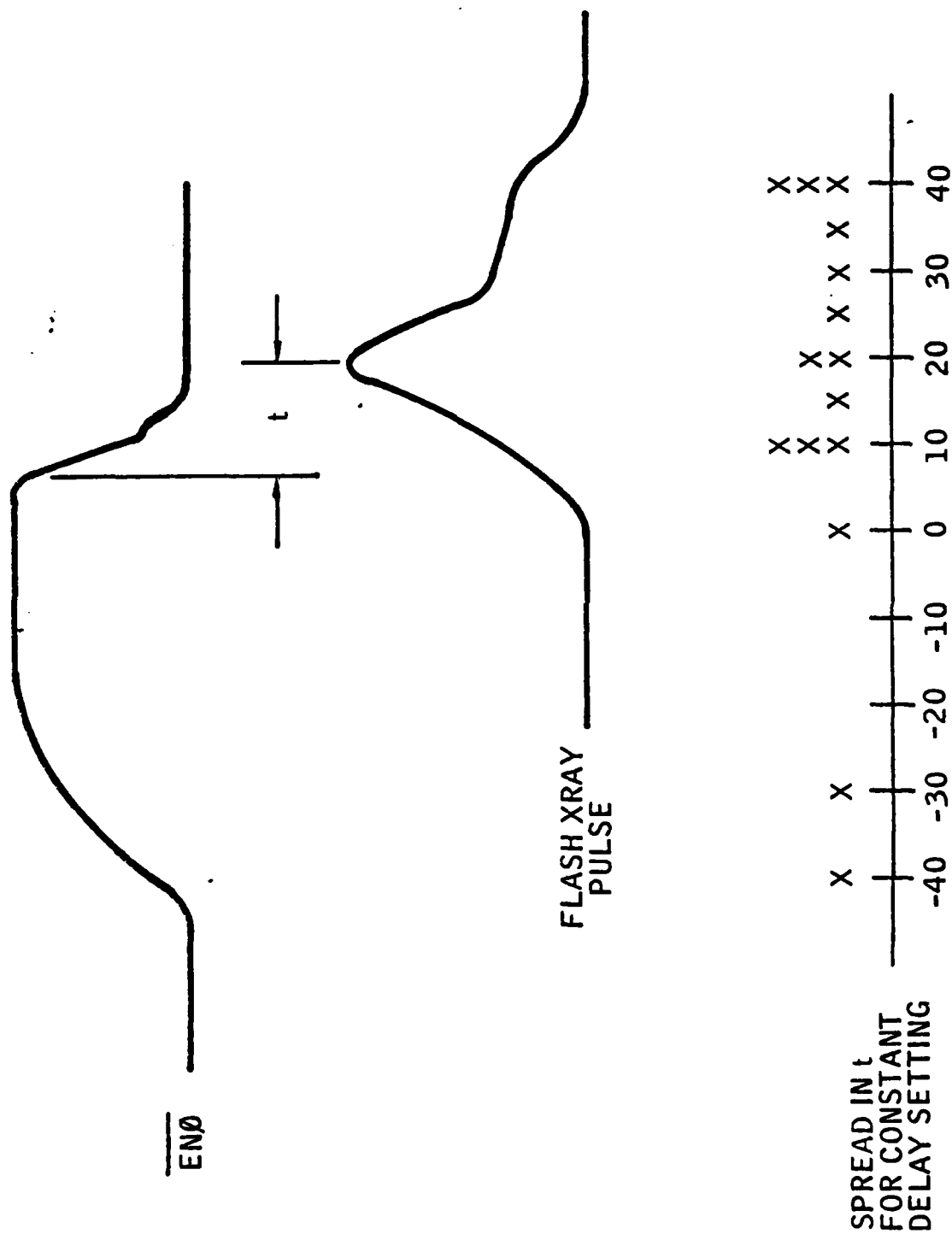


FIGURE 4.6 FLASH XRAY TIMING JITTER

Table of interesting addresses for threshold upset, timed 0 to 50 ns after ENØ fail

ADDRESS	D03	D02	D01	D00
0	T	T	H	W, Ø
20	T	T	W, 1	H
40	W, Ø	T	T	H
60	H	T	T	W, 1
9F	W, 1	H	T	T
BF	H	W, Ø	T	T
DF	T	W, 1	H	T
CO	T	H	W, Ø	T

W = Worse case upset cell

T = Typical, balanced cell

H = Hard to upset, enhanced by gamma dot

Ø is correct when low

1 is correct when high

FIGURE 4.7 ROM ADDRESSES USED FOR FXR YTH TESTS

# MP/ROM DOSE RATE SURVIVABLE TESTS, E-BEAM

FIGURE 4.8

<u>LOT</u>	<u>WAFER</u>	<u>S/N</u>	<u>TIME</u>	<u>SHOT V<sub>dd</sub></u>	<u>ENØ/T<sub>acc</sub></u>	<u>NOTE</u>
3172	7	3632	1/27	10V, 10V	50/100ns	perfect, L1.75
3172	7	3638	1/28	10V	50/103ns	perfect, L1.34 from $\gamma$
3172	7	3640	1/28	10V	50/87ns	perfect, L1.13 from $\gamma$
3172	7	3643	1/28	10V	74/140ns	perfect, L3.98 from TD
3172	7	3644	1/27	10V, 10V	74/110ns	perfect, L2.84
3172	7	3648	1/28	10V	74/100ns	perfect, L1.21
3172	7	3650	1/27	10V, 10V, 10V, 10V	74/120ns	column 8 failed, L6.5
3169	5	3683	1/28	11V, 12V	74/110ns	perfect, L2.47
3169	5	3684	1/28	11V, 12V	74/105ns	perfect, L2.80

### 4.1.2 Survival Level

Survival level radiation testing was conducted on the MPROM at Northrop's Febetron 705 in the E-Beam mode using the IRT drift tube. Instrumentation was as before using Mustang, HSDAS, and Alpha 16.

Nine (9) parts were exposed at two levels in the E-Beam environment. No latch up was observed, but one part exhibited a partial failure. Recovery time of less than 500 nsec was observed. System noise prevented better resolution of recovery times. Previous testing indicates recovery time of approximately 100 nsec.

### 4.2 PSM Transient Results

#### 4.2.1 Upset Level

Two transient test series were conducted on the ACT I PSM. Initial transients tests were performed in 1976 on Westinghouse mask number 6013 devices. Short pulse upset tests were conducted at Northrop's Febetron 705 Flash X-Ray (FXR) facility. Ten (10) devices were exposed at multiple subcycle times including a) before CS fall during initialization precharge b) during the sensitive detection interval with balanced memory currents and c) during the post detection latched interval. Several combinations of row and column addresses were exposed and all words were checked (less masks) immediately after exposure. No upset of any memory word was observed either during or immediately following maximum FXR output of  $10^{10}$  rad(si)/sec.

Wide pulse upset tests were conducted on 6014 PSM's at the ERDA Linac at EG&G in Goleta, California. Operating in the x-ray mode using the 18 MEV part, 111 shots were taken on ten (10) PSM devices. Several devices exhibited upset in this environment, thus a redesign was undertaken.

When the PSM was redesigned to Westinghouse mask number 6023, Flash X-ray tests were again run to verify the design. When exercised as described above, no upsets were observed at maximum output of the Febetron 705 in the gamma mode.

#### 4.2.2 Survival

No survival level radiation tests were performed on the PSM due to resource limitations.

## 5.0 Summary and Recommendations

The goal of the ACT I program was to demonstrate the maturity of CMOS/SOS and MNOS/SOS technologies. This demonstration was to be validated through design, manufacturing and test of candidate LSIC devices. After initial SSIC and test vehicle efforts four such device were attempted, as described in the text. Reasonable success was achieved in three (3) of these efforts; the fourth - an MNOS/SOS RAM device was not successful in meeting specified performance during the period of this contract. Development of the device was continued under RADC/CRL sponsorship.

The Mask Programmable Read Only Memory (MPROM) was the first LSIC device produced. It was also the smallest and predictably achieved the highest yield. It met pre and post rad performance requirements acceptably; this device was exposed to all specified radiation environments including short-pulse transient upset and survivability (Febetron 705) long-pulse transient (LINAC), total ionizing dose ( $CO_{60}$ ), Neutrons (TRIGA) and EMP (Northrop CARTS). The results indicate that this device indeed achieved desired maturity, and could be used as is, or with minor modification, in strategic systems.

A second CMOS/SOS device - The General Purpose Unit or 4-Bit Slice - achieved reasonable design maturity, and was built in small quantity. Subsequent to electrical truth-table and total dose testing, this device effort was discontinued for financial reasons, most of the goals for the device being demonstrated by the MPROM.

The Permanent Store Memory (PSM, also described as an Electrically Alterable Read Only Memory (EAROM) was produced in two (2) versions. The original design was produced with Atmospheric Pressure Nitride Deposition (APCVD); a redesigned device was built with Low Pressure Nitride Deposition (LPCVD). After significant learning problems associated with the LPCVD process, the yield of the device was re-established. The original design was found to be generally suitable in the radiation environment; the redesign corrected known problems and incorporated protect networks on inputs and outputs. The revised design performed without upset at maximum transient gamma levels at the Northrop Febetron.

The last device, the NMOS/SOS Temporary Store Memory (TSM) or, alternately, RAM represented the most difficult challenge. Device growth problems led to a decision to change the organization from 256X2 to 512X1. This design was produced in several lots some of which produced fully functional devices. These generally functioned with write cycle times greater than specified; several devices were observed to operate at or near the specified cycle time. Program funding limits prevented a thorough investigation of the underlying phenomena restricting device performance and the conclusion must be stated; that design and manufacture of a rad-hard MNOS/SOS RAM remains problematic.

Despite the various performance levels achieved by the ACT I devices, several conclusions may be stated:

- 1) The performance, stability and hardness of the CMOS/SOS technology was consistent with the ACT I objectives.
- 2) The performance, stability and hardness of the MNOS/SOS PSM device was consistent with the ACT I objectives.
- 3) Performance and hardness of the MNOS/SOS RAM was only partially achieved, and no life test for stability was attempted.
- 4) The key to any MOS computer lies in the memory area. All problems, including those related solely to CMOS/SOS, are observed on MNOS/SOS memory devices due to the presence of peripheral decoding/addressing/ buffering elements on memory devices.
- 5) Device size of the ACT I Memory parts was allowed to grow for various reasons, to the point of vanishing yield. Die size of the PSM (EAROM) approached 62,000 mils, a size inconsistent with optimum yield. The reasons for this included the provisions for random access read and write (as opposed to block clear), inclusion of desired but not required features such as the memory test feature, extremely conservative design rules (7 micron), inclusion of input protect networks on every vulnerable input or output, and edge protection for all MNOS transistors. Each of these, while desirable, resulted in a device geometry not suitable for volume production.
- 6) Nevertheless, the results confirmed the potential of the SOS technology for meeting difficult radiation environments, and simultaneously, the problems associated with SOS processing.

### Recommendations for Future Efforts

Since ACT I was "one of a series" of programs dealing with the MOS/SOS technology, it would be appropriate to describe those efforts which would establish or enhance the capability of the technology. These are, in rough order of priority:

- 1) Back channel leakage, and the general issue of epitaxial quality is not well understood. There appeared during ACT I the trend that parts performing well in low-level  $\text{Co}^{60}$  test against the back-channel leakage effect, would perform well in total dose and transient testing. The significance of this to any hardness assurance effort is apparent.
- 2) Redesign of the PSM (EAROM) appears a high priority item for any continuation. Since the ACT I parts were built the ACT team at Westinghouse has produced a bulk MNOS 1k by 1 EAROM device with reasonable electrical and radiation performance and with excellent yield. This was achieved largely by building on the ACT I experience. The device was kept to a fraction the size of the ACT I EAROM and achieved yields approaching an order of magnitude improvement over the ACT experience. The goals for an MNOS/SOS EAROM redesign should be to utilize present day design rules and selected organization changes to reduce size considerably.
- 3) Memory threshold testing was accomplished on a laboratory basis on selected bits of PSM and TSM devices at Westinghouse. While this testing was indicative of successful retention/endurance products, a great deal of work remains to be done to characterize this phenomenon. Northrop, during ACT I, created a company-owned tester capable of characterizing every memory bit on an entire device automatically. Such a program should be a basic part of any MNOS continuation, whether bulk or SOS, and should encompass all bits on a given device, rather than selected bits, rows or columns. The ability to contemplate such an effort is a direct result of the ACT I decision to provide the memory test feature and the test equipment necessary to rapidly characterize the device.
- 4) Additional device lots should be run, of present or new designs to improve and establish yield. Significant quantities of such devices should be screened and life tested to establish device reliability.

Since the BMO is presently heavily committed to a bipolar MX Flight Computer, an Air Force Materials Laboratory (AFML) Manufacturing Technology program is a logical vehicle for this support. A thorough reliability and hardness evaluation by Rome Air Development Center (RADC) on these next generation LSIC devices is also recommended.

Upon a successful demonstration of the objectives above, these devices could be considered for Full Scale Development of strategic systems. A lower-cost

LSI MX Computer then could result in an attractive alternative to the existing bipolar dielectrically isolated SSI/MSI computer with its attendant memory restrictions.

## APPENDIX A

During the developments on the ACT-I program, five technical papers were written by various members of the team at Westinghouse and Northrop Corporation. The papers were presented, or published, at several technical conferences or industry workshops and described the novel accomplishments and test results. Copies of the papers are attached in this appendix.

ROM and General Processor Unit

Hardened MNOS/SOS Electrically Reprogramable Nonvolatile  
Memory

CMOS/SOS LSI Input/Output Protection Networks

Built-in Memory Cell Test Feature for a Radiation Hardened  
1024 Bit MNOS/SOS Electrically Programable Nonvolatile  
Memory

Radiation Hardened MNOS - CMOS/SOS Fast Write RAM

# RADIATION HARDENED CMNOS/SOS MASK PROGRAMMABLE ROM AND GENERAL PROCESSOR UNIT\*

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## ABSTRACT

A low temperature CMOS/SOS process has been developed to minimize threshold voltage shifts and back channel leakage currents caused by radiation and temperature-bias stress conditions. Dual dielectric gate structures using CVD nitride 1300 Å thick on thermally grown SiO<sub>2</sub> 100 Å thick have been used to

minimize the oxidation time at high temperatures. The dual dielectric structure has been combined with a multiple boron ion implant,  $\phi = 3.5 \times 10^{12} \text{ cm}^{-2}$  at implant energies of 180 keV and 80 keV to produce n-channel enhancement devices with a graded boron profile with a maximum near the Al<sub>2</sub>O<sub>3</sub>-Si interface.

This process has been utilized to fabricate a 1024 bit mask-programmable ROM (MP/ROM) and general processor unit (GPU). This paper will discuss the organization and fabrication of the MP/ROM and GPU and present data for radiation hardness tests to both accumulated total dose and transient upset radiation

environments at levels of  $1 \times 10^6$  rad (Si) and  $> 10^{10}$  rad (Si)/sec (narrow pulse), respectively. Temperature bias stress data is presented which demonstrates device stability.

## INTRODUCTION

The nitride-oxide gate insulator technology developed for hardened nonvolatile MNOS semiconductor memory has been further developed for CMOS/SOS device<sup>1</sup> applications. Some of the features of the nitride-oxide technology are (a) the low temperature and short time oxidation and nitride deposition processes minimize out diffusion from the sapphire substrate; (b) the deposited gate insulator forms a reliable coverage of silicon island steps; (c) the nitride-oxide gate insulator is a very good surface passivation layer that is relatively insensitive to subsequent low temperature processing steps such as gate metalization; (d) radiation induced threshold shifts are directly proportional to the thickness of the nitride rather than the square of the thickness as for oxide insulators, thus larger gate voltages are possible<sup>1</sup>; (e) radiation induced threshold shifts are nearly the same for both positive and negative gate biases required for CMOS logic; (f) transient annealing times of nitride-oxide insulator after large total dose transient pulses are orders of magnitude shorter than for single oxide layers, and (g) the possibility of a nondestructive "radiation-thermal anneal" quality assurance test for hardness exists for nitride-oxide gate insulators.

The total dose hardness of this nitride/oxide development work is less than that reported for metal

gate - oxide SOS and bulk silicon technology.<sup>2, 3</sup> However, the superior transient annealing characteristics of the nitride-oxide gate insulator compared to oxide insulators<sup>4</sup> needs to be considered for some applications.

The total dose hardness already demonstrated is not indicative of a fundamental limitation of the performance of nitride-oxide gate insulators. Rather, these are the characteristics of a given set of nitride deposition and oxide growth conditions. There are indications of significant total dose hardness improvement by variation of these process conditions.

The low temperature CMNOS/SOS process has been utilized to fabricate a 1024 bit mask-programmable ROM (MP/ROM) and general processor unit (GPU). This paper will discuss the organization and fabrication of the MP/ROM and GPU and present data for radiation hardness to both accumulated total dose and transient upset radiation environments at levels of  $1 \times 10^6$  rad (Si) and  $> 10^{10}$  rad (Si)/sec, respectively. Temperature bias stress data is presented which demonstrates device stability. Neutron test results are also presented.

## FABRICATION OF CMOS/SOS LSI

Figure 1 is a cross section of the n-channel enhancement mode transistor utilized in the design of the MP/ROM LSI. The silicon islands are formed in a 0.5 micrometer n-type epitaxial layer on a sapphire substrate. Two boron implants are used to set the n-channel characteristics. The preradiation threshold voltage is determined by a  $3.5 \times 10^{12} \text{ cm}^{-2}$ , 80 keV boron implant resulting in  $V_{TN} = 2.5 \text{ V}$ . The

second implant,  $3.5 \times 10^{12} \text{ cm}^{-2}$ , 180 keV, is used to grade the boron profile in the silicon so that the peak occurs at the silicon-sapphire interface. This boron concentration is utilized to minimize the back channel leakage induced in n-channel devices by ionizing radiation. The N<sup>+</sup> and P<sup>+</sup> source and drain regions are formed by diffusion prior to gate dielectric deposition. A silicon nitride film is utilized as the diffusion masking layer, resulting in "pseudo - self - aligned" gate structures. To minimize the shift in threshold voltages for both n and p-channel devices, a silicon nitride - silicon dioxide (nit/ox) dual dielectric gate structure is used. The oxide thickness is 80 - 100 Å, with a layer of 1300 Å silicon nitride, resulting in an effective oxide thickness of 900 Å. The thin oxide layer minimizes the capture volume presented to the radiation environments, thus reducing the positive charge buildup in the gate insulator.

The oxide is grown at 900C, and utilizes ultra clean oxidation technology. The final interconnect is an aluminum metalization, resulting in a final gate length of 3 micrometers, with a gate overlap of 1 micrometer. The process has nominal alignment tolerances of  $\pm 2$  micrometers, with minimum metal spacing of micrometers, and minimum silicon island spaces of 6 micrometers. Source - substrate contacts are utilized to minimize the kink effect and threshold hysteresis inherent with CMOS/SOS devices.

Photographs of the MP/ROM and GPU using the metal gate CMOS/SOS process described above are shown in figures 2a and 2b. Since conservative mask and device design rules were used, allowance was made for radiation-induced mobility reductions, large output drive currents were needed and extra test points were bonded out for each device, the device density is not optimized and is less than for commercial LSI devices.

### MP/ROM FUNCTIONAL DESCRIPTION

The mask-programmable, "read-only" memory is organized to store 256 words of 4 bits each. A block diagram of the MP/ROM is shown in figure 3. The desired bit pattern is incorporated into the part during fabrication at the metal interconnect level. Eight address inputs determine the word to be read and four 3-state buffers provide outputs capable of driving 15pf loads in 10ns at a supply voltage of 10V. For operation of more than one MP/ROM on the same 4-bit data bus, the outputs of the parts not addressed are prevented from driving or loading the bus by setting a "Chip Select" input (CS) at the high level. When this control input is low, the part outputs the addressed word. A pair of enable inputs are used to operate the internal decode and read circuitry: either or both ( $\overline{EN}_1$  &  $\overline{EN}_2$ ) must cycle high-low with each address change.

A useful feature of this MP/ROM is a "Data Ready" output ( $\overline{DR}$ ). It signals when all four data outputs are correct, i.e., when the data is valid and is available to be read. It can be used to strobe the output into a register or it can serve as the enable signal to a second tier of MP/ROM's which are addressed by outputs of a first tier of MP/ROM's. Because the 8-bit address would come from two MP/ROM's, two enable inputs are accepted ( $\overline{EN}_1$  and  $\overline{EN}_2$ ). The second tier MP/ROM would not be enabled until both  $\overline{DR}$  inputs were low. When not needed, one enable input can be tied low.

The internal organization of this 1024-bit ROM is 32 rows by 32 columns. The five least significant address bits (A0 - A4) are decoded to select one of 32 rows; the remaining three address bits (A5 - A7) select one of eight columns for each of the four outputs. The "Chip Select" input (CS) can serve as the ninth bit of address and is used if more than one ROM outputs to the same 4-bit data bus, to provide more than 256 words. The CS signal inputs to the 3-state output buffers only. When CS is high, the buffers are forced into a high impedance state, neither driving nor significantly loading the bus, by turning off both the n- and p-channel output transistors. The response of the 3-state buffers to this CS input favors applications with two or more ROM's on a common data bus.

When selection is transferred from one ROM to another, the internal timing ensures that the overlap time during which both ROM's are in the active state is insignificant, thereby minimizing current surges on the supply lines.

The enable function serves to discharge decoders and to charge differential sense lines and bistable detect latches before responding to a new address. This design provides highly reliable operation with a minimum transistor count and insensitivity to radiation effects, either from threshold shifts, mobility degradation, or photocurrents.

The 1024-bit pattern is programmed during wafer fabrication at the metal interconnect level. The drain of each transistor in the 32 row by 32 column memory array is connected to either the "one" or "zero" column sense line of the detect latches by custom design of this portion of the interconnect pattern.

The key features and operational characteristics of the MP/ROM are detailed in table 1.

### MP/ROM DUAL RAIL MEMORY CELL

The memory for the MP/ROM is structured as 32 row by 32 column array. Both the row and column select circuits are n-channel decode trees, with the A4 - A0 address lines being decoded to 1 of 32 rows, and addresses A7 - A5 performing a 1 of 8 column decode, thus providing a 256x4 data pattern. Each of the decode trees is provided with a parallel p-channel ladder network to provide an active pull up to the supply voltage  $V_{DD}$  for all unaddressed rows and columns. This is essential to proper array operation during a transient upset radiation pulse, since no gate line should be left floating during such a pulse.

The MP/ROM data storage cell, column select and detect latch circuit are shown in figure 4. The decoded row and column address lines are set to select the proper data cell. The 1024-bit pattern is programmed during wafer fabrication at the metal interconnect level. The drain of each transistor in the 32 row by 32 column memory array is connected to either the "one" or "zero" column sense line of the detect latches by custom design of this portion of the interconnect pattern. To cycle through a desired address, the two column lines of the ROM cell and the two inputs of the detect latch are precharged to  $V_{DD}$ , thus setting both outputs of the latch to the high state. This is accomplished by the ENA signal which is derived internally from the two chip enable ( $\overline{EN}$ ) signals. Each detect latch serves eight columns of the array.

The ROM data cell which is addressed will be selected by the row decode lines, thus turning on the n-channel data transistor. Immediately prior to this, ENA is switched and the p-channel transistors which precharged the data lines are turned off. The selected column address will enable the proper column select switches, Y1, Y2, etc., in figure 4, in the detect latch input lines. The select switch will thus connect the programmed bit to the data latch. If the selected bit is programmed as a zero, the data transistor will discharge the LO line to  $V_{SS}$ , chip ground. If a ONE is programmed in the data cell, the L1 line will be discharged. Thus, the detect latch will be set and

DO will go low and high, respectively for a ZERO and ONE data bit. When the chip is deselected, e.g., a new address, the ENA signal will again precharge the L0 and L1 lines to  $V_{DD}$ , establishing the detect latch output levels for the succeeding address.

#### GPU FUNCTIONAL DESCRIPTION

The general processor unit (GPU) is a 4-bit slice of a central processor unit (CPU) architecture. A block diagram of the GPU is shown as figure 5. The GPU includes four registers, all clocked by the low-to-high transition of CL, the system synchronous clock. These registers are: a dual accumulator A1 & A2, an operand OPR and a multiplier MQR register. Associated with each register, and interconnected with many other blocks as well, is a multiplexer: an A MUX driven by the dual A register, a B MUX driven by the OPR, and an MQ MUX driven by the MQR. These provide selection between direct, complement, or shifted signals, or force a zero or one. A major block in the GPU is the arithmetic-logic circuit (ALC), which performs "add", "and", "or", and "exclusive or". The output of the ALC drives a fourth mux, the File MUX FX, which provides direct or shifted outputs.

Appropriate mux selections of the data paths between the four registers and the ALC provide all necessary arithmetic and logic operations including 2-bit at-a-time multiply. By means of buffered outputs from the registers and ALC and corresponding inputs to the mux's and ALC, data is transferred to and from adjacent GPU 4-bit slices of the CPU. These permit all operations with any multiple-of-four word length. Speed of the arithmetic operations is dependent upon word length because carry must propagate from the first GPU to the last. Logic operations run at a speed which is independent of word length.

The fifth mux, I/O MUX, selects the 4-bit data path to be outputted from the GPU via the 3-state output buffers to a 4-bit bidirectional data bus. The I/O MUX also causes deselect of the 3-state output buffer and admits input data from that same 4-bit data bus.

#### CMOS/SOS LSI SIMULATION

Extensive computer simulation of both the CMOS/SOS LSI's has been conducted to verify the proper operation of the circuit for worst-case conditions. For these parts, a prime consideration is to minimize the propagation delay for the worst-case condition of high temperature (125C) and post-radiation environments. The basic device operating requirements and mask design rules form the basis for the circuit design rules. The effects of minimum supply voltage, external capacitive drive capability, internal nodal capacitance, and process variations must all be factored into the design equations. Also, especially for the GPU, logic gate complexity must be limited, preferably to 4 inputs or less, to minimize input capacitance, reduce total channel width, and simplify the LSI layout routines.

To optimize the device model used to simulate the LSI circuits, particular attention must be paid to properly identifying individual transistor parameters and what are the worst-case conditions for the LSI operation. A conservative approach is essential to

ensure proper operation of the LSI in its worst-case environments, i.e., post radiation and high ambient temperature. The actual device parameters, design equations and computer simulation have matured through several iterations. In particular, determination of worst-case shifts in threshold voltage, post-radiation mobilities, and short channel effects upon device operation must be analyzed.

These effects upon the circuit are used as input to the simulation through the device model utilized.

ISPICE circuit analysis programs<sup>5</sup> have been used to simulate the LSI circuits, both for preradiation, 25C environments and for postradiation, both total dose and transient upset, high temperature environments. In particular, the short channel lengths,  $L_0 \approx 3$

microns, required that the short channel MOSFET device model (SCMOSFET) be utilized to account for channel length modulation, voltage dependent gate-source and junction capacitances, and field dependent mobilities. Several methods of measuring the mobility were evaluated to optimize the fit of actual device characteristics to the model's characteristics. Mobility values obtained in the triode region ( $V_{DS} < V_{gs} - V_T$ ) and correlated to mobility in the pentode region provided excellent correlation between actual and predicted device characteristics. The measurements in the triode mode of transconduction versus gate bias,  $g_{ds}$  vs  $V_{gs}$ , yielded threshold data as well as the mobility. The mobility was determined from the slope,  $k'$ , and the threshold from the intercept, since  $g_{ds} = 2k'(V_{gs} - V_T)$ .

This measurement technique was used to evaluate the changes in threshold voltage and mobility for n- and p-channel devices for worst-case environments. Extensive testing of test vehicles allowed the accurate determination of  $\Delta V_T$  and mobility. The results were

$k'_n = 3.84 \times 10^{-6} \text{ A/V}^2$  (25C) and  $k'_p = 3.25 \times 10^{-6} \text{ A/V}^2$  (25C), preradiation for n- and p-channel devices respectively. At 25C, post total dose, the  $k'$  had degraded to  $2.6 \times 10^{-6} \text{ A/V}^2$  and  $2.2 \times 10^{-6} \text{ A/V}^2$ , respectively for  $k'_n$  and  $k'_p$ . Other degradation factors

were determined for high and low temperature operation and other environments.

These parameters were employed in the ISPICE device model to simulate the critical circuits of both the MP/ROM and GPU. Extensive testing of the MP/ROM and GPU to determine operational envelopes has shown the high degree of accuracy that has been incorporated into the ISPICE simulations, both pre and postradiation, and over wide temperature ranges.

#### ISPICE Simulation

An example of the ISPICE simulation performed for the MP/ROM is the modeling of the effects of the photocurrent generated in the MP/ROM array and detect latch due to a transient upset radiation pulse. Figure 6 is the circuit used to simulate the MP/ROM shown in figure 4. The timing for this circuit is such that the output of the detect latch, DO and  $\overline{DO}$ , is established by which sense line goes to  $V_{SS}$  first,

through the active n-channel device of the selected data cell, i.e., data line L1 or L0 is discharged to set the latch. In figure 6, the selected data bit has been programmed as one, thus when addressed the L1 line to the detect latch will be discharged. A resistor is used to model the loading of the selected L1 line to the column select switch. For transient radiation, a worst-case data bit will be when the addressed cell is connected to one data line; in this case, L1, and all 31 other transistors in the same column are programmed to the other data line, L0. Any photocurrent generated in the selected cell will aid in discharging the L1 input, while the photocurrents generated in the other 31 transistors will cause the L0 latch input to be discharged. Thus, the output state of the detect latch will be determined by the race between the "on" n-channel device and the photocurrent in the "off" devices in discharging L1 and L0, respectively.

To simulate these effects upon the array and detect latch caused by the photocurrents, a transistor is used as a model for the photocurrent generator. The 31 devices connected to L0 are simulated by a distributed RC network. The photocurrent generator is directly connected to the array side of the column select switch in the L0 sense line. L0 then will have a tendency to be discharged by the photocurrent generator. The ISPIICE simulation of this circuit is shown in figure 7 for a postradiation, 125C environment. The forcing function for this simulation is signal X1 and represents the ENA precharge signal, column select, and row decode signals. With the programmed bit set at one, L1 is discharged and D0 is set high. The effect of the photocurrent generator is seen in the signal L0. The photocurrents cause L0 to be discharged but L1 switching precedes the fall of L0, thus the relative timing required between L1 and L0 is preserved.

#### TOTAL GAMMA DOSE TEST

The CMOS/SOS LSI's developed have been characterized as to the operation in an ionizing radiation environment. For the total gamma dose tests of the MP/ROM, parts were subjected to doses exceeding  $1 \times 10^6$  Rad(Si) from a Co60 source at a dose rate of approximately 20K Rad(Si)/min. Figure 8 is a plot of the worst-case access time for the slowest bit in a given MP/ROM part versus total dose, measured approximately 1 hour after exposure. The data shown is for parts from several different wafers from separate process lots. The average change in access time was 0, 3, and 6 nanoseconds at total gamma dose levels of  $3 \times 10^5$ ,  $6 \times 10^5$  and  $1 \times 10^6$  Rad(Si), respectively, for a supply voltage of 10V and a 40pf output load test condition. During the irradiation, the devices were dynamically biased at a cycle frequency of 500 KHz and a supply voltage of 13V. The change in access time represents a nominal increase of only 8 percent at a dose level of  $1 \times 10^6$  Rad(Si). The operational characteristics of the MP/ROM are a reflection of the net changes occurring in the individual n- and p-channel transistors which comprise the LSI.

The GPU has also been subjected to total gamma dose tests exceeding  $6 \times 10^5$  Rad(Si). The propagation delay through the GPU for several data paths were measured pre and postradiation. Primarily, with the B MUX selection data line serving as the enable to the

ALU block, the delay to data out (DIO), zero detect (Z) and the ALU outputs (ALO), were characterized. During irradiation, the GPU under test was static-biased at a supply voltage of 13V. The part was clocked twice prior to irradiation to load all data registers in the data paths to be measured following a total dose exposure. Figure 9 is a plot of these selected propagation delays versus total dose. Following irradiation, the propagation delays were measured for a supply voltage of 10V and a nominal capacitive output loading of 20pF. As can be seen from this figure, there is essentially no change in the propagation delay along the measured paths through the GPU at levels of  $6 \times 10^5$  Rad(Si). This performance is typical of the critical timing paths present in the GPU operation.

#### Transient Radiation Tests

Short pulse width transient upset radiation tests have been conducted on the MP/ROM utilizing a flash-X-ray source (FXR). The LSI has been investigated for wide and narrow pulse transient upset versus timing and worst-case data patterns up to levels of  $2 \times 10^{10}$  Rad(Si)/sec. For a nominal pulse width of 30 nanoseconds, the test system utilized a 500 nanosecond cycle time with accurate access time strobing of the data stream into a high speed computerized data acquisition system. This allowed study of the transient annealing effects of the LSI. In all cases, independent of circuit timing, the transient threshold shifts due to photocharge generated in the gate dielectric by the ionizing radiation pulse had annealed out and the device under test was fully functional, with the correct data patterns within the 500 nanosecond period. This is of prime concern to systems which require minimum downtime following a transient radiation pulse.

Two interesting timing points in the MP/ROM were identified for transient upset radiation tests. Since the MP/ROM utilizes a dual rail dynamic detect circuit, i.e., a detect latching scheme, the inputs to the latches are both precharged to  $V_{DD}$  when the enable signal ( $\overline{EN}$ ) is high. The most critical time is between the time when  $\overline{EN}$  goes low releasing the precharge source from the data (lines) and the currently addressed memory cell is activated. At this time, the inputs to the detect latches are at  $V_{DD}$  and depending on the data in the array for that column, one input will be pulled to ground, thus setting the latch to the proper state. The effect of the transient upset radiation pulse is to generate photo current in the unaddressed n-channel memory devices. Thus, in a given column, transistors connected to the same detect latch input as the addressed bit will aid in setting the latch to the proper state, while the photocurrents in the devices connected to the other input, will try to set the latch to the opposite state. Upset will occur when the photocurrent generated in the opposite data input is able to discharge that node more rapidly than the addressed bit transistor, resulting in the wrong data being presented to the output buffer. The results of the narrow pulse width transient dose testing show that for this critical circuit timing and worst-case data patterns, upset did not occur for levels  $> 2 \times 10^9$  Rad(Si)/sec. The second interesting time is after the detect latches have been set and the

input lines to the MP/ROM begin the setup for the next data to be addressed. At this point, the decision on the output state of the detect latch has been made, and the new data will not be set into the latch until EN is cycled. Higher level,  $> 10^{10}$  Rad(Si)/sec. FXR E-beam tests showed this latter time to be much harder in the narrow detect timing described above. Figure 10 shows the response of the MP/ROM to a narrow transient pulse for two separate addresses.

#### Neutron Fluence Test

The primary effect of neutron irradiation upon a semiconductor is the creation of displacement damage in the bulk of the material<sup>6</sup>. This, in turn, results in a degradation of the minority carrier lifetime and bulk mobility. However, for MOS devices, these effects are minimized in that conduction in such devices is by majority carriers in a very thin channel at the surface of the semiconductor. Thus, a neutron fluence should have a minimal first order effect upon MOS devices.

A further reduction in the effects of a neutron fluence upon MOS devices is through the utilization of MOS/SOS technology. The capture volume subject to displacement damage is drastically reduced by using submicron epitaxial silicon layers, and further reduced by reducing the active silicon area with a given LSI. This is readily attainable since the epitaxial layers are selectively removed to form silicon islands. This reduces the capture cross section by nominally 7 percent.

Figure 11 is a plot of worst-case access time for a neutron fluence of  $5 \times 10^{14}$  N/cm<sup>2</sup>, with the device being stressed at zero bias. Also accumulated during the neutron dose is a background gamma total dose of  $2 \times 10^5$  Rad(Si). As can be seen from the data, there is virtually no change in the access time for this neutron fluence. This data confirms that CMOS/SOS device technology has a high degree of tolerance to high level neutron fluence environments.

#### Temperature Bias Stress Test

The CMOS/SOS LSI's are designed to operate over the full temperature range of -55C to +125C. To demonstrate the long term stability of the LSI's, the MP/ROM has been subjected to dynamic temperature bias stress (TBS) testing at 125C. The addresses are continuously cycled in an incremental manner to fully exercise the logic and memory array at a nominal rate of 500 KHz. At temperature, the supply voltage and input levels were set to 13V, and the output buffers are biased with an RC network to simulate worst-case loading effects. The parts are cooled to 25C for characterization while under dynamic bias to prevent any zero bias temperature anneal effects from influencing the data. The access time from chip enable (EN) to data ready (DR) and the slowest address in the memory array (DO) are measured, initially and after each increment of time at temperature. These measurements are done utilizing an automatic LSI test system, which allows complete characterization of the LSI's for both functional and parametric characteristics.

Figure 12 is the dynamic TBS data for the worst-case bit access time (DO) and data ready (DR) access time for 1000 hours of stress at +125C. The measurements were made at 25C, with a supply voltage of 10V and 40pf loading of the output buffers. Essentially, for the stress of 125C at 1000 hours, there is less than a 5 nanosecond variation in both access times. This represents a change of less than 5 percent in access time.

#### RADIATION, ANNEAL, AND STRESS TESTS

An interesting approach to verifying the radiation performance of delivered LSI circuits is to characterize the LSI's for radiation hardness and temperature stability after the parts have been irradiated and then annealed to remove the induced charge. If this can be done and reliable operation can be obtained, this technique provides a method by which the reliability of delivered LSI circuits can be determined virtually on an individual part basis.

To demonstrate this characteristic for the present CMOS/SOS LSI devices, a group of MP/ROM parts were irradiated to  $3 \times 10^5$  Rad(Si), under the dynamic stress described above, then annealed under zero bias at 200C for approximately 30 hours. The group was then split, and half the parts were irradiated to  $6 \times 10^5$  Rad(Si) and the other half were subjected to 168 hours of dynamically cycled temperature bias - stress. The worst-case access time for the MP/ROM is plotted versus the sequence of events the LSI in each group experienced in figure 13 for radiation + anneal + radiation and in figure 14 for radiation + anneal + temperature-bias-stress.

As can be seen in these figures, after 30 hours at 200C, all the parts had fully recovered from the effects of the ionizing radiation of  $3 \times 10^5$  Rad(Si). All the charge trapped in the gate insulator has been annealed out during this thermal cycle. Thus, the original characteristics are recoverable. (Note: several parts in the group were originally irradiated at levels up to  $1 \times 10^6$  Rad(Si). The data for the  $3 \times 10^5$  Rad(Si) exposure prior to the anneal is shown to facilitate comparison to the postanneal irradiations. Thus, the recovery to the original access times following the anneal represents more than just the return from a dose of  $3 \times 10^5$  Rad(Si).) Also, as figure 14 shows, the post anneal temperature bias stress data demonstrates the MP/ROM LSI is stable following this sequence of events.

Finally, figure 13 dramatically shows that not only have the initial access times been recovered, but the irradiation to  $3 \times 10^5$  Rad(Si) following the anneal tracks the data for the initial exposure. These characteristics for both series of events indicate that this technique may be a viable option to confirm the radiation properties of delivered CMOS/SOS LSI devices which use a nitride/oxide gate insulator. This may possibly be a new nondestructive radiation quality assurance test.

## ACKNOWLEDGEMENTS

The planning and process development by the process development group led by D. S. Herman, the discussion and performance of radiation tests by C. M. Modla and H. Kalapaca of Westinghouse; technical critiques by SAMSO, TRW and Quesstron advisors; support and encouragement by W. S. Corak and G. Strull; and program management by S. Stewart of Northrop and R. C. Lyman of Westinghouse, are gratefully acknowledged.

## REFERENCES

1. J. R. Cricchi, M. D. Fitzpatrick, F. C. Blaha and B. T. Ahlport, "Hardened MNOS/SOS Electrically Reprogrammable Non-Volatile Memory," 1977 IEEE Annual Conference on Nuclear and Space Radiation Effects, Paper C5, 13 July 1966. (Ref. this issue)
2. R. A. Kjar, S. N. Lee, R. K. Pancholy, J. L. Peel, "Self-Aligned Radiation Hard CMOS/SOS", IEEE Trans. Nuclear Science, NS 23 pp. 1610-12, December 1976.
3. G. F. Derbenwick, B. L. Gregory, "Process Optimization of Radiation Hardened CMOS Integrated Circuits," IEEE Trans. Nuclear Science, NS-22, pp. 2151-56, December 1975.
4. J. C. Pickel and R. A. Williams, "Prompt Radiation Damage and Short Term Annealing in CMOS/SOS Devices," Trans. Nuclear Science, NS 23, pp. 1623-28 December 1976.
5. ISPICE, National CSS, Inc., Norwalk, Conn.
6. K. G. Aubuchon, J. Bereisa, "Performance of Hardened CMOS Devices in Severe Neutron Environments," IEEE Trans. Nuclear Science, NS 19, 6, pp. 299-304 December 1972.

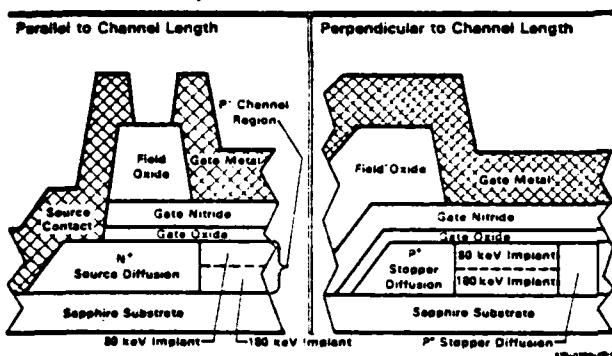


Figure 1. CMOS/SOS: Cross Section of N-Channel Enhancement Mode Transistor with Two-Level Boron Implant and Channel Stops to Reduce Channel Leakage

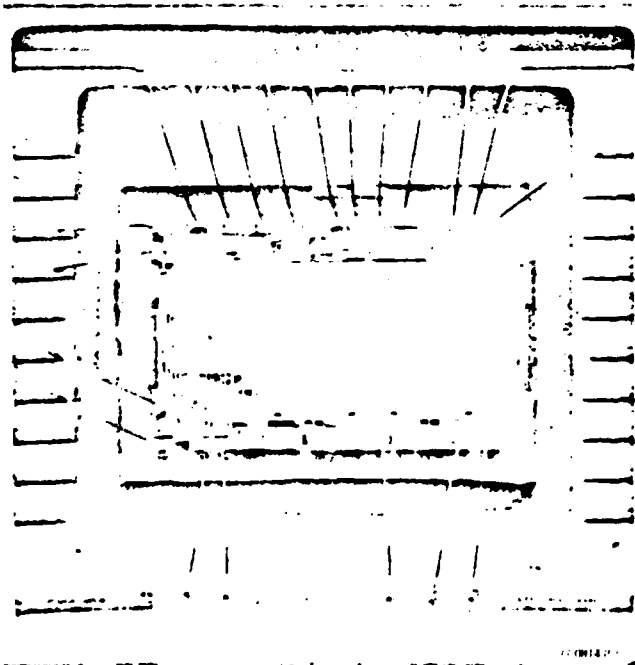


Figure 2A. Microphotograph of CMOS/SOS Mask Programmable ROM

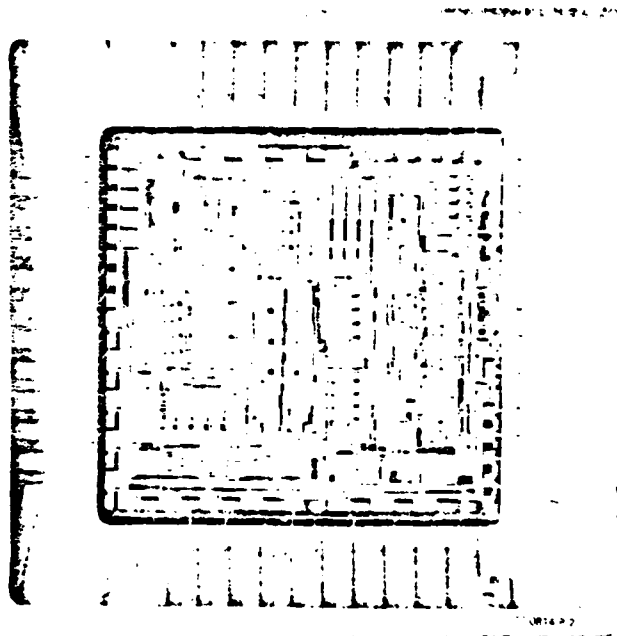


Figure 2B. Microphotograph of CMOS/SOS General Processor Unit

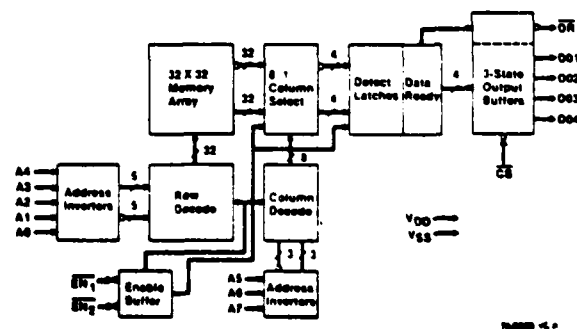


Figure 3. CMOS/SOS ROM Mask Programmable Organization for 256 Words by 4-Bits

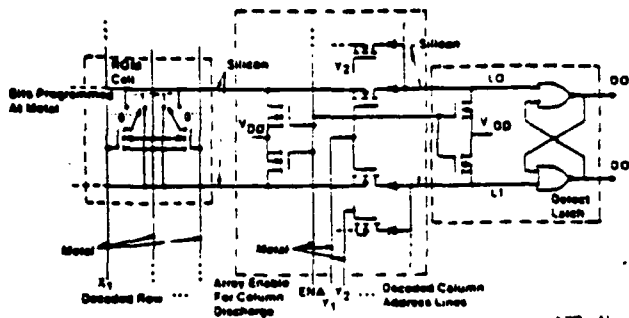


Figure 4. MP/ROM: Storage Cell, Column Select, and Detect Latch

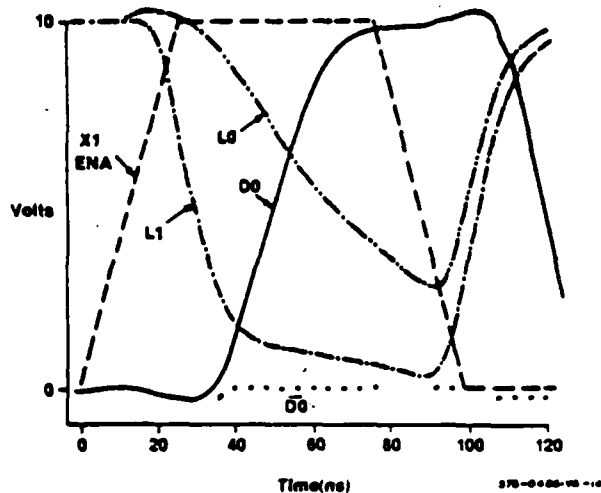


Figure 7. ROM Simulation of ROM Array with Photocurrent

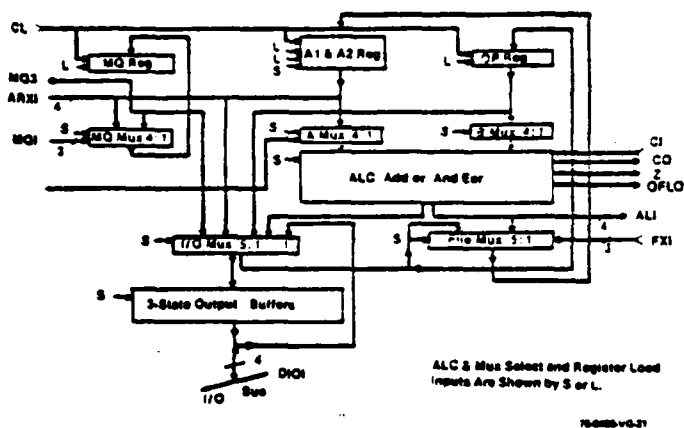


Figure 5. GPU Data Flow Diagram

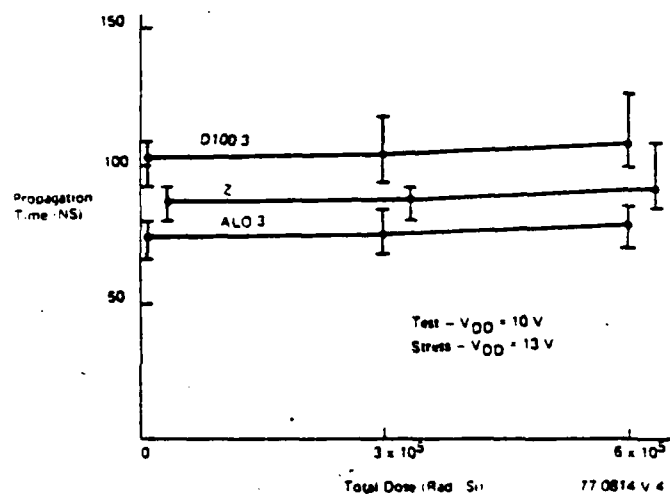


Figure 8. ROM: Access Time vs Total Dose

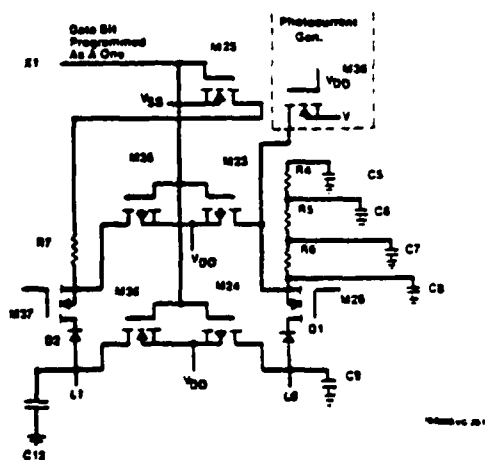


Figure 6. ROM: Simulation Circuit, Photocurrent

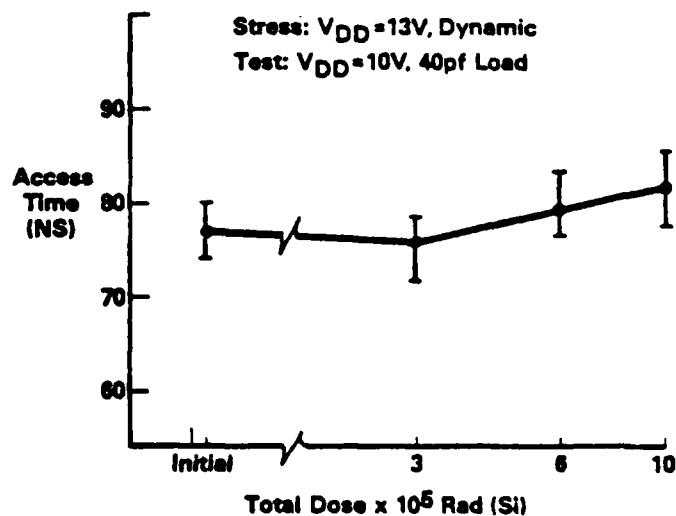


Figure 9. GPU Selected Propagation Delays (from BMUX SEL) vs Radiation, Static Bias

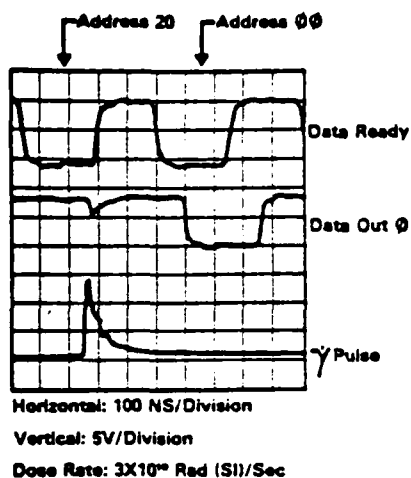


Figure 10. Febetron 705 Test (Gamma Mode) MP/ROM

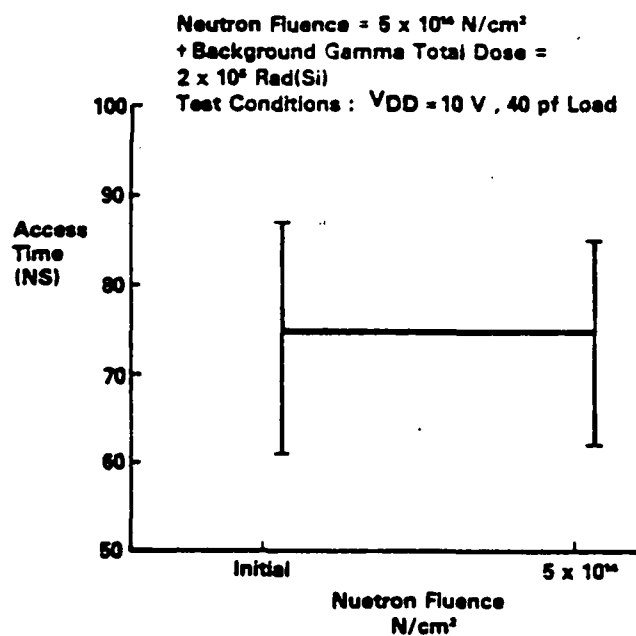


Figure 11. Access Time vs Neutron Fluence

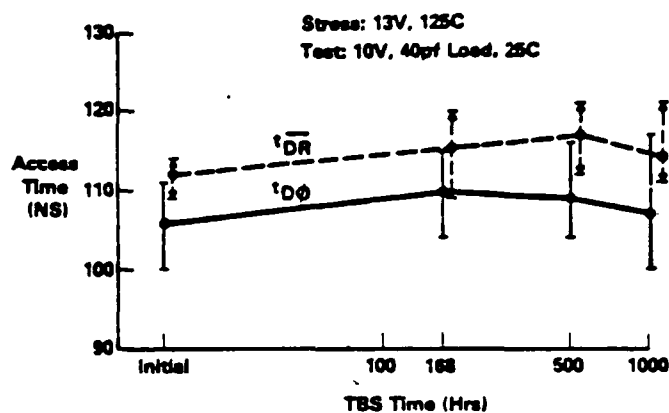


Figure 12. ROM: Access Time After Dynamic TBS-125C

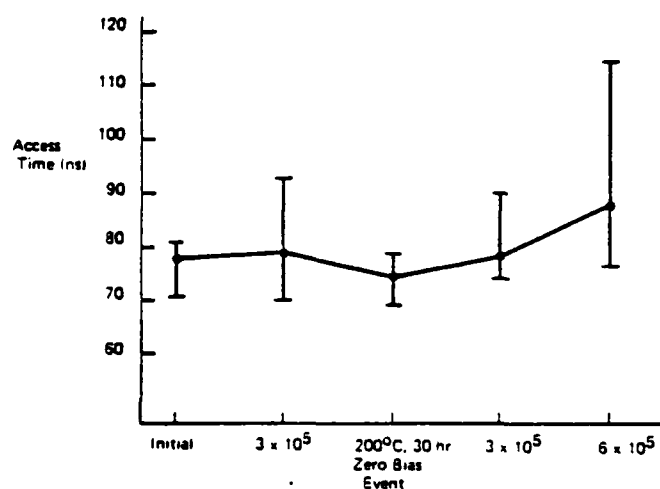


Figure 13. Access Time vs Anneal + Rad

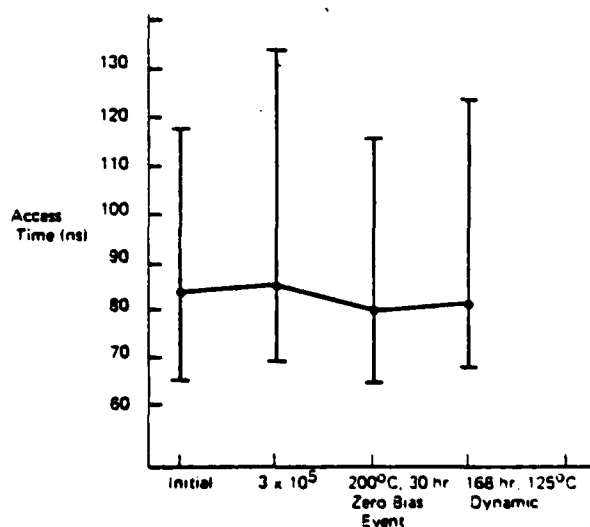


Figure 14. Access Time vs Anneal + TBS (125C)

# HARDENED MNOS/SOS ELECTRICALLY REPROGRAMMABLE NONVOLATILE MEMORY

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## Abstract

A random access  $256 \times 4$  MNOS/SOS nonvolatile memory has been designed, processed, and characterized. Significant advances have been made in radiation hard low power MNOS/SOS technology by the development of nitride-oxide memory devices and high voltage p-enhancement and n-depletion mode devices used in complementary symmetry circuits. This CMOS compatible memory dissipates less than 300 mW with a read access time of less than 400 nsec at total dose levels near 500K rads (Si). The balanced memory detection and read enhancement features help assure long term data retention through total dose and transient radiation environments. Temperature-bias stability has been demonstrated.

## Introduction

Major problems encountered in the development of hardened MNOS memory arrays have been compatible processes for both memory devices and the fixed threshold devices required in the address and decode logic, high voltage input levels not compatible with low power off-chip drivers, and high internal power dissipation. The new technology described in this paper significantly reduces these problems and provides new added features.

Radiation effects in nitride-oxide gate insulators have been studied previously;<sup>1,2,3</sup> however, this work represents the first application to hardened CMOS/SOS LSI. A nitride-oxide gate insulator technology is described which is compatible for both the memory and fixed threshold SOS devices required. Further, n-depletion mode SOS devices are used in depletion mode complementary symmetry circuits (DM/CMNOS) to provide both CMOS compatible input/output signal levels as well as low power dissipation. The added features include a read enhancement effect that eliminates limitations on the number of memory read cycles; a two transistor memory cell and balanced detection circuit that helps assure long term data retention and operation through total dose and transient radiation environments; a rapid transient anneal characteristic; and circuits for analog measurement of memory thresholds for memory retention characterization. A random access  $256 \times 4$  MNOS/SOS memory using this nitride-oxide SOS technology has been developed, processed, and characterized.

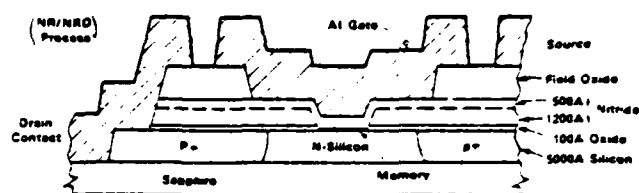
## Device Technology and Physics

A reliable form of MNOS memory device termed the drain-source protected (DSP) structure incorporates a fixed threshold MNOS structure in series with the variable threshold memory region.<sup>4</sup> A number of alternative approaches to a hardened version of the DSP memory were studied.<sup>5</sup> The approach chosen and shown in Figure 1 minimizes the interaction between process steps and permits the processing parameters for the fixed threshold MNOS region to be controlled independently from the MNOS memory region and vice versa. The fixed threshold region is formed first and overlaps the source and drain. The memory gate window is then etched through the first 1300Å nitride layer and 100Å oxide. Then the memory oxide is formed and the 300Å memory nitride is deposited. This nitride removal and subsequent second nitride deposition sequence is termed the NR/NRD process.

The fixed threshold p-channel devices used in the decoding circuits have the same 1800Å nitride/100Å oxide gate insulator as in the fixed threshold region of the above memory device. The fixed threshold ion implanted N-depletion mode high voltage device shown in Figure 1 uses the same fixed threshold gate insulator. The  $p$ -boron implant (180 keV) is used to control the back channel leakage at the silicon-sapphire interface. The boron implant extends over a part of channel length to prevent low drain breakdown

\*This work was supported by the Space and Missile Systems Organization under contract F04704-75-C-0006.

Drain Source Protected MNOS/SOS Memory X-Section



Implanted N-Depletion Mode SOS IGFET

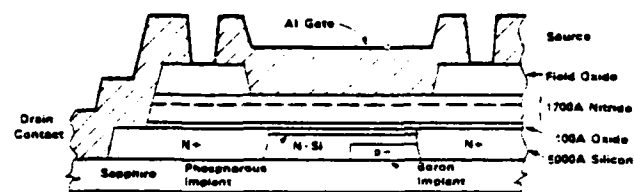


Figure 1. Device Cross Sections

voltage. The shallow phosphorous implant is used to set the drain-source current at zero-bias ( $I_{DS0}$ ). Additional details on device fabrication are given in a paper describing CMNOS/SOS devices.<sup>6</sup>

The effect of ionizing radiation on fixed threshold nitride-oxide gate insulators has been studied previously by A.G. Stanley,<sup>1</sup> C.W. Perkins et. al.,<sup>2</sup> and by Newman and Wegener.<sup>3</sup> It has been found that the hardness of the gate insulator is improved as the oxide thickness is reduced. However, if the oxide thickness is reduced below 50Å, then the stability is adversely affected. A 100Å oxide provides a controllable and stable structure provided the nitride thickness is adjusted to accommodate the maximum operating voltage.

We have found in our own studies that the radiation induced threshold shift increases with the square of the oxide thickness given a fixed nitride thickness. This is consistent with a trapped charge distributed uniformly throughout the volume of the oxide. However, the radiation induced threshold shift does not appear to increase with the square of the nitride thickness given a fixed oxide thickness (100Å). Consider the simplified charge density versus insulator thickness diagram shown in Figure 2. The charge trapped in the nitride is given in terms of a uniform space charge distributed a distance  $d$  into the nitride from the nitride oxide insulator. The threshold shift caused by the charge trapped in the nitride may be expressed in terms of the center of charge (charge centroid  $\bar{X}_n = X_n - d/2$ ) by

$$\Delta V_T = - \frac{X_{ne}}{\epsilon_n} (\rho_1 \cdot d) \cdot \frac{\bar{X}_n}{X_n} \quad (1)$$

where  $X_{ne} = X_n + \frac{\epsilon_n}{\epsilon_{ox}} \cdot X_{ox}$  (effective nitride thickness) and

$\epsilon_n$  = nitride permittivity,

$\epsilon_{ox}$  = oxide permittivity

For the special case of charge distributed throughout the nitride ( $d = X_n$ ) and  $X_{ox} < X_n$ , the threshold shift is given by

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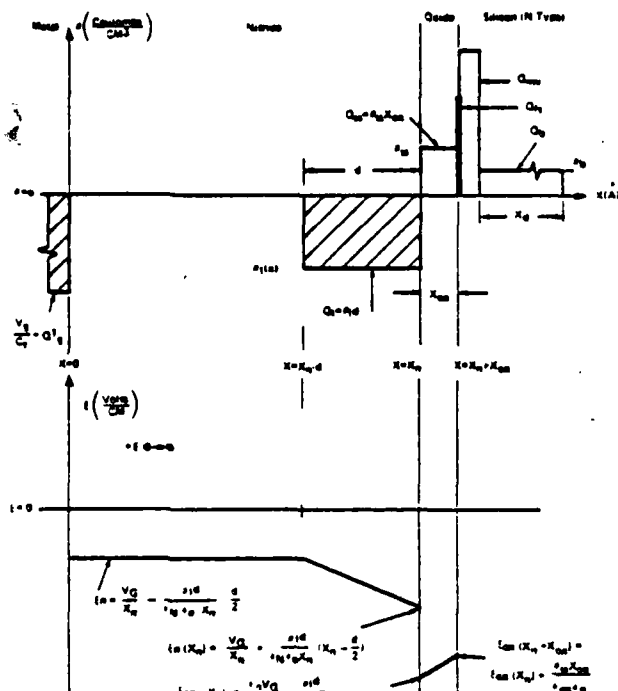


Figure 2. Charge Density ( $C/cm^3$ ) vs Insulator Thickness

$$\Delta V_T = - \frac{\rho_{it} X_{ne} X_n}{2 \epsilon_n} \approx - \frac{\rho_{it} X_n^2}{2 \epsilon_n} \quad (2)$$

Another special case of interest is for  $d$  much less than  $X_n$ . Then in terms of a thin sheet of charge  $Q_I = \rho_{it} d$ , the threshold shift is

$$\Delta V_T = - Q_I \cdot \frac{X_{ne}}{\epsilon_n} \quad (3)$$

The charge in the oxide and fast surface states will produce a threshold shift

$$\Delta V_T = - (Q_{ss} + Q_{fs}) \cdot \frac{X_{ne}}{\epsilon_n} \quad (4)$$

The shift produced by interface states may be separated from that caused by space charge by C-V measurements; however, it is very difficult to separate the effect of a space charge in the nitride near the nitride-oxide interface ( $Q_I$ ) from the charge in the oxide ( $Q_{ss}$ ).

The threshold shift caused by ionizing radiation has been measured for the fixed threshold devices described in Figure 1. Further, the nitride thickness has been varied from about 1000Å to 1300Å, while the oxide thickness has been kept constant at 100Å  $\pm$  10%. The p-channel threshold shift versus effective nitride thickness ( $V_T$  vs  $X_{ne}$ ) is shown in Figure 3. The gate bias for these measurements was -12V. It can be seen that a linear relationship between  $\Delta V_{TP}$  and  $X_{ne}$  exists over this thickness range. The space charge density ( $Q_I + Q_{ss}$ ) that exists near the silicon interface is found from the slope of the  $\Delta V_{TP}$  versus  $X_{ne}$  relationship. From C-V measurements, it was found that the interface state density was small compared to the space charge density. At a total dose of 100K rads (Si) the average positive charge density ( $N_I$ ) trapped in the oxide and nitride is  $2.3 \times 10^{11} cm^{-2}$ , and at 300K rads (Si)  $N_I$  is  $5.7 \times 10^{11} cm^{-2}$ .

Since voltages as great as 30V are sometimes required in MNOS memory devices, the radiation induced threshold shift dependence on gate bias has been studied.  $\Delta V_{TP}$  versus  $V_{GS}$  data taken from more than 10 different MNOS/SOS memory lots is shown in Figure 4. The nitride thickness was 500Å  $\pm$  200Å and the oxide thickness was 100  $\pm$  10Å for all of the samples used for this figure. The spread in  $\Delta V_{TP}$  is caused partly by nitride thickness variations and partly by nitride charge transport variations.

\*The  $CO_2$  source used is located at the Armed Forces Radiological Research Institute in Bethesda, Maryland. Dosimetry was provided by the same laboratory and cross-correlated at Northrop by using TLD's spaced laterally across the test fixture.

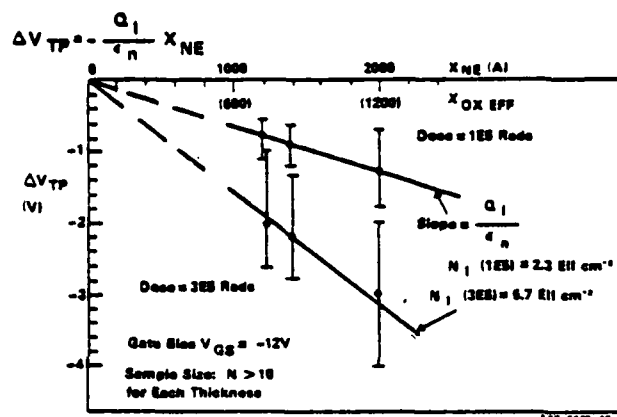


Figure 3. Threshold Shift vs Effective Nitride Thickness

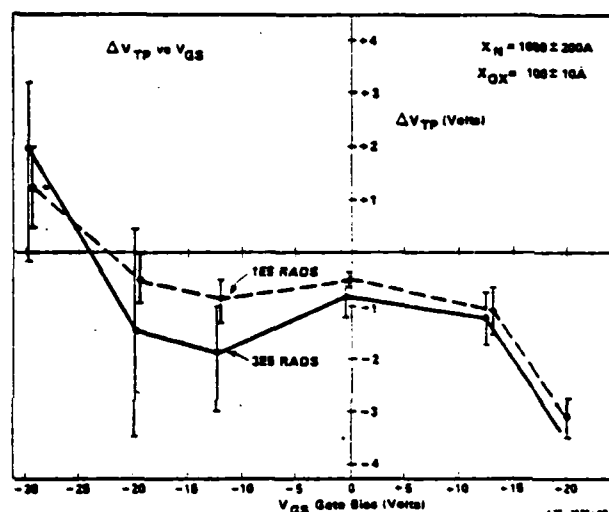


Figure 4. Radiation Induced Threshold Shift vs Applied Gate Bias

There is a significant difference between p-channel threshold shifts for the nitride-oxide gate insulator compared to oxide gate insulators. The latter usually exhibits a gradually increasing negative  $\Delta V_{TP}$  for increasing negative gate bias. Also, there is usually a very large negative  $\Delta V_{TP}$ , even for small positive gate bias. However, the nitride-oxide gate insulator shows a positive threshold shift for large negative bias and a large negative shift for large positive bias.

It appears that for negative bias levels on the nitride-oxide insulator at least two compensating mechanisms are taking place. One is positive space charge build-up in the oxide ( $Q_{ss} + Q_{fs}$ ) and the second is negative charge trapping in the silicon nitride. The negative charge dominates (i.e.,  $-Q_I > |Q_{ss}|$ ) at large negative gate bias levels and produces the positive  $\Delta V_{TP}$ .

The large negative  $\Delta V_{TP}$  for large positive gate bias can be explained by the  $-Q_{ss}$  in the oxide and the added effect of  $+Q_I$  trapped in the nitride.

The differences between radiation effects in oxide and nitride gate insulators may be better understood when consideration is given to conduction differences in the two insulators. Silicon dioxide has much lower electronic conduction compared to silicon nitride. Also, hole transport in silicon dioxide is minimal because of low hole mobility and deep hole traps. On the other hand, charge transport in silicon nitride is controlled by both hole and electron transport and hole and electron traps in the bulk of the insulator. The hole and electron traps are believed to be distributed over a range of shallow to deep energy levels. These trapped charges can cause strong internal fields to develop that affect both the bulk silicon nitride conduction and charge carrier injection at the contacts and at the nitride-oxide barrier.<sup>3,9,10</sup>

The radiation induced positive and negative  $\Delta V_{TP}$ , shown in Figure 4, may be explained by the hole and electron conduction and trapping proper-

ties of silicon nitride with the aid of an energy band diagram. An energy band diagram showing the relative heights of the conduction and valence bands for the metal gate, silicon nitride, silicon dioxide, and silicon are shown in Figure 5. For the case of a negative gate bias shown in the upper part of the figure, the bands are tilted to the right. It can be seen that there is a tendency to shift the centroid of *negative* trapped charge towards the nitride-oxide interface. This is consistent with the positive  $\Delta V_{TP}$  observed for large negative bias. For the case of positive gate bias shown in the lower figure, there is a tendency to shift the centroid of *positive* trapped charge towards the nitride-oxide interface. This is consistent with the negative  $\Delta V_{TP}$  observed for large positive bias.

It should be noted that the radiation data shown are not indicative of a fundamental limitation of the performance of nitride-oxide gate insulators. Rather, these are only the characteristics of a given set of nitride deposition and oxide growth conditions on SOS that illustrate the physical mechanisms involved. The  $\Delta V_{TP}$  versus  $V_{GS}$  is dependent on the hole and electron conduction properties of the nitride and is thus dependent on the nitride deposition conditions.

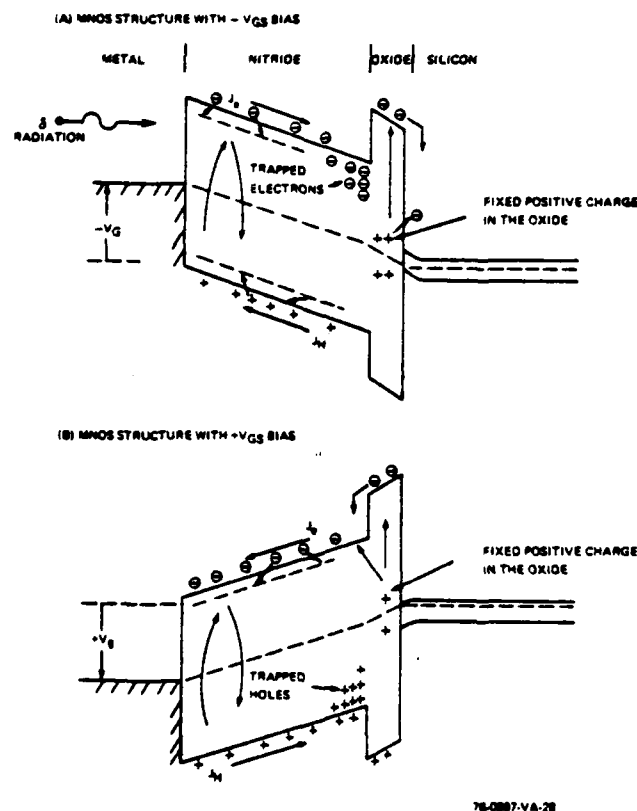


Figure 5. Energy Band Diagram Showing the Effects of Ionizing Radiation on MNOS Structures

#### 256 x 4 MNOS Memory Design

A random access 256 x 4 MNOS/SOS electrically reprogrammable non-volatile memory has been designed, processed, and characterized. The memory uses the DSP MNOS memory, ion implanted N-depletion mode, and p-channel enhancement mode devices described in Figure 1. A block diagram of the memory is shown in Figure 6. Included on the LSI device are low power Depletion Mode/CMNOS buffers to generate internal control, timing, address, and input/output signals. All input and output signals are CMOS compatible. A low power p-channel tree decoder is used to select any one of 64 rows of memory array and another decoder selects any two of 32 columns of the memory array. This provides random access in the clear, write and read modes of any two memory transistors which comprise one memory cell. This two MNOS FET balanced cell is designed to provide reliable detection with variations in supplies and with operation in a radiation environment. Each output bit has an associated column detection circuit and I/O buffer. Although organized as a random access 256 x 4 memory, the SOS isolation and circuit design permit a random access 1024 x 1 organization.

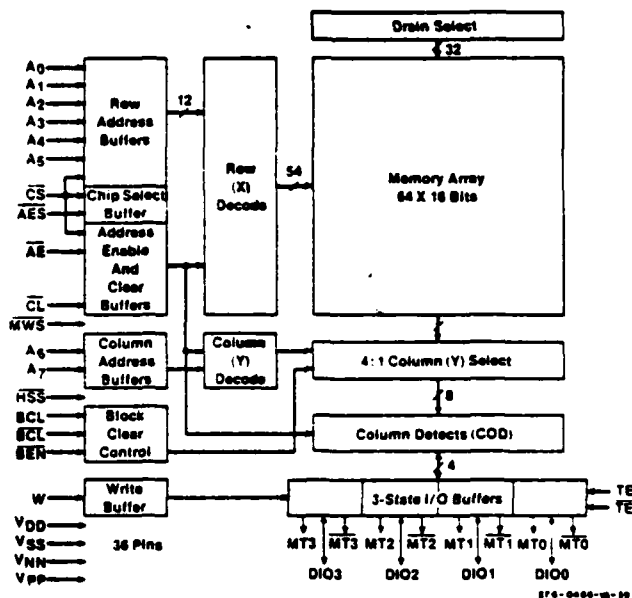


Figure 6. Permanent Store Memory Block Diagram

A photograph of the 256 x 4 MNOS/SOS memory is shown in Figure 7. The chip is 237 x 260 mils in size for conservative mask design rules were used. The chip size is also affected by the 12 extra memory array and test transistor test points brought out to package pins. All inputs are protected with high performance input protection networks that are rated at greater than 20 microjoules (1  $\mu$ sec). Three supplies are required to power the chip;  $V_{DD} = +12$ ,  $V_{NN} = -9$ , and  $V_{pp} = -18$  volts.

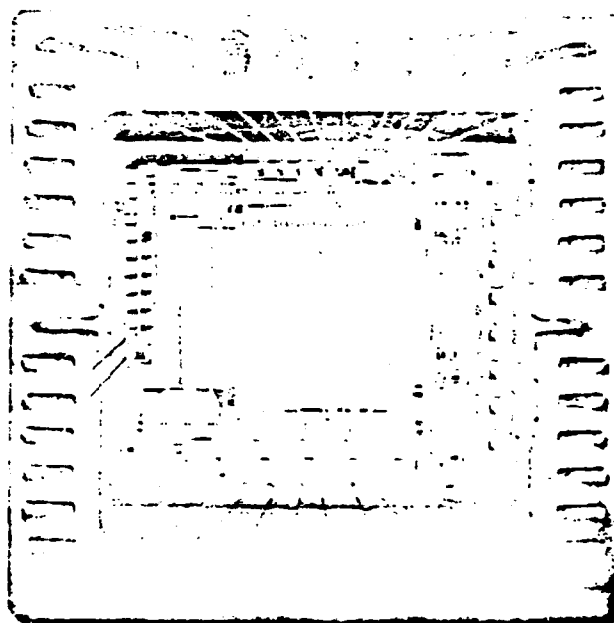


Figure 7. Microphotograph of MNOS/SOS Permanent Store Memory

Since MNOS memory requires write voltages with magnitudes of up to 30 volts, it is imperative that the peripheral logic be capable of withstanding these voltages, and in order to operate at high speeds with low power consumption, the logic must also be of the push-pull type. Present MNOS arrays utilize all P-channel circuitry. While this type circuitry is capable of withstanding 30-volt supplies, the high-speed and low-power dissipation is difficult to achieve. With standard CMOS, high speeds at low power is possible, but this type circuitry cannot meet the 30-volt breakdown requirement. In order to meet all of these requirements, a new logic type, Depletion Mode CMOS (DM/CMOS) was developed. This type circuitry uses a high breakdown, N-channel depletion mode device in conjunction with a P-channel driver fabricated on SOS to provide high-speed, low-power circuitry.

A schematic diagram for a peripheral timing buffer which utilizes DM/CMOS logic is shown in Figure 8. Both the N-channel depletion mode devices and the P-channel enhancement mode devices are operated in the negative gate-source bias regime to provide radiation hardness. In the normal "on state," the N-channel depletion mode devices will conduct  $I_{D50}$  (the drain current that flows in a depletion mode device for zero gate to source bias) while in the "off state," the N-channel devices are pinched off with  $-10$  volts which is well above the nominal pinchoff of  $-3$  volts. In normal operation, devices N2, N3, and N5 are always on, conducting  $I_{D50}$ . These devices are very small load devices compared to the other devices in the circuit and provide a dc holding current which compensates for leakage currents and any photocurrents that may be produced in a transient radiation environment.

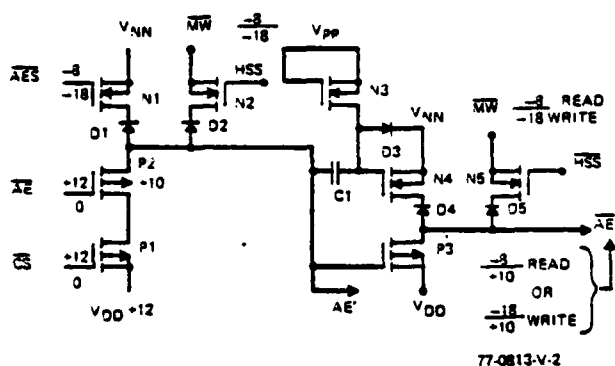


Figure 8. DM/CMOS Buffer

The buffer circuit is based on the operation of two distinct inverter types. The first, composed of P1, P2, N1, and N2 is a precharge type with dc holding element N2. N1 is used to precharge the output node while P1 and P2 are off. N1 then turns off, and the inverter output will switch when the inputs to P1 and P2 turns these devices on. The second type, composed of P3, N4, and N5 utilizes a level shifter composed of C1, D3, and N3 which level shifts the output of the first inverter stage so that push-pull operation of this stage is attained. Voltage (20V) transition times of 20 to 30 nsec have been achieved with very low dc power dissipation using this circuit configuration.

The column detection circuit shown in Figure 9 is comprised of a balanced cross coupled bistable circuit which detects the state of the memory cell. The detection sensitivity has been found to be less than 100 mV. A significant test feature has been added to the detection circuit. The devices TT1 and TT2 are used to measure the threshold voltage of every memory transistor in the memory array. This permits analog measurement of the memory window as a function of time and thus, accurate measurement and prediction of memory retention is made possible.

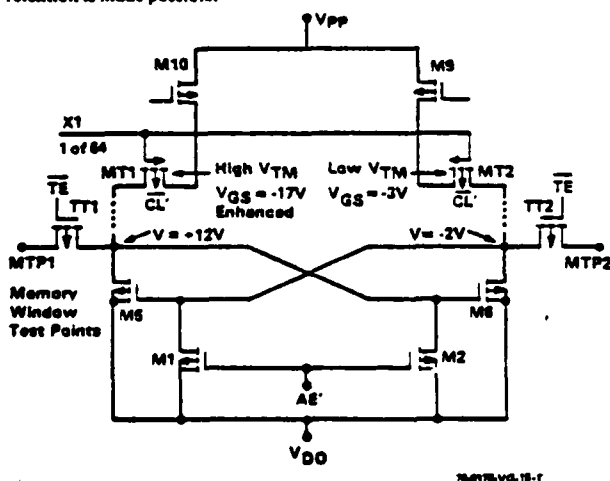


Figure 9. Detection Latch Provides Read Enhancement. Also Analog Memory Test Feature

Another significant design feature of the memory is the enhancement of the stored data during the read cycle. The simplified detection circuit shown in Figure 9 will be used to describe the read enhancement feature. First, the

memory transistors are read out in the common drain or source follower mode of operation. The detection circuit pulls the source of the low conductance (high  $V_{TM}$ ) memory transistor (M1) to  $V_{DD}$ , while the high conductance (low  $V_{TM}$ ) memory transistor (M2) just charges line capacitance. Since the memory gate read voltage is about  $-5$  V and the M1 source is at  $+12$ , a small write voltage ( $-17$  V) is applied to M1. This tends to rewrite the high threshold state of the device and thus enhances the data stored. On the other hand the source voltage of M2 is just one threshold drop higher than the gate voltage. Thus, a minimal read disturb voltage of  $-3$  V is applied. Thus, each time a memory cell is read out, the data stored is enhanced. There is no limitation on the number of read cycles because of the read enhancement feature.

The noninverting I/O buffer consists of several DM/CMOS stages to buffer input signals to the proper level. Also, the I/O buffer provides a 12V output drive of a 15 pF external load capacitance in 20 nsec or 30 pF in 40 nsec.

#### 256 x 4 Random Access MNOS/SOS Memory Characteristics

The pre-rad electrical characteristics and design features of the 256 x 4 MNOS/SOS memory are summarized in Table 1. The memory tests were performed over the temperature range of  $-55^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$  on a Macrodata 134 computer controlled test system. It has been found that supplies may be varied more than 10% without degradation of pre-rad performance.

TABLE 1  
PERMANENT STORE MEMORY: CHARACTERISTICS AND FEATURES

• 256 X 4 Organization	• CMOS Compatible Inputs and Outputs
• Random Access	• MNOS/SOS Technology
Clear/Write Cycle 200 $\mu\text{s}$	• Two PMNOS FETs Per Bit
Read Cycle 500 ns	• Differential Detection
Read Access 250 ns	• Read Enhancement
• Retention 3 Years	• PENT and NDMT Circuitry
After $10^4$ Reversals	• Test Mode for Analog Measurement of All Memory $V_T$
• Endurance $10^8$ Cycles	• Single Block Clear Option
with 3 Months Retention	• Three Power Supplies and Ground
• Power (mW)	+12V, -5V, -18V.
Read 300	
Write 97	
Standby < 1	

The pulse response and retention of the memory transistor within the LSI array for a single 100-  $\mu\text{sec}$ -clear and a 100-  $\mu\text{sec}$ -write pulse are shown in Figure 10. The memory threshold difference (window) is shown as a function of time for different numbers of clear-write reversals of the data. The memory window for a sample of memory parts from different lots has been measured out to 6 months. By extrapolating over a fraction of one decade, retention is predicted to be much more than 3 years ( $10^8$  seconds) after  $10^4$  clear-write reversals, near 3 years after  $10^6$  reversals, and 3 months to 1 year after  $10^8$  reversals.

The memory may also be written with shorter or longer pulsewidths with a tradeoff in retention time. For example if written with a 10-  $\mu\text{sec}$  pulse the retention period will be reduced by about 2 decades from the 100-  $\mu\text{sec}$  data.

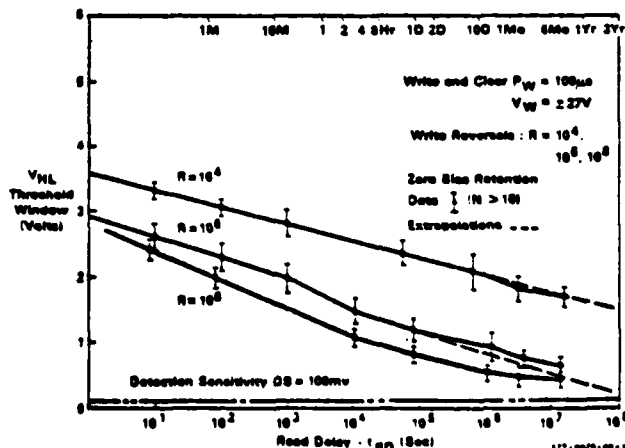


Figure 10. PSM: Pulse Response and Retention

The read enhancement effect is shown in Figure 11. The memory transistor threshold difference  $\Delta V_{th}$  is plotted as a function of the number of read cycles. It can be seen that only a small enhancement of the window occurs up to  $10^3$  read cycles but a significant increase in the memory window occurs when the devices were read continuously out to  $10^6$  read cycles. Because of the read enhancement feature there is no limitation on the number of read cycles.

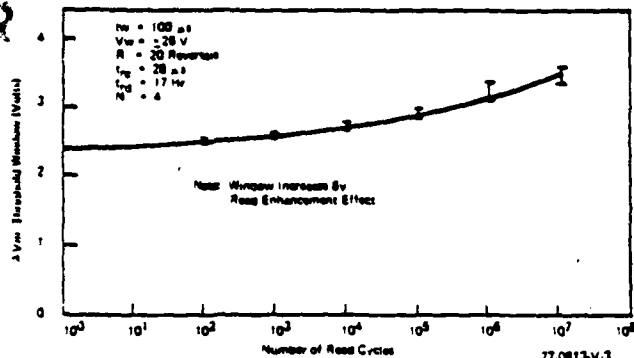


Figure 11. PSM Read Enhancement

Ionizing radiation tends to decrease the MNOS memory window and thus memory retention as the total dose increases.<sup>5,11</sup> The effect is dependent on the gate bias applied during the radiation. The memory window is significantly affected at  $CO^{60}$  total dose levels approaching  $10^6$  rads (Si). These effects are compensated to some degree by the read enhancement feature of this memory array.

Total gamma dose tests using the  $CO^{60}$  source at AFRRRI were performed on fully functional MNOS memory arrays in both the static deselect mode and in the dynamic read mode. Measurements were made 1 hour after exposure. It was found that the read access time increased from 250 nsec to 400 nsec at total dose levels approaching  $5 \times 10^5$  rads (Si). The measurements were with minimum supply conditions and with an output load capacitance of 40 pF. This data reflects the characteristics of the nitride-oxide processes used for the transistors described in the first part of this paper and is not a fundamental limitation of MNOS memory arrays using a nitride-oxide gate insulator. With an increase in the read mode operating voltages, best part performance is extended to beyond  $10^6$  rads (Si).

The deselect power dissipation in the  $256 \times 4$  memory array is less than 1 mW before radiation. After radiation the deselect power dissipation is increased to 0.5 to 4 mW. The increase in standby power reflects the increase in the N-depletion mode back channel leakage currents. These are typically 0.1 to 2  $\mu$ A per mil of n-channel transistor width at total dose levels of  $10^5$  to beyond  $10^6$  rads (Si). The n-channel drain voltage was  $\pm 20$  volts and the off-state gate voltage was  $\pm 10$  volts for these measurements.

Transient radiation tests have been performed with both FXR short pulse (30 nsec) conditions and LINAC wide pulse ( $>1$   $\mu$ sec) conditions. The transient radiation tests were synchronized with the dynamic read operation of the  $256 \times 4$  MNOS memory arrays to probe the sensitive period during memory state detection. No data upset or data loss occurred for the maximum output of the FXR facilities ( $10^{10}$  rad/sec). This verifies the computer simulation of the balanced two transistor memory cell and detection circuit. The wide pulse LINAC tests produced no memory data loss but logic upset was detected at a significant factor below the narrow pulse tests.

Transient annealing effects of the nitride-oxide gate insulator are orders of magnitude shorter than for oxide gate insulators. This is related to the greater hole and electron conductivity in silicon nitride as compared to silicon dioxide. Transient annealing for high total dose levels has occurred in the LSI parts in less than 500 nsec. Of course, the low lifetime and small junction areas of SOS technology contribute to the rapid recovery. This means that although logic upset may occur in a memory array at a high dose rate level, that within one read cycle time the memory array becomes fully functional.

As a part of the memory array test program, temperature-bias stress tests of fully functional MNOS/SOS memory arrays have been carried out. Special test points have been bonded out for the fixed threshold p-enhancement and n-depletion test transistors as well as for the analog measurement of the memory transistor thresholds in the memory array. After 1,000 hrs of S at  $125^\circ\text{C}$ , there was negligible change in the p-channel threshold  $V_{tp}$ , the n-channel  $I_{DSO}$ , and drain leakage current  $I_{DSL}$ . Also the memory array access time change was less than 5%.

Additional accelerated TBS tests have been carried out over the temperature range of  $125$  to  $200^\circ\text{C}$  to determine activation energies associated with thermally activated threshold voltage shifts.<sup>7</sup> Larger samples of data are needed to generate long term reliability factors; however, the data indicates high reliability requirements can be met.

## Conclusions

Major problems encountered in previous MNOS memory array development have been significantly reduced by the approach presented above. A random access  $256 \times 4$  MNOS/SOS nonvolatile memory has been designed, processed, and characterized. Significant advances have been made in radiation-hard low-power high-voltage MNOS/SOS technology by the development of the nitride/oxide NR/NRD process used on the DSP MNOS memory devices and the depletion mode n-channel devices used in the DM/MNOS circuits. This LSI memory provides high-speed, low-power operation at total dose levels exceeding 500K rads. The balanced memory detection and read enhancement features help assure long term data reduction through total dose and transient radiation environments. Long term temperature bias stability has been demonstrated.

## Acknowledgements

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## References

1. A.G. Stanley, "Comparison of MOS and Metal-Nitride-Semiconductor IGFETS Under Electron Irradiation," *IEEE Transactions on Nuclear Science*, NS-13, No. 6, pp. 248-254, Dec. 1966.
2. C.W. Perkins, K.G. Aubuchon and H.G. Dill, "Radiation Effects and Electrical Stability of Metal-Nitride-Oxide-Silicon Structures," *Applied Physics Letters*, Vol. 12, 385-387, 1 June 1968.
3. P.A. Newman, H.A.R. Wegener, "Effects of Electron Radiation on Silicon Nitride Insulated Gate Field Effect Transistors," *Trans. on Nuclear Science*, pp. 293, Vol. NS-14, No. 6, Dec. 1967.
4. J.R. Cricchi, F.C. Blaha, M.D. Fitzpatrick, "The Drain-Source Protected MNOS Memory Device and Memory Endurance," *IEEE Int. Electron Devices Digest*, pp. 157-162, Dec. 1973.
5. J.R. Cricchi, F.C. Blaha, M.D. Fitzpatrick, F.M. Sciuilli, "Semiconductor Memory Research," Tech. Rpt. AFAL-TR-75-233, pp. 109-127, Dec. 1975.
6. R.S. Ronen, et. al., "High Voltage SOS/MOS Devices and Circuit Elements: Design, Fabrication and Performance," *JSSC*, 11, 431-42, August 1976.
7. J.R. Cricchi, D.A. Barth, H.G. Oehler, R.C. Lyman, J.M. Shipley, "A High Speed, Radiation Hardened CMOS/SOS Mask Programmable ROM and General Processor Unit," 1977 IEEE Annual Conference on Nuclear and Space Radiation Effects Poster Section - 20, 14 July 1977. (See this issue)
8. P.C. Arnett and D.J. Di Maria, "Contact Currents in Silicon Nitride," *J. Appl. Phys.*, Vol. 47, 2092-97, May 1976.
9. D.J. Di Maria and P.C. Arnett, "Conduction Studies in Silicon Nitride: Dark Currents and Photocurrents," *IBM, J. Res. Develop.*, pp. 227-244, May 1977.
10. C.M. Svensson, "The Conduction Mechanism in Silicon Nitride Films," *J. Appl. Phys.* Vol. 48, No. 1, pp. 329-335, Jan. 1977.
11. H.A.R. Wegener, M.B. Doig, P. Marrifino and B. Robinson, "Radiation Resistant MNOS Memories," *IEEE Trans. on Nuclear Science*, NS-19, p. 291, Dec. 1972.

## CMOS/SOS LSI INPUT/OUTPUT PROTECTION NETWORKS

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### ABSTRACT

An improved input and output electrical surge protection has been developed for CMOS and MNOS large scale integrated circuitry fabricated on sapphire. The failure mode was designed to be the input or output series limiting diffused resistor, which can be controlled reliably through the fabrication processes. Forward bias diodes attenuate the overvoltage surges. Failure energies and voltages have been evaluated, and design equations are developed and verified.

### SUMMARY

This paper reviews the integrated circuit networks developed to protect the input MOS gate insulators and output MOS drain-body junctions of CMOS devices fabricated as LSI circuits with silicon on sapphire technology. The major concern and experimental verification was with low impedance high voltage transients having pulse widths between 40ns and 1μs. High voltage exponential zap tests also were done. Reliable and repeatable results were obtained with many parts of four different LSI types designed and fabricated by the Advanced Technology Laboratories, Westinghouse Electric Corporation. The pulse testing equipment, EMP tests, and data evaluation were developed and performed by the Electronics Division, Northrop Corporation.

This work was performed under Contract F04704-75-C-0006 to the Space and Missile Systems Organization, Norton Air Force Base, Captain Robert Warzynski, Project Officer.

The design utilizes one weakest element which is the input or output series current limiting resistor, which can be replicated reliably. The narrow high power density regions of this resistor must be formed with uniform resistivity in the epitaxial silicon film, using a straight cornerless geometry in the epitaxial silicon, using greater than minimum width. Cross-overs can be made over the lower potential end of the input resistor if the width is widened 60% to lower the localized heating. Resistor ends should be flared 20% with large contact windows greater than 0.6 square. Failure voltage or energy is proportional to the resistor length, measured in squares. Other variables are less important with failure dependent on the square root of sheet resistivity and inverse fourth root of the pulse width. The failure voltage is not much influenced by the uniform resistor width, which is chosen as a trade between die area and electrical performance.

The transferred voltage is clamped to the nearest supply voltage with semiconductor junctions sized not to fail first, since they are more variable. They are operated in the forward bias mode, permitting maximum power and repeatable production characteristics. A single resistor small diode clamp will not attenuate fast voltage input spikes adequately. A cascaded double L attenuator topology is used for the input assuring transient protection of the thin gate dielectric. A single L attenuator protects the output MOSFETS. Multiple low bulk resistance diodes are paralleled across the power buses, reverse bias connected and processed to break down at a few volts greater than the maximum operating voltage. The sizing of the single level aluminum conductors is chosen to withstand the transient surge currents, and failure levels were determined on metallization test patterns crossing over etch patterns on sapphire.

#### INTRODUCTION

During the course of developing complex CMOS/SOS logic and MNOS/SOS memory circuits in a study on advanced computer technologies, a reliable input protection network was needed which would withstand usual static discharges that occur during electronic module construction and maintenance. It was desired that these new MOSFET parts could be handled at the die and packaged part level with

no more precautions than those commonly used with bipolar parts. Further, these parts were hardened to tolerate nuclear radiation effects, and superior protection must be provided against internally generated EMP transient voltages that might develop with low source impedances. The major emphasis of verification tests was done with all operating potentials on the parts, 12V for CMOS and up to 30V for MNOS parts. The transition between adiabatic and quasi-adiabatic region occurs near 90ns, so most of the measurements were made between 100ns and 1us. Transient RC zap tests and human equivalents also have time constants in this time domain (Ref. 1 and 2). Since transients run both ways on interconnecting wiring, tests included both inputs and outputs. Input tests were also run with all supply pins floating except the ground or Vss connection and the input under test. The floating supply condition was not worst case.

Tests were done on hundreds of inputs and several dozen outputs on four LSI devices; a mask programmed read only memory (ROM), an electrically alterable read only permanent store memory (PSM 6013), a fast random access memory used for scratch pad temporary store (TSM), and an improved PSM (6023). These devices are large die, 25 to 40mm<sup>2</sup> (40K to 60K mil<sup>2</sup>), so eighteen or more protective networks each about 0.05mm<sup>2</sup> use only about 0.9mm<sup>2</sup> or 3% of the chip area. The level of protection increases with allocation of more power dissipating area, and the networks chosen are adequate for these LSI parts. These large protective networks would be less attractive for small scale integrated circuitry since they would noticeably increase the die size and lower the wafer die yield. Input protection has been demonstrated with arc gaps (Ref. 3 and 4) using short 20 to 40ns pulse widths. Ground rings and large 50um arc gaps, unpassivated for low dynamic arc impedance, were not considered attractive for high reliability LSI that would be subjected to many repeated EMP surges. The chosen approach keeps high voltage surges at the perimeter of the die, permits inspection with conventional input resistive and leakage current measurements, withstands repeated over voltage surges without degradation if kept 20% under the failure threshold, and has been demonstrated successfully for about two years on over a hundred LSI parts which have received extensive handling and repetitive measurements in temperature-bias reliability aging and nuclear hardness tests.

PULSE TEST NETWORK

A test jig was constructed to interface the LSI component with a charged transmission line pulser. The design matched the RG-58 50 Ohms coaxial cable which determined the pulse width at about 3.0ns/ft. A Simulation Physics Pulser, Model 25, was used to form the single input pulse. A 20 Ohms current limiting resistor was added between the LSI terminal and the output of the pulser. This avoided damaging the pulse forming network by reducing somewhat the surge currents that developed when the input resistor ionized into a low conductive path. A low impedance non-inductive divider sampled 0.100 of the LSI input voltage, thus protecting the Tektronix Model 7844 oscilloscope wide bandwidth preamplifiers. The LSI input current was simultaneously measured with a CT-2 current probe. The network was constructed over a ground plane, and less than 2.5 inch lead dress was used to contact one LSI input or output. Voltage transitions were achieved within 10ns. LSI power was supplied through limiting resistors, but capacitively stiffened at the zero insertion socket terminals.

Typical waveforms are shown for a +580V, 100ns wide input pulse. In Figure 1 note resistor heating first reduces the current until the high temperature heating causes the current to hook up at the end of the pulse.

Ten repeated low duty cycle pulses will not change these waveshapes, but just one pulse with 10% more input voltage will destroy the input resistor since the low source resistance of 21 Ohms does not limit thermal run-away.

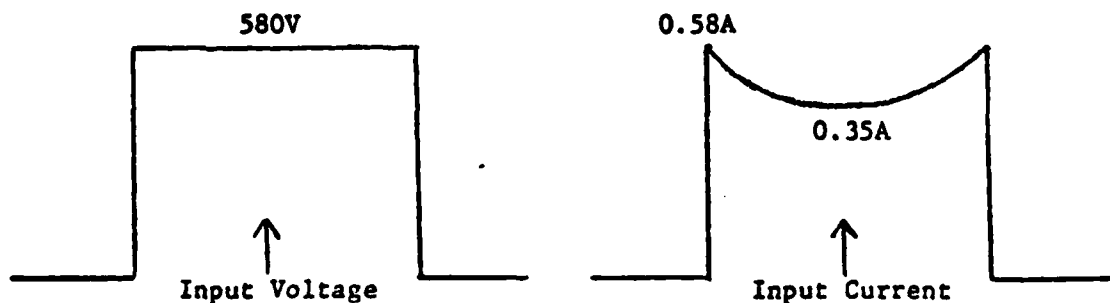


FIGURE 1, INPUT WAVEFORMS

### INPUT PROTECTION CIRCUIT

The thin gate dielectric is usually the weakest region in MOSFET circuits. Depending on process/fabrication/layout details, this region may destructively breakdown at the gate edges with potentials as low as 40 to 60 Volts in nominal 800Å to 1200Å thick silicon dioxide gate insulators (Ref. 2). The Westinghouse designs use diffusion aligned edgeless gate layouts with a thin 80Å silicon dioxide layer, then a 1300Å silicon nitride layer, forming an equivalent gate of 900Å  $\text{SiO}_2$ . CV measurements have shown the onset of nitride conductivity at 75V, with destructive breakdown or threshold shifts requiring even higher gradients. Destructive breakdown typically occurs between 100 and 120 Volts.

The input circuit design prohibits such large potentials from reaching the MOSFET, and shifts the failure mechanism to the input series resistor. This element can readily be inspected both with a pre-lid visual and packaged electrical screen, and is fabricated with easily controlled and verifiable processes, giving improved quality assurance. The input is built with a double L attenuator topology, shown in Figure 2. The power density in the p+ diffused resistor,  $R_1$ , sets the failure threshold.  $R_2$  and  $R_3$  are n+ diffused with half the sheet resistivity of the input, and do not degrade. The clamp diodes are small geometry, about  $140\mu$  junction periphery, are ion implanted for breakdown near 18V with a dynamic bulk resistance of 180 Ohms. They are sized not to be the weakest element, the input resistor is the circuit fuse.

The double attenuator provides a delay to the gate while the first L section clamp diode turns on. The performance is almost symmetrical with input polarities. The metal runs are sized to carry the surges and shunt photocurrents from intense ionizing radiation. The first node reduces a 580V 100ns pulse to typically 70V (worst case 100V) past the supply voltage. The smaller second attenuator then reduces the gate to body stress to 32V (48V worst case). Worst case assumes a diode resistance of 225 Ohms. Initially 600ma of surge current flows, but this drops about 40% as  $R_1$  heats. Thus, if the input surge comes from a higher impedance, as 1500 Ohms in a handling static discharge, (Ref. 1), the forcing voltage is dropped externally another 900V, or a pulse of 1500V for 100ns is required to cause serious damage.

### INPUT PROTECTION LAYOUT

The layout of the input protect network is shown in Figure 3. An earlier input protection layout is shown in Figure 4. The original layout exemplifies several conditions which should be avoided. The small contact at the top of the resistor caused localized heating which induced failure before the rest of the resistor degraded. A conductor path crossed the input resistor at 90% of the input potential, and the heated silicon underneath developed a premature arc through to this 2nd signal line. The improved design widened the resistor to  $25\mu\text{m}$  in the cross-over region, and crossed at the 50% voltage point. No failures have occurred in this wider cross-over region. The input resistor,  $R_1$ , was lengthened and the contact region was widened with a large 0.6 square contact window. A wider short aluminum path connects to the input pad. These changes improved the voltage failure level 1.9 times.

The original input layout, used on the ROM, needed  $0.041\text{mm}^2$ , the improved layout uses  $0.054\text{mm}^2$ .

Resistor  $R_1$  is sized at  $15\mu\text{m}$  wide so variations in edge etching will not contribute more than 10% to the resistance value or local power density. The resistivity variations of 17% contribute most to the tolerance spread, mostly between lots. The resistor length is  $320\mu\text{m}$  which gives protection up to 320V for pulses  $1\mu\text{s}$  wide, or 580V for pulses 100ns wide. The p+ sheet resistivity is about 40 Ohms/square.  $R_1$  is  $850\text{ Ohms} \pm 20\%$ ,  $R_2$  is about 300 Ohms, and  $R_3$  is the sum of internal cross-unders to the remote gate electrode, typically under 200 Ohms. The input protect network must be located adjacent to the connection pad on the die perimeter, and heavier power buses carry the surge current return.

Failure occurs when high temperatures develop an increasingly negative temperature coefficient (Ref. 5, 6) and the thermal ionization arcs along the center of the resistor, allowing the current to increase several fold. The arc extinguishes at the end of the pulse. Thereafter  $R_1$  is a fused open circuit. This surge may cause a secondary failure with a thin filament through

the junction of the forward biased clamp diode, (Ref. 7), and a larger destroyed region frequently occurs at corners in the reverse breakdown clamp diode. If the pulse is 10% below resistor failure, repeated low duty cycle single pulses do not degrade the resistance nor increase the input nanoamp leakage of the back biased diodes. If the resistor is not widened at the cross-over, the failure threshold will be somewhat lower, since the resistor will heat the silox near 500C where the aluminum reacts chemically to reduce the silox and develop a catastrophic arc-through.

A typical failure of the original input design after a +325V, 100ns wide pulse is shown in Figure 5 where the input resistor of ROM address 5 has burned open, the tiny heating filament degrading the forward biased diode cannot be seen, but two corner burnouts of the reverse biased diode are obvious. No visible degradation ever occurs in the second attenuator stage. For a square pulse, 1μs wide, the failure current density is about  $3 \times 10^6$  Amp/cm<sup>2</sup> and the energy density is about 1.3 joules/cm<sup>2</sup>, and the power density is  $1.3 \times 10^6$  Watts/cm<sup>2</sup>.

#### FAILURE CRITERIA

Significant degradation was used as the failure criteria. Since LSI devices have many functional characteristics, and degradation of narrow cross-unders in the test samples would cause multiple failures, a thorough parametric and logic test was made between each of the step stress levels. Most of the steps were recorded on high speed film using a dual trace so the true power could be integrated visually from the E and I waveforms. The Pacific Western Mustang LSI Tester, controlled by a minicomputer, made 200 to 300 parametric measurements on each LSI, between each voltage test group. These measurements were logged with a high speed printer in real time and scanned before the next stress step. Step increases near the failure level were about 10% in voltage, and ten repeated pulses were made in each test group. An optimum sequence of inputs was determined from the layout, augmented by trial and error, so that multiple input/output failure level data was obtained from the same LSI. Impending negative resistance thermally induced run-away frequently was avoided, and the same input could be retested at another pulse width.

All input and output high impedance 3-state leakage currents were measured with

10na resolution for logic 0 and 1 levels. Degradation criteria was obvious since leakages remained satisfactory and below 100na, or jumped over 100ua when degraded. Input resistances were measured, and changed only a couple percent before a catastrophic opening. Output current source or sink currents changed little until catastrophic failures. Internal logic changes were not found except as related to an input opening. Total power supply currents also did not change until large increases occurred from junction fusing or burn-out.

### INPUT FAILURE LEVELS

The failure voltage as a function of low duty cycle pulse width is shown in Figure 6 for the earlier ROM and 6013 PSM, and for the improved 6023 PSM. Many measurements on identical geometries gave consistent failure thresholds with about a 20% spread.

The resistor energy density for failure will be constant for very short pulses where negligible thermal conduction can occur. This adiabatic region occurs with pulses shorter than about 90ns. For longer pulses, a quasiadiabatic region occurs with failure energy increasing with the square root of pulse width, see break in Figure 7. At very long pulse widths, constant power equilibrium will occur with energy increasing with the first power of pulse width. The instantaneous integral of applied voltage and current was measured and the energy failure threshold for single pulses between 40ns to 1μs are shown for the two designs in Figure 7.

The voltage failure in the 100ns to 1μs (or longer) pulse interval can be predicted from linear heat flow theory using the Wunsch-Bell model (Ref. 8).

$$\text{Energy/area} = k t_w^{1/2} \quad (1)$$

The failure threshold current  $I_f$  for a pulse  $t_w$  wide in the narrow region of a resistor of length  $L_n$  and width  $W_n$  with sheet resistance  $\rho$  in Ohms/square yields the following relation:

$$\text{Energy/area} = \frac{I_f^2 R_n t_w}{L_n W_n} = \frac{I_f^2 \rho t_w}{W_n^2} \quad (2)$$

where  $R_n = \rho \frac{L_n}{W_n}$

If the resistor  $R_t$  is composite with one or more wider sections  $L_w$  long and  $W_w$  wide, the total failure threshold voltage  $E_t$  is determined by:

$$E_t = I_f R_t = I_f \rho \left( \frac{L_n}{W_n} + \frac{L_w}{W_w} + \dots \right) \quad (3)$$

Solving (1) and (2) for  $I_f$  and substituting in (3)

$$I_f = W_n k^{\frac{1}{2}} \rho^{-\frac{1}{2}} t_w^{-\frac{1}{2}}$$

$$E_t = k^{\frac{1}{2}} \rho^{\frac{1}{2}} t_w^{-\frac{1}{2}} W_n (\square_1 + \square_2 + \dots)$$

$$\text{or } E_t = k^{\frac{1}{2}} \rho^{\frac{1}{2}} t_w^{-\frac{1}{2}} (L_n + L_w \left( \frac{W_n}{W_w} \right) + \dots)$$

the constant  $k$  includes the specific heat, density, thermal conductivity and temperature rise to failure of the silicon resistor on the SOS structure.

Tests were done with and without the passivating silox on the parts, and the energy constant changed little (same result reported in Ref.2). Tests on 70 $\mu$ m wide output limiting resistors and 15 $\mu$ m wide input limiting resistors gave similar constants, with more experimental error in the output measurements, since the series diodes dropped about 42% of the total output voltage pulse, while the input diodes absorbed about 15% of the total input voltage surge.

The average energy density constant  $k$  at failure of 0.5 $\mu$ m diffused silicon resistors on a 330 $\mu$ m sapphire substrate is 1,260 joules  $\text{cm}^{-2}\text{sec}^{-\frac{1}{2}}$ . The experimental results are tabulated below for several pulse widths, resistor widths, B and P diffusion types and sheet resistivities.

Aver k value joules $\text{cm}^{-2}\text{sec}^{-\frac{1}{2}}$	Pulse width $\mu\text{s}$	Resistor width $\mu\text{m}$	Type $\Omega/\square\rho$
1,460	0.10	16	p+,40
1,311	1.0	16	p+,40
1,319	0.10	70	n+,34
1,118	1.0	70	n+,34
1,265	0.10	10	{ p+,95 and n+,24
1,172	1.0	10	
1,170	10	10	

The last three values are from Ref. 2, page 38.

Note that the failure voltage is only dependent on the resistor length, not the width which determines the electrical resistance and circuit delay time constant.

The resistivity determines resistor aspect ratio only. If the  $n^+$  were one fourth the sheet resistance of the  $p^+$  diffusion, two equivalent designs would use the same layout area, but the  $n^+$  resistor design would be half the width and twice the length of the  $p^+$  design for the same resistance and voltage failure threshold.

Simplifying the expression for 40 Ohm/ $\square$  resistors, with  $t_w$  in  $\mu s$  and  $L$  in  $\mu m$ , and correcting for the resistor thermal nonlinearity and the voltage dropped in the clamp diodes, the voltage failure threshold of improved input protect is approximately:

$$E_f = 1.0 (L_n + L_w (\frac{W_n}{W_w})) t_w^{-1/2} \text{ Volts}$$

#### CAPACITIVE DISCHARGE TESTS

A test circuit was made with a capacitor charged to a high potential, then switched to an input through 1500 Ohms. The 100pf with 1000 Volts, or 50 $\mu$ joules, voltage zap test (Ref. 1) was performed with no degradation on the improved input. The capacity was increased to 140pf with 1000 Volts peak applied to the 1500 Ohms source. Here the input resistor just started to degrade, rising about 1% in resistance with each zap. The failure level for capacitive discharges is broad, since large increases in the input resistor can occur before a failure in device access time results. Charging 140pf to 2000 Volts did not fail the input network or degrade gate or diode reverse leakage currents. The heated input resistor dropped in resistance far below power match to the 1500 Ohms source, and most of the increasing input voltage and energy is absorbed in the external source. Several 2000 Volts pulses increased the input resistor 25%. No arcs developed between the close 11 $\mu m$  spacing of the input pad and  $V_{DD}$  bus with a 0.8 $\mu m$  of silox passivation overcoat. Tests on non-silox circuits developed destructive arcs at 270 Volts or  $2.5 \times 10^7$  V/m.

POWER SUPPLY CLAMPING

Multiple parallel breakdown diodes clamp the supply lines from excessive transients when the power supply is not a low impedance. All tests described had nominal power on all supply lines with sufficient local energy storage to limit supply variations to less than 1 Volt during the transient pulse. Tests were also run to simulate static handling with all supply pins floating, except for the grounded  $V_{SS}$  connection. The excursions of the floating  $V_{DD}$  line were clamped well enough that no destructive breakdown occurred in the internal circuitry and the  $V_{DD}$  line rose to 25V through the 20 Ohms dynamic breakdown impedance when the input pulse was 580V at 100ns, the threshold of burn-out of the input limiting resistor.

METALLIZATION BURNOUT

The metallization widths are sized to carry the input surge currents and survive high ionization pulse currents without failure. The aluminum is a nominal  $1.0\mu\text{m}$  thick, with  $0.9\mu\text{m}$  as a minimum. The silox-silicon island step edges are graded to avoid step thinning. A special test structure has been designed with passivated  $1.0\mu\text{m}$  thick aluminum conductors in 5, 6 and  $8\mu\text{m}$  widths serpentine over 100 steps of  $0.8\mu\text{m}$  silox plus  $0.5\mu\text{m}$  silicon on a  $330\mu\text{m}$  thick sapphire substrate. Rectangular pulse tests were made with 100ns and  $1\mu\text{s}$  widths. The three line widths failed at about the same current density,  $J$ . Metallization burnout has been related to current density (Ref. 9 and 10) by

$$J = k t^{-1/2}$$

These test results gave results similar to those reported, although an exponent fit would have been  $-0.35$  rather than  $-0.50$  for 100ns and  $1\mu\text{s}$ .

$k$ $\times 10^4 \text{ A cm}^{-2} \text{ sec}^{1/2}$	$t_w$ $\mu\text{s}$	$J$ $\times 10^7 \text{ A cm}^{-2}$
1.71	0.1	5.4
2.40	1.0	2.4
2.00	0.51	2.8 (Ref. 10)
1.95	-	- (Ref. 9)
2.76	0.09	9.2 (Ref. 11)

Thus with  $k = 2 \times 10^4 \text{ A cm}^{-2} \text{ sec}^{1/2}$  an  $8\mu\text{m}$  minimum line width will handle up to  $1.4\text{A}$  or a current density of  $200 \times 10^5 \text{ A cm}^{-2}$  for a  $1\mu\text{s}$  pulse. The steady state current density is kept less than  $2 \times 10^5 \text{ A cm}^{-2}$ .

### OUTPUT PROTECTION

The historic approach to output protection is to do nothing. Since output devices have PN junctions that breakdown at reasonable voltages and conduct static currents, there has been little historic problem from higher impedance static discharges, compared to the input gate protection. Adding series current limiting from the output driver to the package pin detracts from the fast rise time characteristics when driving capacitive bus structures, so series resistance would usually be minimized.

A computer subsystem might have outputs and inputs interconnected on a bus with a low characteristic impedance for short pulse widths. Our tests have shown failure of the output drain junctions with only 90V pulses, 1us wide. Thus the output FETS are more susceptible to failure than the inputs described above. A balanced design requires some output protection.

The clamping action of the drain-body diodes in the output buffer transistors is poor, since the short channel regions have considerable lateral bulk resistance. Improved protection is obtained by adding low bulk resistance reverse biased clamp diodes shunting the output surge currents to  $V_{DD}$  or  $V_{SS}$ . The capacitive loading of these diodes is quite negligible, and they are sized so that the more easily controlled series output resistor  $R_1$  is the weakest element.

Since the output drain junctions can reverse breakdown (worst case) or forward bias to the power lines, a double L attenuator design is achieved by placing a limiting resistor  $R_1$  from the output to diode clamps returned to the  $V_{SS}$  and  $V_{DD}$  supplies. Since the output bus has much higher capacitance than the input gate, the resistance must be lower. Then a second resistor,  $R_2$ , of much lower power dissipation, connects to the output drains. The failure voltage of  $R_1$  is directly proportional to length, so the resistor must be large. A lower resistivity n+ diffusion ( $33 \Omega/\square$ ) was used to thin the width and give a longer aspect ratio for the output resistor, which is 252um long, 70um wide. The output layout is shown in Figure 8.  $R_1$  is 120 Ohms,  $R_2$  is 100-Ohms, and each diode that clamps to the supplies is formed with two parallel

diodes of the same design as the input. Failure occurs in R1 with a 100ns 580V pulse applied to the output, a 220V peak appears across the two clamp diodes, and the FET drain junctions survive and still can be switched into high impedance with leakages less than 100na. The most significant penalty for this output protection into a 50pf output bus is 10ns of added delay.

The area needed for R1 and the four clamp diodes is  $0.06\text{mm}^2$ . R2 is needed anyway as a cross-under. Thus 4 output protect networks add only 0.6% more area to the PSM die.

#### ACKNOWLEDGEMENTS

The authors are indebted to the many careful measurements and detailed post mortem analysis performed by Mr. Richard Washabaugh.

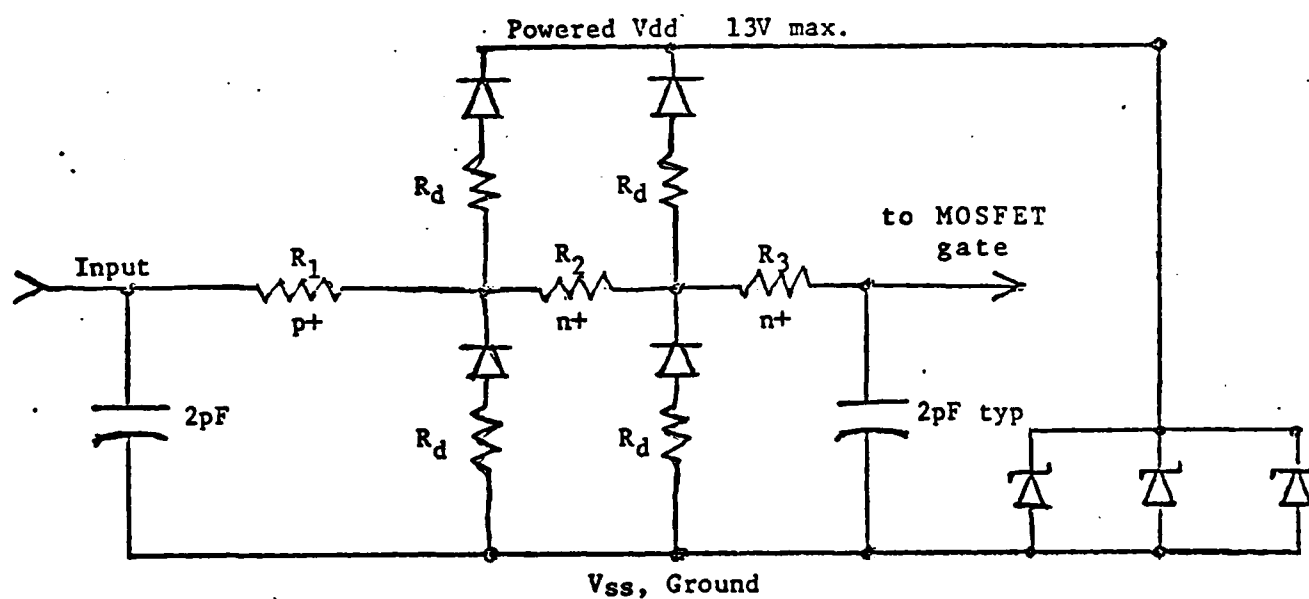
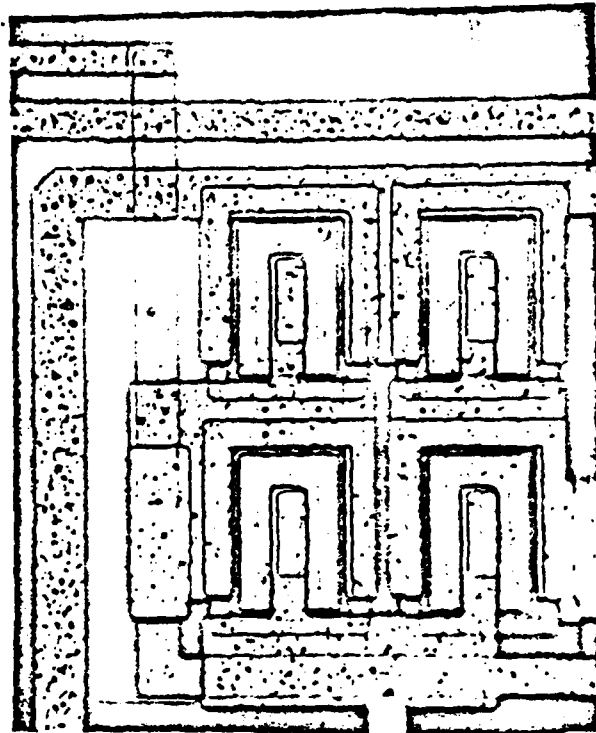


FIGURE 2, INPUT ATTENUATOR TOPOLOGY

TO INPUT PAD



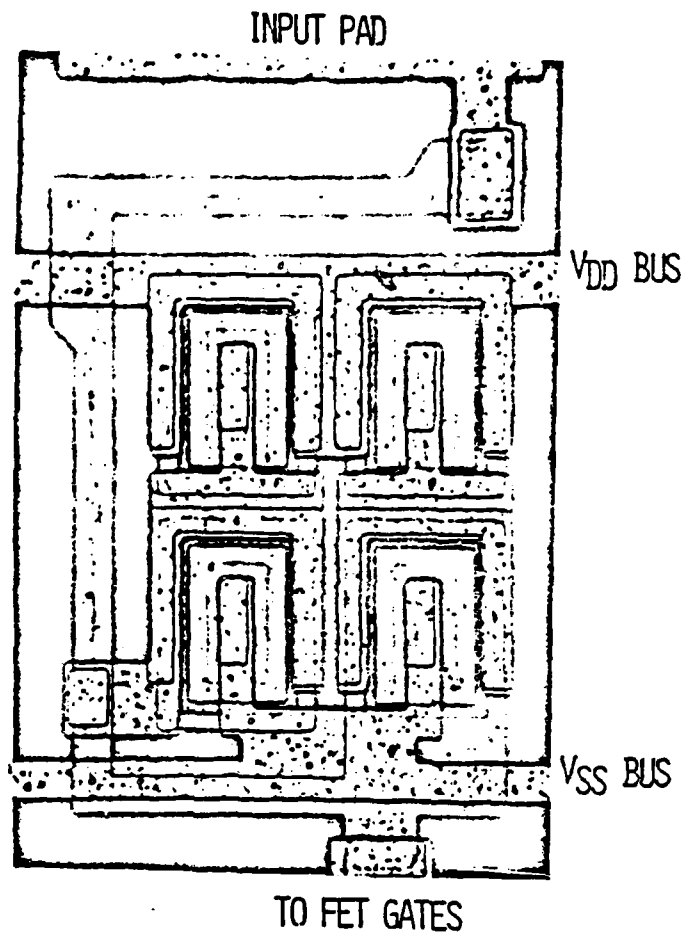
2ND SIGNAL

VDD BUS

TO FET  
GATES

VSS BUS

ORIGINAL INPUT PROTECTION LAYOUT  
FIGURE 3



IMPROVED INPUT PROTECTION LAYOUT  
FIGURE 4

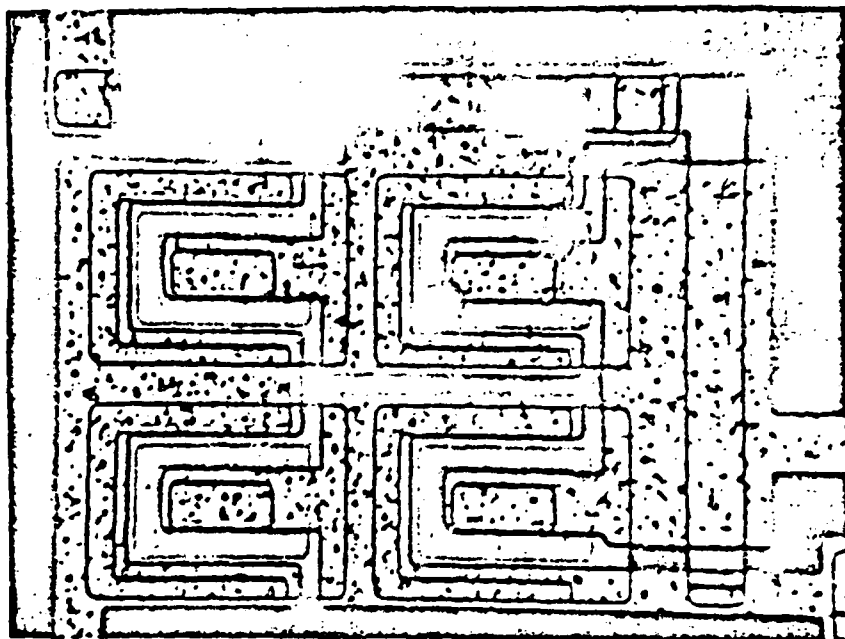
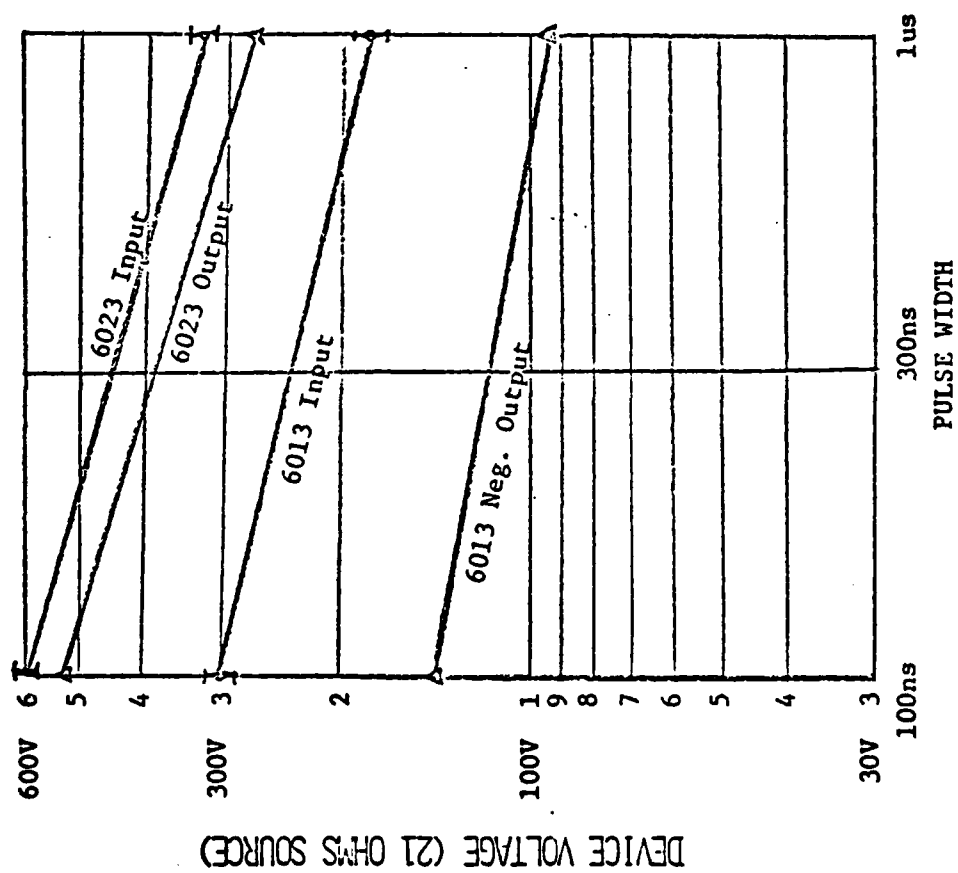
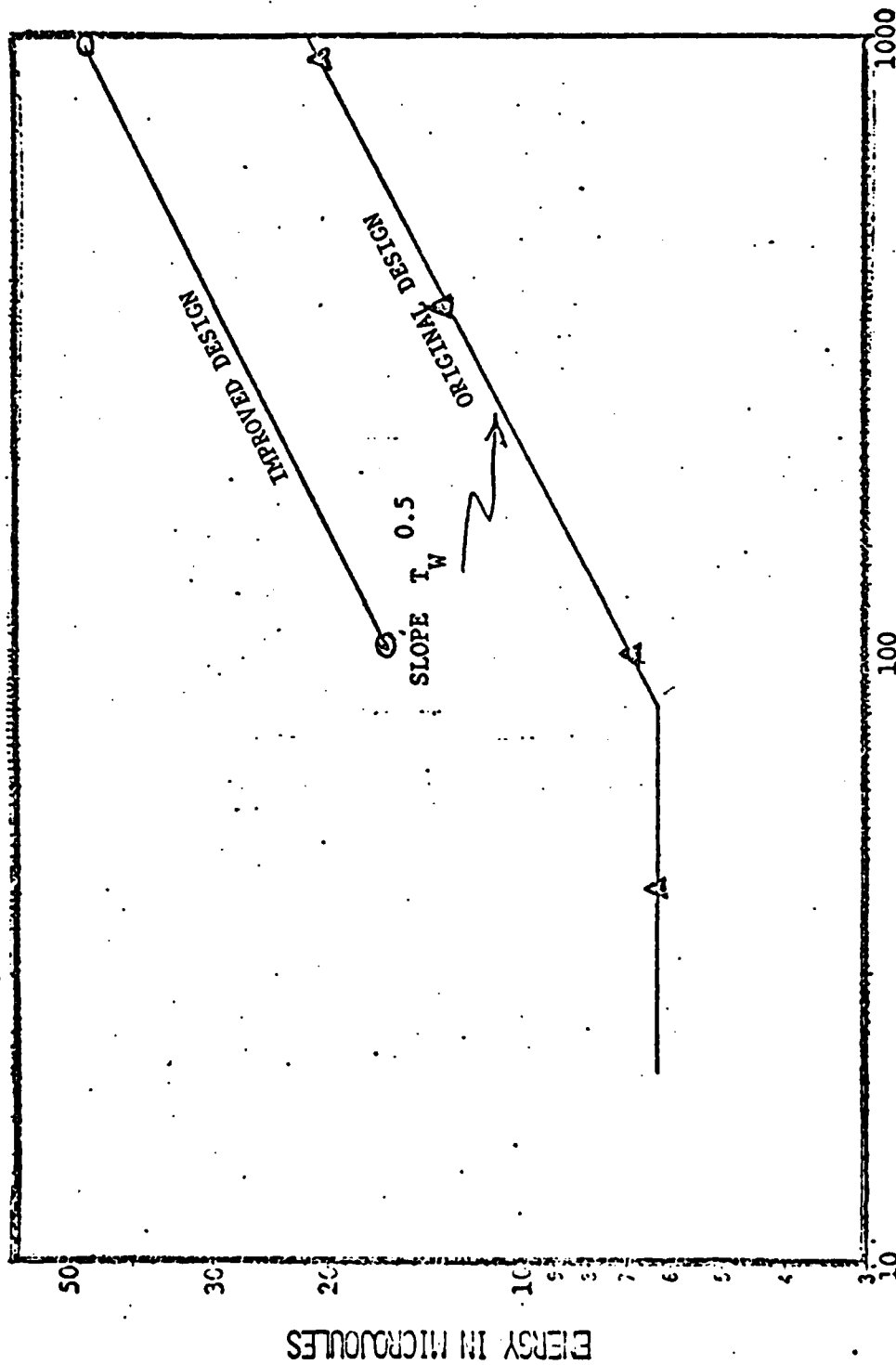


FIGURE 5, ROM INPUT NETWORK, POST FAILURE



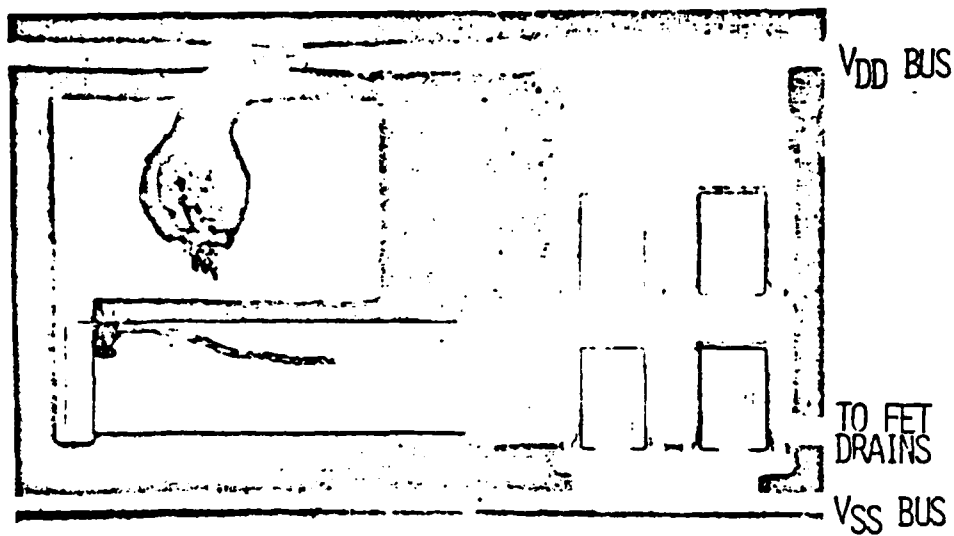
INPUT/OUTPUT PROTECT VOLTAGES  
FIGURE 6



PULSE WIDTH IN NANSECONDS  $T_W$

COS/SOS INPUT PROTECT ENERGY

FIGURE 7



OUTPUT PROTECTION LAYOUT, POST FAILURE  
FIGURE 8

## LIST OF REFERENCES

1. Military Specification, "High Voltage Zap Test of Input Protection Circuits" MIL-M-38510/52A, Microcircuits, Digital, CMOS, NOR Gates, Paragraph 4.5.3, p. 27-28, September 1974.
2. R. K. Panchoby, "SOS Gate Protection", Scientific Report RADC-TR-77-134, April 1977.
3. L. W. Linholm, R. F. Plachy, "Electrostatic Gate Protection using an Arc Gap Device". IEEE 11th Annual Reliability Physics, p. 198, 202 (1973).
4. F. H. De LaMoneda, D. E. Debar, K. P. Stuby, C. L. Bertin, "Hybrid Protective Device for MOS-LSI Chips", IEEE Transactions on Parts, Hybrids and Packaging, Vol. PHP-12, No. 3, p. 172-175, September 1976.
5. P. P. Budenstein, D. H. Pontius, W. B. Smith, "Secondary Breakdown and Damage in Semiconductor Junction Devices", Report RG-TR-72-15, U. S. Army Missile Command, Redstone Arsenal, Alabama, (1972).
6. W. R. Runyan, Silicon Semiconductor Technology, McGraw-Hillbook Company, New York, (1965).
7. D. H. Pontius, W. B. Smith, P. P. Budenstein, "Filamentation in Silicon-on-Sapphire Homogeneous Thin Films", J. Appl. Phys., 44-1, p. 331 (1973).
8. Wunsch, D. C. and Bell, R. R., "Determination of Threshold Failure Levels of Semiconductor Diodes and Transistors Due to Pulse Voltages", IEEE Trans. Nucl. Sci., NS-15, 1968, p. 244-259.
9. J. Spratt, "Proposed Design Rules of Burn-Out Protection", Internal RCA Report, April 1977.
10. H. Gurev, "Sensitivity of Current Pulse Burn-Out testing to the Geometry of Defects in Aluminum Metallization", IEEE 12th Annual Proceedings Reliability Physics, p. 187-195, (1974).
11. J. Cornell, "Gamma Pulse Survivability Calculations for Digital Circuits", Internal Harris Corporation Report, p.17, March 1978.

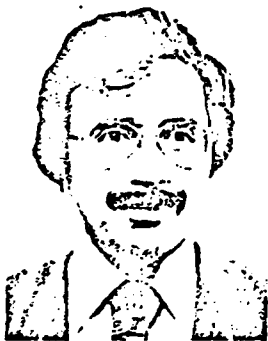
## FIGURE CAPTIONS

- Figure 1 Input Waveforms
- Figure 2 Input Attenuator Topology
- Figure 3 Original Input Protection Layout
- Figure 4 Improved Input Protection Layout
- Figure 5 Row Input Network, Post Failure
- Figure 6 Input/Output Protect Voltages
- Figure 7 CMOS/SOS Input Protect Energy
- Figure 8 Output Protect Layout, Post Failure



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He was employed at the Naval Electronics Laboratory in underwater countermeasures in 1949-51. Currently he is a Research Engineer at the Northrop Corporation, Electronics Division in Hawthorne, California where he has been occupied in staff and electronics assignments for the past twenty-six years. He is a member of the Northrop Corporate Radiation committee and has been involved with radiation effects on electronics and missile applications for the past fifteen years. His current position is Technical Director of the LSI SOS parts development on the Advanced Computer Technology contract from SAMSO.



**J. Ronald Cricchi (SM'66)** was born in Glen Ridge, NJ, on January 22, 1935. He received a Certificate of Electrical Engineering and the B.S. degree in electrical engineering from the Johns Hopkins University, Baltimore, MD, in 1956 and 1960, respectively.

In 1953, he joined the Westinghouse Defense and Electronic Systems Center, Baltimore, MD. Since 1960, he has been responsible for research and development programs in digital and linear integrated circuits, complementary MOS integrated circuits and MIS interface phenomena. He has been Program Manager of several nonvolatile semiconductor memory development programs since 1968. He has also been concerned with reliability and radiation effects in IGFET structures. He is the author of a number of papers in these fields and over 25 patents have been issued in his name. He is presently an Advisory Engineer in the Solid State Technology Section of the Westinghouse Advanced Technology Laboratories, Baltimore, MD. He is a Registered Professional En-

gineer.

Mr. Cricchi has served in IEEE activities as a member of the MNOS Standard's subcommittee and a Program Chairman of the 1976 IEEE Non-Volatile Semiconductor Memory Workshop. He is the 1977 General Chairman for the same meeting.



Douglas A. Barth (S' 69-M 71) was born in Detroit, Michigan, on June 3, 1949. He received the B.S. degree in Electrical Engineering from the University of Michigan, Ann Arbor, and the M.S. degree in Electrical Engineering from the Johns Hopkins University, Baltimore, Maryland, in 1971 and 1973, respectively.

Since 1971, he has been with the Westinghouse Advanced Technology Laboratories, Baltimore, Maryland and is presently a Senior Engineer in the Solid State Technology Group. He has been involved in the design and fabrication of bipolar microwave transistors, the fabrication and evaluation of charge-coupled devices, and is presently involved in CMOS/SOS and MOS LSI technology programs. He has also been involved in semiconductor measurement techniques and ion implantation processes for LSI. He is presently working towards the Ph. D. degree at the University of Maryland, College Park.

Mr. Barth received the Westinghouse Advanced Study Award in 1974.

## BUILT-IN MEMORY CELL TEST FEATURE FOR A RADIATION HARDENED 1024-BIT MNOS/SOS ELECTRICALLY PROGRAMMABLE NONVOLATILE MEMORY

M.D. Fitzpatrick, J.R. Cricchi, B.L. Stamps  
Westinghouse Electric Corporation  
Baltimore, Maryland

### Introduction

A random access 256 x 4 MNOS/SOS nonvolatile memory has been designed, processed, and characterized. This CMOS compatible memory dissipates less than 300 mW with an access time of less than 400 nsec at total dose levels exceeding 500K rads (Si). A unique memory cell test feature has been incorporated in the design and allows an analog measurement of memory windows for all 1,024 memory cells. This built-in test feature easily allows direct measurement of memory array performance as well as being a useful diagnostic tool.

### Array Characteristics and Features

A summary of characteristics and features of this 256 x 4 MNOS/SOS nonvolatile random access memory is given in table I.

Utilizing the unique depletion mode complementary symmetry circuits (DM-CMOS)<sup>1</sup> in conjunction with a radiation hardened process<sup>2</sup>, which is compatible for both memory devices and fixed threshold devices required in the address and control logic, access times of 400 nsec at total dose levels exceeding 500K rads (Si) have been achieved.

This high-speed, low-power memory is intended for program storage applications with a retention of 3 years after 10<sup>4</sup> write reversals. A unique decoding scheme allows random access in both the clear write and read modes to allow true word alterability.

To enhance data detection and maximize retention of the array, a balanced detection scheme incorporating two MNOS drain-source protected memory FET's for each storage cell was used. One of the parameters which determines the retention of any given cell is known as the memory window of that cell. The memory window is simply the difference in threshold voltages of the two MNOS FET's which make up that cell.

### Memory Window Test Circuitry and Retention Measurements

In order to determine overall retention of a memory array, the memory window voltage as a function of time must be known for all cells in order to determine the worst-case window which will ultimately limit the long term retention of the array. Previous designs had to rely on characteristics of a single test FET not in the array or to operate the array with nonstandard voltages and timing to arrive at a prediction of the long term retention of the array. Neither of these methods has proved to be satisfactory. The design described herein utilizes a simple circuit which allows direct analog measurement of the memory window as a function of time for all 1,024 cells and thereby allows an accurate measurement of long term retention for the entire array.

This circuit, which utilizes P-channel enhancement mode devices, is shown in figure 1. The only additional elements re-

quired for the test feature are P1 - P4 which are present for each I/O bit.

In the test mode of operation, TEST ENABLE goes high which disconnects the latch from V<sub>DD</sub> and TEST ENABLE goes low which gates the memory source line voltages to the MT and  $\overline{MT}$  output pins. Otherwise operation occurs if the array were in a normal read mode of operation. It can be seen that by taking the difference of the MT and  $\overline{MT}$  outputs, the memory window for each cell can be obtained:

$$\Delta V_{TM} = MT - \overline{MT} \\ = V_{READ} - V_{TM1} - (V_{READ} - V_{TM2})$$

$$\Delta V_{TM} = V_{TM2} - V_{TM1}$$

A photograph of 256 memory windows (one I/O) measured by connecting the MT and  $\overline{MT}$  outputs to the differential input of an oscilloscope is shown in figure 2. By viewing the memory windows this way, one can determine if any write disturb conditions or addressing sensitivities exist in the array. In addition, this is a very useful tool for examining memory window uniformity.

By measuring the memory window as a function of time, one can predict long term retention for the array. Figure 3 shows a plot of memory window voltage vs time for cells which have undergone 10<sup>4</sup>, 10<sup>6</sup>, and 10<sup>8</sup> endurance reversals. By extrapolating over a fraction of one decade, retention is predicted to be much more than 3 years (10<sup>8</sup> seconds) after 10<sup>4</sup> clear-write reversals, near 3 years after 10<sup>6</sup> reversals, and 3 months to 1 year after 10<sup>8</sup> reversals.

### Determination of Other Array Parameters

In addition to retention measurements, the memory window test feature may be used to measure other array parameters.

The detection circuit sensitivity, which must be known in order to predict long term retention, can be easily determined and has been found to be less than 100 mV (i.e., proper data state will be determined for a memory cell with a window of 100 mV or greater).

Write characteristics of the array can also easily be obtained by measuring the array memory window as a function of write voltage. This type of information is invaluable in providing guard band limits for specifying retention time.

In memories intended for program storage, as this one is, the read mode of operation is the predominant one. In many MNOS memories, constant readout of the array can degrade the memory window resulting in premature retention failure. It therefore becomes very important to be able to measure the memory window as a function of a number of read cycles. This data, which is again provided by the built-in test feature, indicates an actual enhancement of the window occurs which will result in an improvement in retention time for the array.

This work was supported by the U. S. Air Force, Space and Missile Systems Organization (SAMSO), Contract F44704-75-C-0006, Monitored by Capt. R. Warzynski.

### Statistical Analysis

In order to obtain a statistical data base for memory window measurements, a program has been generated on a computer-controlled MD-501 LSI tester which automatically takes memory window measurements for all 1,024 memory cells. This data may be printed out in histogram form or used to generate a geographical map of the memory windows. The array may be stored under various conditions (TBS, rad, zero-bias, etc) and then the test can be repeated at a later time yielding both an indication of window uniformity as well as retention characteristics for all bits in the array.

### REFERENCES

1. Fitzpatrick, et al., "MNOS/SOS Memory Using High-Voltage Depletion - Mode CMOS Logic," 1975 GOMAC Digest of Papers, Pg. 196.
2. Cricchi, et al., "Hardened MNOS/SOS Electrically Reprogrammable Nonvolatile Memory," IEEE Trans. on Nuclear Science, NS-24, Pg. 2185, Dec. 1977.

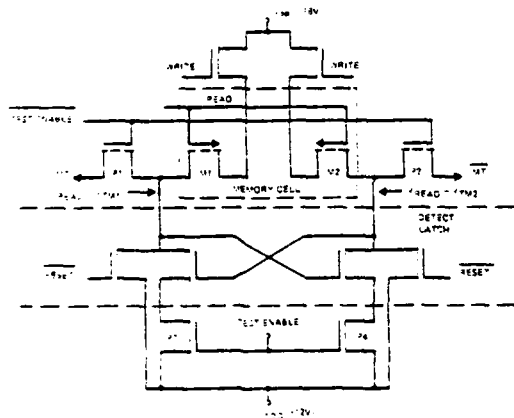


Figure 1. Detection and Memory Window Test Circuitry

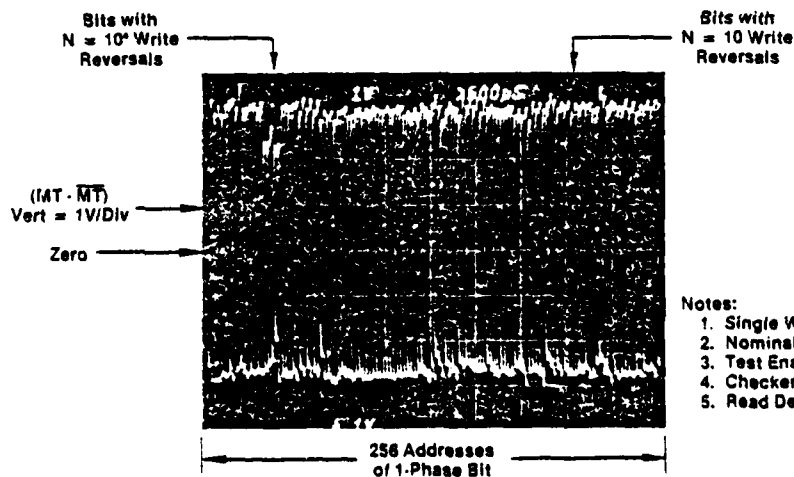


Figure 2. Measurement of Memory Window

TABLE I  
PERMANENT STORE MEMORY:  
CHARACTERISTICS AND FEATURES

- 256 X 4 Organization
- Random Access
  - Clear/Write Cycle 200  $\mu$ s
  - Read Cycle 500 ns
  - Read Access 250 ns
- Retention 3 Years
  - After  $10^4$  Reversals
- Endurance  $10^6$  Cycles
  - with 3 Months Retention
- Power (mW)
  - Read 390
  - Write 37
  - Standby < 1
- CMOS Compatible Inputs and Outputs
- MNOS/SOS Technology
- Two PMNOS FETs Per Bit
- Differential Detection
- Read Enhancement
- PEST and NDMT Circuitry
- Test Mode for Analog Measurement of All Memory  $V_T$
- Single Block Clear Option
- Three Power Supplies and Ground
  - +12V, -9V, -18V

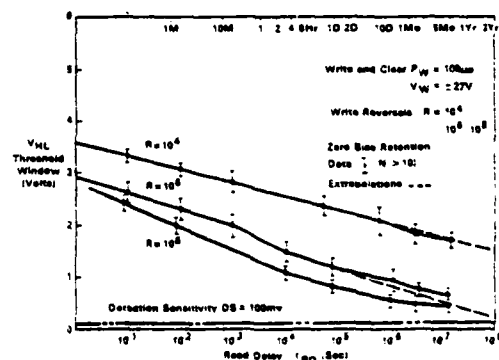


Figure 3. PSM: Pulse Response and Retention

### Notes:

1. Single Write Cycle,  $t_w \approx 100 \mu$ s
2. Nominal Supply Voltages
3. Test Enable Mode (TE = +12)
4. Checkerboard Pattern
5. Read Delay = 30 Sec

RADIATION HARDENED MNOS-CMOS/SOS FAST WRITE RAM\*

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Date:

July 14, 1978

For the

IEEE Annual Conference on  
Nuclear and Space Radiation Effects  
18-21 July, 1978  
Albuquerque, New Mexico

## RADIATION HARDENED MNOS-CMOS/SOS FAST WRITE RAM\*

J.R. Cricchi, D.W. Williams, J.L. Fagan, F.C. Blaha, B.G. Stamps

Westinghouse Electric Corporation  
Baltimore, Maryland 21203

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Northrop Corporation  
Hawthorne, California 91274

A fast write nonvolatile silicon nitride CMOS on sapphire memory device has been fabricated and tested. The device is being developed as a potential replacement for hardened plated wire memory. The MNOS memory incorporates hardened low voltage (12V) and high (30V) CMOS/SOS logic and control circuits required for low power and minimum write cycle time. The memory is organized as a 512 word by 1 bit random access memory in both the write and read modes. The write cycle time is less than 1.4 $\mu$ s, the read access time is less than 250nsec and the power dissipation is less than 200 mw. A significant feature of the memory operation is that the two MNOS memory transistors per memory cell are written simultaneously to opposite memory states to reduce the write cycle time.

### Device Technology

A nitride-oxide gate insulator SOS technology is used because it is compatible with both the drain source protected nonvolatile MNOS memory and the fixed threshold devices required. Both P and N enhancement mode, low (12V) and high (30V) voltages devices are used in the CMOS/SOS circuits. The P channel MNOS memory device which contains both fixed threshold and variable threshold regions is shown with the high voltage n-enhancement device in Figure 1. The threshold and back channel leakage of the N-channel device are controlled by ion implantation of boron.

The nitride-oxide gate insulator and ion implant levels are similar to that described for a radiation hardened CMNOS/SOS ROM and an electrically alterable MNOS/SOS memory.<sup>1,2</sup> The nitride-oxide insulator characteristics have been improved by the use of resistance heated low pressure chemical

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\*This work was supported by the U.S. Air Force, Space and Missile Systems Organization (SAMSO), Contract F04704-75-C-0006, monitored by Capt. R. Warzynski.

vapor deposition (LPCVD) of silicon nitride from dichlorosilane rather than the atmospheric pressure CVD rf heated system using silane. The LPCVD nitride provides significantly improved uniformity of thickness, initial charge, stability and radiation hardness.

The N and P-channel threshold shifts after  $\text{Co}^{60}$  total dose radiation are shown for different gate bias conditions in Figure 2. The initial  $V_{Tp}$  is -2.8 to -3.2 volts and the initial  $V_{Tn}$  is +1.4 to +1.8 volts. It has been shown previously that the threshold shifts are linearly proportional to the nitride thickness.<sup>1</sup> The LPCVD nitride exhibits the same characteristic as shown in Figure 3.

The gate oxidation technique and oxide thickness have a significant effect on the total dose hardness. A study was made of the effect of oxide thickness on radiation hardness for oxidation techniques. One technique was a pyrogenic  $\text{H}_2 + \text{O}_2$  oxidation at 800C and the other a dry  $\text{O}_2$  oxidation at 900C. The sensitivity of the radiation induced threshold shift as a function of the oxide thickness is shown in Figure 4. The dry  $\text{O}_2$  oxidation has a much smaller sensitivity.

#### Nonvolatile RAM Design and Characteristics

The radiation hardened nonvolatile fast write MNOS-CMOS/SOS RAM has been designed, processed and characterized. Further development and evaluation of the radiation hardness is continuing. The 512 word by one bit RAM contains both 12V and 30V CMOS address and control circuits. The design incorporates level shifting circuits which allow only the following bias conditions to exist: N-channel gate source bias  $V_{GS}$  of 0 to +12; P-channel  $V_{GS}$  0 to -30V; memories  $V_{GS}$  of  $\pm 30\text{V}$ .

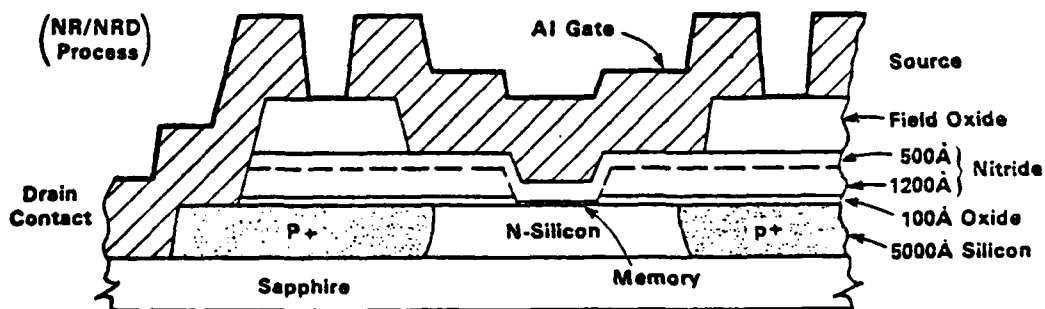
A block diagram of the memory is shown in Figure 5. Note that two 512 transistor memory arrays are decoded. This is to allow writing of the two memory transistors per bit to occur simultaneously, one to a high conductance state and the other to a low conductance state. This minimizes the write cycle time. A second significant feature is that during a write cycle, data is first read out and compared to incoming data before writing is allowed. This read compare mode prevents the memory transistors from being driven into an unrecoverable state by multiple write pulses of the same polarity. A photograph of the 512 x 1 MNOS-CMOS/SOS memory is shown in Figure 6. LSI Memory array retention times of up to a week have been obtained after  $10^8$  write cycles of 1usec width and  $\pm 30\text{V}$  amplitude. Retention data is shown in Figure 7.

The pre-rad measured electrical characteristics and design features of the 512 x 1 fast write nonvolatile RAM are shown in Table 1. Only  $\text{Co}^{60}$  total dose data has been taken for a small sample of developmental parts. These parts were irradiated in the static deselect mode. The read access time was less than 250ns after a total dose of 100K rads, however, this is the extent of the tests to date. The radiation tests on the complete array are continuing.

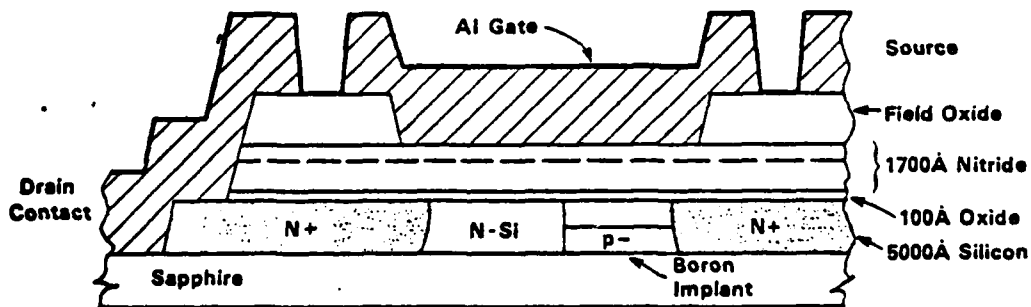
## Conclusion

There are several significant aspects of this work. One is the improved radiation hardness of the nitride-oxide gate insulator along with greater understanding of process variables affecting hardness. A second is the development of CMOS/SOS technology compatible with nonvolatile MNOS memory. A third significant factor is a number of new concepts for the memory operation. All of these factors contribute to the low power, fast write performance and radiation hardness. Although this part is not fully developed, this new technology continues to show promise of replacing hardened plated wire memory.

**FIGURE 1**  
**Drain Source Protected MNOS/SOS Memory X-Section**



**Implanted N-Enhancement Mode SOS IGFET (High Voltage)**

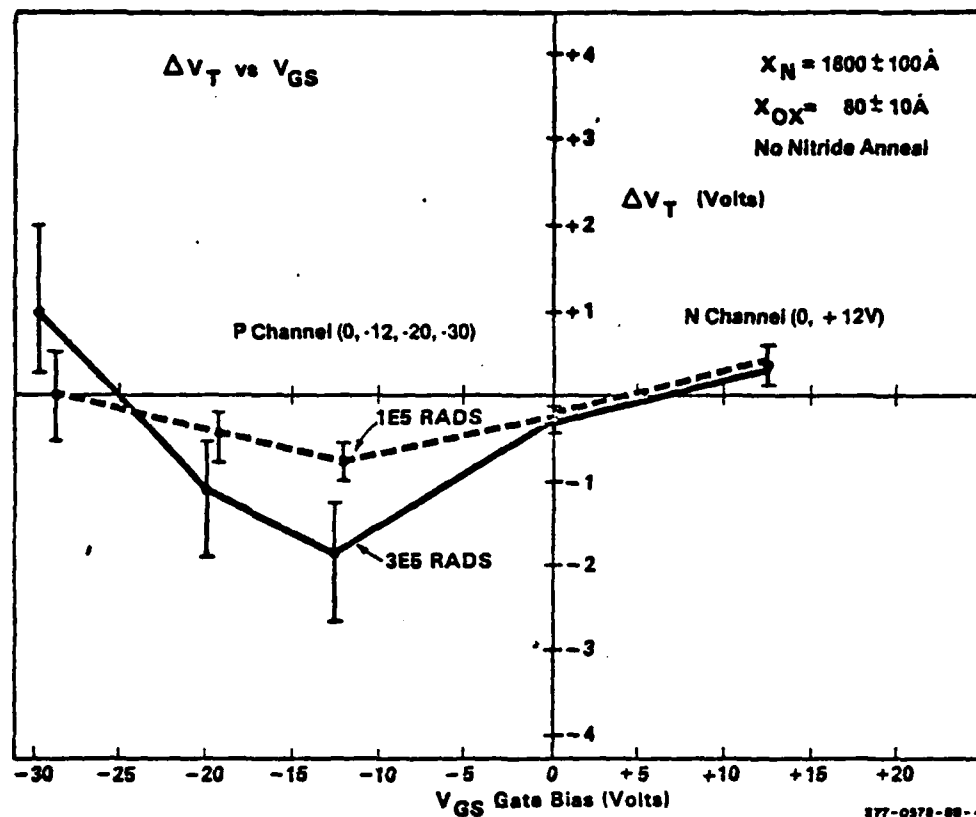


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<sup>1</sup>J.R. Cricchi, M.D. Fitzpatrick, F.C. Blaha, and B.T. Ahlport, "Hardened MNOS/SOS Electrically Reprogrammable Nonvolatile Memory," IEEE Trans. on Nuclear Science, NS-24, Page 2185, December 1977.

<sup>2</sup>J.R. Cricchi, D.A. Barth, H.G. Oehler, R.C. Lyman, J.M. Shipley, "A High Speed Radiation Hardened CMOS/SOS Mask Programmable ROM and General Processor Unit," IEEE Trans. on Nuc. Sci., NS-24, Page 2236, December 1977.

**FIGURE 2**  
Radiation Induced Threshold Shift vs Applied Gate Bias  
LPCVD Nitride



**FIGURE 3**

Threshold Shift vs Effective Nitride Thickness  
LPCVD Nitride

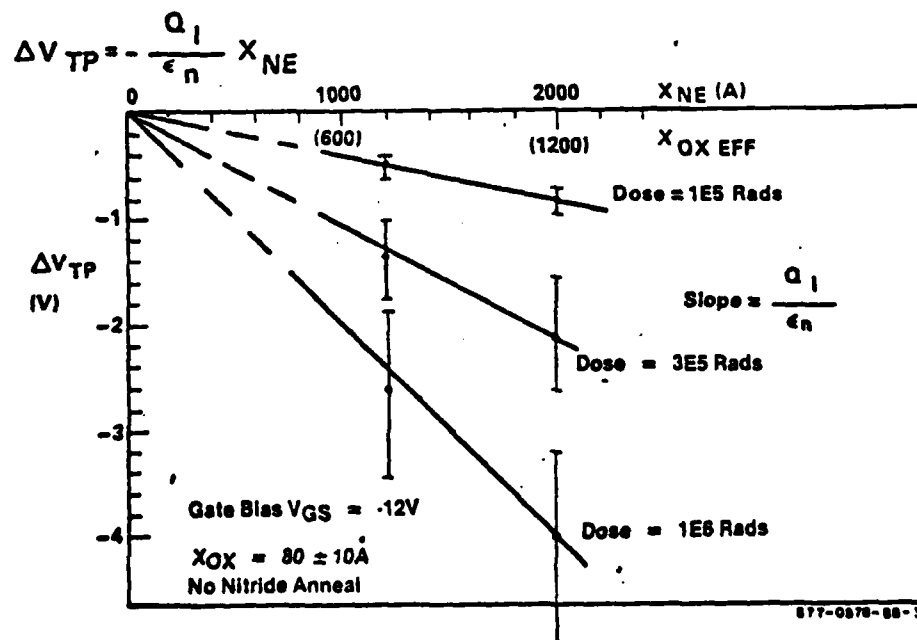


FIGURE 4  
Flatband Shift vs Oxide Thickness

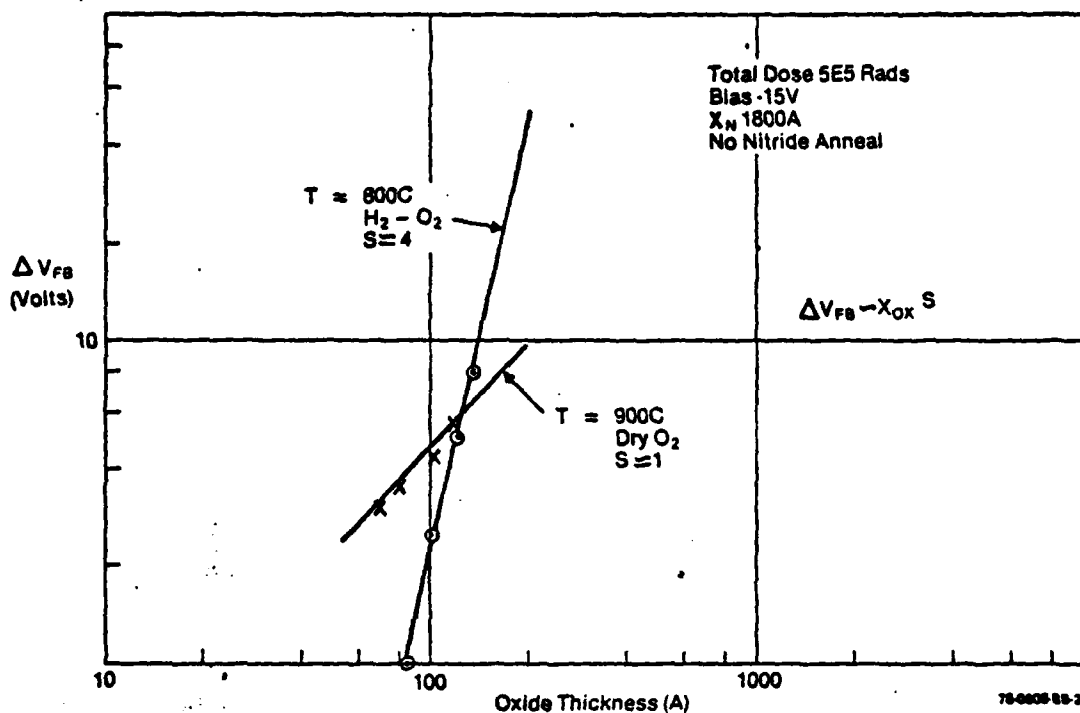
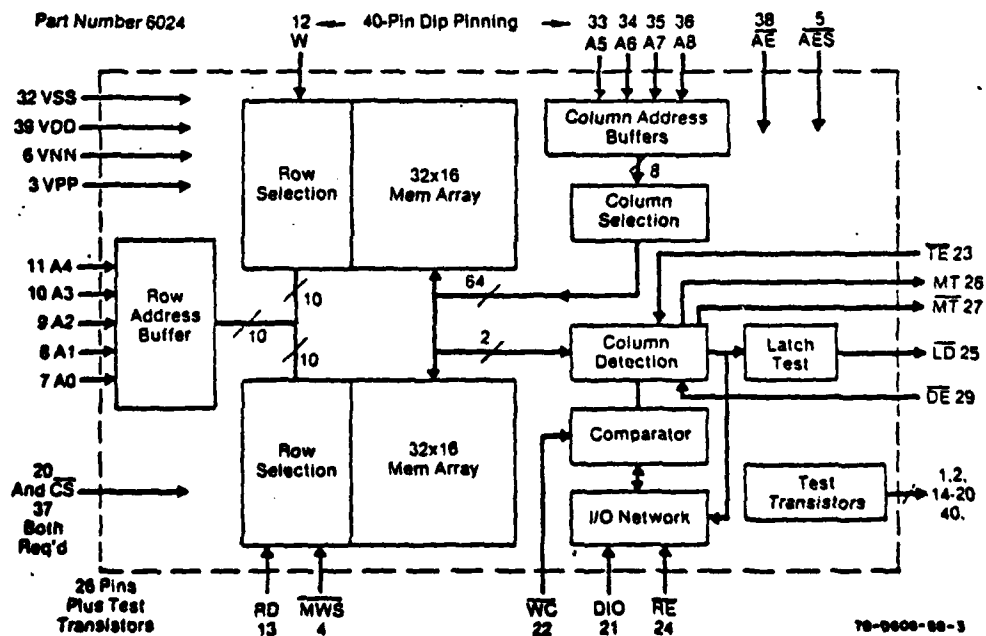


FIGURE 5  
TSM 512 x 1 Simplified Block Diagram  
MNOS/SOS



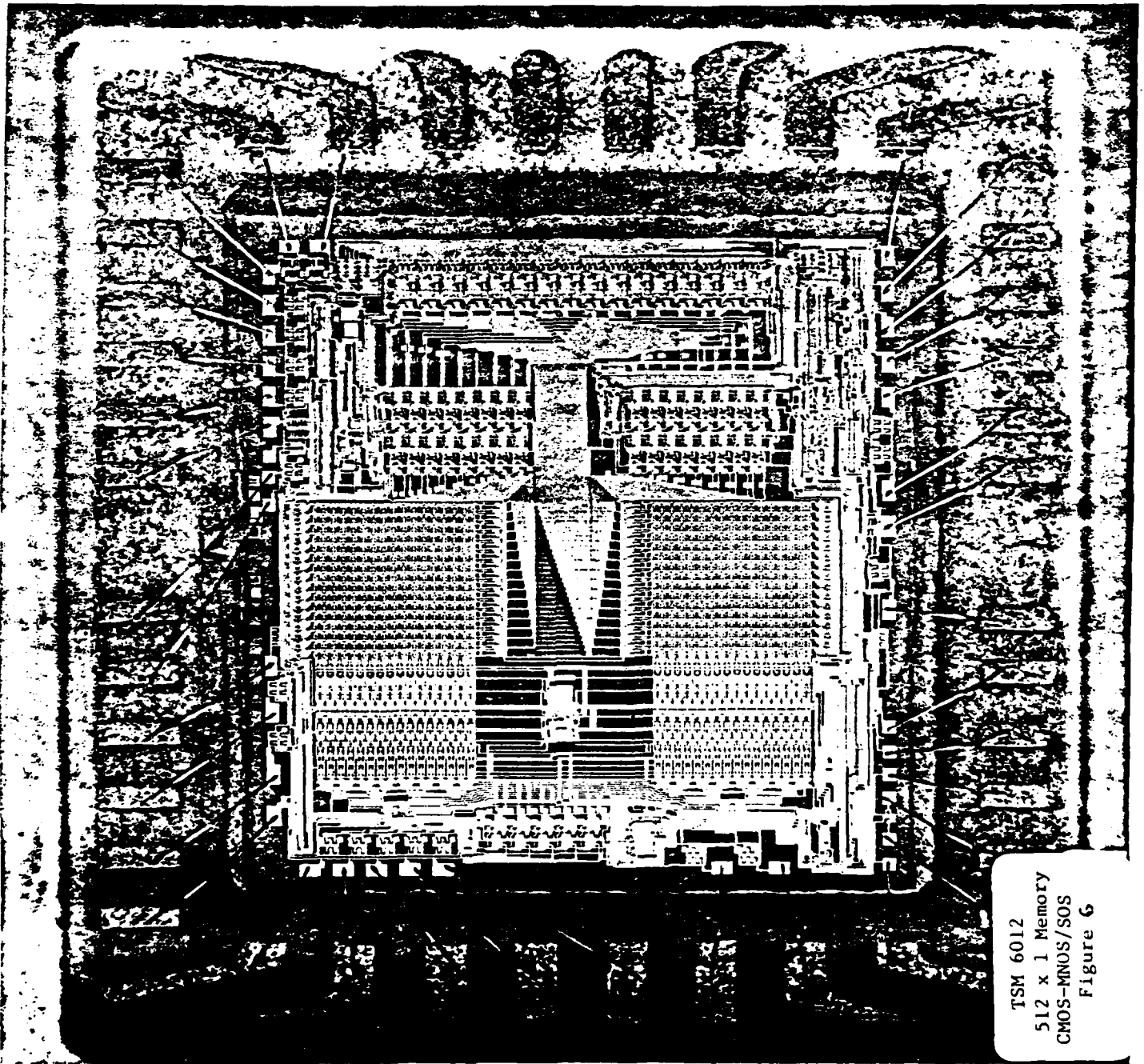


FIGURE 7

TSM: Retention for Fast-Write MNOS  
Write Pulsewidth 1.0  $\mu$ s, Voltage 30V

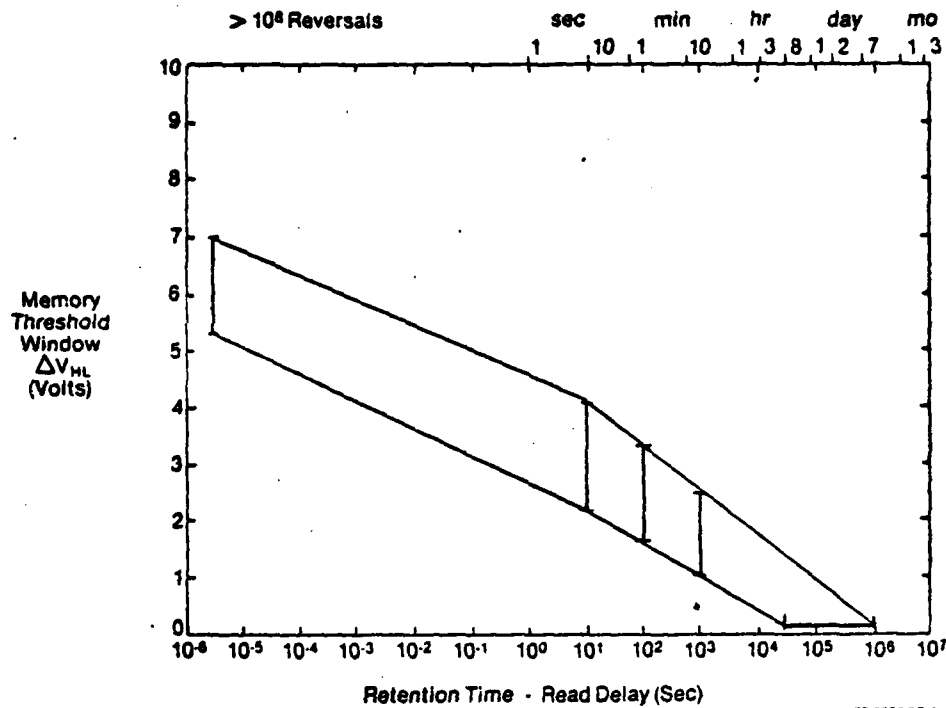


FIGURE 8

TSM: Temporary Store, Fast Write Memory

Characteristics

- 512 x 1 Organization
- Random Access
  - Write Cycle 1.4  $\mu$ sec
  - Read Cycle 0.6  $\mu$ sec
  - Read Access 250 nsec
- Retention 8 to 160 Hours After  $10^5$  Reversals
- Endurance -  $10^{12}$  Cycles Demonstrated on Single Transistors
- Low Power - 150 mW Operating 2 mW Standby
- Three Supplies and Ground +12V, -9V, -18V

Features

- Two PMNOS FET's Per Bit
- Low and High Voltage CMOS/SOS (PEMT, NEMT, HVPENT, HVNEMT)
- Read Compare Before Write Prevents Saturation
- Differential Write (Simultaneous)
- Write Voltage Independent of  $V_T$
- Differential Detection
- CMOS Compatible Inputs and Outputs
- Memory  $V_T$  Test Mode

78-0808-28-5

**NORTHROP**

Electronics Division

APPENDIX B

SPECIFICATION FOR MPROM, 26760502



AD-A085 969 NORTHROP CORP PALOS VERDES PENINSULA CALIF ELECTRONICS DIV. F/G 9/2  
ADVANCED COMPUTER TECHNOLOGY-I (ACT I)  
01 MAY 80 F04704-75-C-0006 NL

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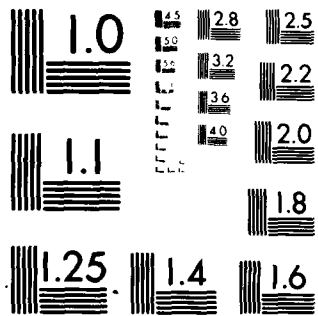

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MICROCOPY RESOLUTION TEST CHART  
NATIONAL BUREAU OF STANDARDS-1963-A

# 1. SCOPE

- 1.1 Scope. This specification covers the detail requirement for a monolithic silicon on sapphire, CMOS/SOS, mask programmable, 1024 bit, organized 256 words by 4 bits, Read Only Memory (ROM) Microcircuit.

The ROM microcircuit incorporates both P-channel and N-channel enhancement mode devices as well as Tri-State Outputs which are directly controllable by a chip select complement (CS) input. A data ready complement (DR) output is provided for use as EN for second level ROMS.

- 1.2 Part Number. The complete part number shall be 26760502 .

- 1.3 Device Class. The device class shall be Product Assurance Level Class B as defined in MIL-M-38510.

- 1.4 Case Outline. The case outline shall be per Figure 1 (40-pin, 0.60" x 2.0", dual-in-line configuration).

- 1.5 Absolute Maximum Ratings.

Supply voltage range ( $V_{DD} - V_{SS}$ )----- -0.5V to +15V (< 1 m Sec)  
 Input current (each input)-----  $\pm 3$  mA  
 Input capacitance  
     Any input----- 5pf  
 Input voltage range-----  $1.2V \leq V_I \leq V_{DD} + 1.2V$   
 Storage temperature range----- -65° to 175°C  
 Maximum power dissipation----- 300 mW (< 1 m Sec)  
 Lead temperature----- 300°C  
 Junction temperature-----  $T_J = 175^\circ C$

- 1.6 Recommended Operating Conditions. ( $V_{SS} = 0$  Vdc, Ground)

Supply voltage ( $V_{DD}$ )----- 12 Vdc + 1, -2Vdc  
 Minimum high level input voltage----- ( $V_{DD} - 1.2V$ )  
 Maximum low level input voltage----- 1.2 Vdc  
 Normalized fanout (each output)----- 10 maximum ( $\pm 5$  mA)  
 Ambient operating temperature range----- -55°C to 125°C

Northrop Corporation Electronics Division Palos Verdes Peninsula, California	SIZE	CODE IDENT NO.		
	A	22915	26760502	
	SCALE	REV	SH	2



1.6.1 Dynamic Operating Conditions ( $T_A = 25^\circ\text{C}$ )  $10\text{V} \leq V_{DD} \leq 13\text{V}$

Cycle time, $t_{\text{cycle}}$	-----	250nsec minimum
Address Setup delay, $t_{AS}$	-----	40ns minimum
Address Release time, $t_{AR}$	-----	100ns minimum
CS delay to enable data out, $t_{DE}$	-----	55ns minimum
Access time, $t_{ACC}$	-----	148ns maximum
EN to data out delay, $t_{EN}$	-----	20ns minimum
CS delay to disable data out, $t_{DD}$	-----	55ns maximum
EN Deselect width, $t_{ED}$	-----	40ns minimum
Data Ready delay ( $t_{DR} > t_{ACC}$ ), $t_{DR}$	-----	166ns maximum
, $t_{CS}$	-----	150nsec
, $t_{CSW}$	-----	100nsec
, $t_{CSD}$	-----	50nsec

NOTE: All timing measured at 50% pt unless otherwise specified.

$C_{LOAD} = 15\text{pf}$ ,  $V_{DD} = 10\text{V}$

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	A	22915	
	SCALE	REV	SH 3



2. APPLICABLE DOCUMENTS

- 2.1 The following documents, of the issue in effect on date of this specification, form a part of this specification to the extent specified herein.

SPECIFICATIONS

MILITARY

- MIL-M-38510 - Microcircuits, General Specification for.  
MIL-M-55565 - Microcircuits, Packaging of.

STANDARDS

MILITARY

- MIL-STD-883 - Test Methods and Procedures for Microelectronics

3. REQUIREMENTS

- 3.1 Detail Specifications. The individual item requirements shall be in accordance with MIL-M-38510, and as specified herein. In the event of conflict between MIL-M-38510 and this detail specification, this detail specification shall govern.
- 3.2 Design, Construction, and Physical Dimensions. The design, construction, and physical dimensions shall be specified in MIL-M-38510, and herein. Epoxy die bonding shall be performed. The resin used shall be DuPont 5504A Conductive Silver Paste which is cured at  $150^{\circ}\text{C} \pm 10^{\circ}\text{C}$  for a minimum of 1 hour plus  $260^{\circ}\text{C} \pm 10^{\circ}\text{C}$  for a minimum of 1 hour, or at  $150^{\circ}\text{C} \pm 10^{\circ}\text{C}$  for a minimum of 1 hour plus  $200^{\circ}\text{C} \pm 10^{\circ}\text{C}$  for a minimum of 2 hours. The use of an alternate epoxy or cure cycle shall be approved by Westinghouse Quality Control.
- 3.2.1 Block Diagram. The block diagram showing essential function with signal and control terminals shall be as specified on Figure 2. The terminal (lead) numbers shall be as specified in Figure 3.
- 3.2.2 Input/Output Protection Circuitry. All transistor gate inputs/outputs (excepting to test structures) shall be protected from transients such as electrostatic discharge by the diode circuit shown in Figure 4. These diode circuits are intrinsic to the part in this specification.

Northrop Corporation Electronics Division Palos Verdes Peninsula, California	SIZE	CODE IDENT NO.		
	A	22915	26760502	
	SCALE	REV	SH	4

- 3.2.3 Truth Tables and Logic Diagrams. The truth tables and typical logic diagrams shall be as specified in Figures 5 and 6.
- 3.2.4 Case Outline. Case outline shall be as specified in 1.4.
- 3.3 Lead Material and Finish. Lead material and finish shall be Alloy 42 with gold plating, 100 microinches, minimum.
- 3.4 Electrical Performance Characteristics. The electrical performance characteristics are as specified in Table I, and apply over the full recommended ambient operating temperature range and radiation environment unless otherwise specified.
- 3.5 Radiation Performance Characteristics. The radiation performance characteristics after exposure to the radiation environments, shall be as specified in a classified document. The radiation environments shall be as specified therein.
- 3.6 Rebonding. Rebonding shall be in accordance with MIL-M-38510.
- 3.7 Electrical Test Requirements. Electrical test requirements shall be as specified in Table II. The Sub-groups of Table III, which constitute the minimum electrical test requirements for screening and quality conformance, are specified in Table II.
- 3.8 Marking. Marking shall be in accordance with MIL-M-38510 except the following marking shall be placed on each microcircuit:
- a) Date Code
  - b) Manufacturer's Identification
  - c) Manufacturer's Part Number (See 6.5)
  - d) Serial Number
- 3.9 Environmental. Devices shall be capable of operating within the specified electrical performance characteristics during and after exposure to the environmental stresses indicated in MIL-STD-883, Method 5005 for Class B devices. Data shall be maintained by the manufacturer on electrically and structurally similar devices (generic family) which demonstrates the continuing ability of the integrated circuits to pass the environmental tests.
- 3.10 Manufacturer Requirements. All testing requirements and product assurance provisions herein, including the requirements of the verification of the specified truth table, shall be satisfied by the manufacturer prior to delivery.

Northrop Corporation Electronics Division Palos Verdes Peninsula, California	SIZE	CODE IDENT NO.		
	A	22915	26760502	
	SCALE	REV	SH	5

4. PRODUCT ASSURANCE PROVISIONS

4.1 Sampling and Inspection. Sampling and inspection procedures shall be in accordance with MIL-M-38510 and Method 5005 of MIL-STD-883, except as modified herein.

4.2 Qualification Inspection. Qualification inspection shall be in accordance with the MX/ACT I Environmental Test Plan, Number 2676-0013.

4.3 Quality Assurance Inspection. Quality assurance screening shall be in accordance with Method 5004 of MIL-STD-883, and shall be conducted on all devices prior to qualification and quality conformance inspection. The following additional criteria shall apply:

- a) Test samples for the group B bond strength test specified in Method 5005 of MIL-STD-883 may, at the manufacturer's option, be randomly selected immediately following the internal visual (precap) inspection and prior to sealing (see 4.4.2(b)).
- b) Temperature cycling (Method 1010 of MIL-STD-883).
  - (1) Omit seal test as post-test measurement.
- c) Thermal shock (Method 1011 of MIL-STD-883), when substituted for temperature cycling.
  - (1) Omit seal test as post-test measurement.
- d) Burn-in test (Method 1015 of MIL-STD-883).
  - (1) Test condition D or E, using the circuit shown on Figure 8 (TBA), or equivalent.
  - (2)  $T_A = 125^\circ\text{C}$  minimum.
- f) Interim and final electrical test parameters shall be as specified in Table II, except interim electrical parameters test prior to burn-in is optional at the discretion of the manufacturer.
- g) External visual inspection shall not include measurement of case and lead dimensions.
- h) Percent defective allowable (PDA) - The PDA is specified as 5 percent for class A devices and 10 percent for class B devices based on failures from group A, subgroup 1 test after cooldown as final electrical test in accordance with Method 5004 of MIL-STD-883, and with no intervening electrical measurements. If interim electrical parameter tests are performed prior to burn-in, failures resulting from pre burn-in screening may be excluded from the PDA. If interim electrical parameter tests prior to burn-in are omitted, then all screening failures shall be included in the PDA. The verified failures of group A, subgroup 1 after burn-in divided by the total number of devices submitted for burn-in in that lot shall be used to determine the percent defective for that lot, and the lot shall be accepted or rejected based on the PDA for the applicable device class.

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4.4 Quality Conformance Inspection. Quality conformance inspection shall be in accordance with MIL-M-38510.

4.4.1 Group A Inspection. Group A inspection shall consist of the test subgroups and LTPD values shown in Table I of Method 5005 of MIL-STD-883 and as follows:

- a) Tests shall be as specified in Table II.
- b) Subgroups 4, 5, 6, 7, and 8 of Table I of Method 5005 of MIL-STD-883 shall be omitted.

4.4.2 Group B Inspection. Group B inspection shall consist of the test subgroups and LTPD values shown in Table II of Method 5005 of MIL-STD-883 and as follows:

- a) End point electrical parameters shall be as specified in Table II.
- b) Bond strength test may be conducted on samples collected prior to sealing (see 4.3(a)).

4.4.3 Group C Inspection. Group C inspection shall consist of the test subgroups and LTPD values shown in Table III of Method 5005 of MIL-STD-883 and as follows:

- a) End point electrical parameters shall be as specified in Table II.
- b) Subgroups 7 and 8 shall be added to the group C inspection requirements for class B devices and shall consist of the tests, conditions and limits specified for subgroups 10 and 11 of group A.
- c) Lead bend in only one direction is required for initial conditioning prior to moisture resistance and salt atmosphere tests.
- d) High temperature storage test (Method 1008 of MIL-STD-883) conditions:
  - (1) Temperature:  $150 \pm 10^{\circ}\text{C}$
  - (2) Duration: 1,000 hours, except as otherwise permitted by Appendix B of MIL-M-38510.
- e) Operating life test (Method 1005 of MIL-STD-883) conditions:
  - (1) Test condition D or E, using the circuit shown on Figure 8, or equivalent.
  - (2)  $T_A = 125^{\circ}\text{C}$ , minimum.
  - (3) Test duration: 1,000 hours, except as permitted by Appendix B of MIL-M-38510.
  - (4) Devices selected for testing, shall be programmed prior to commencing the test to the specified Truth Table as shown on Figure 5.
- f) Radiation test
  - (1) Bias per Figures 9A, 9B or 9C.

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4.5 Methods of Examination and Test. Methods of examination and test shall be as specified in Table II and as follows:

4.5.1 Voltage and Current. All voltages given are referenced to the micro-circuit  $V_{SS}$  terminal, unless otherwise specified. Currents given are conventional current and positive when flowing into the referenced terminal.

4.5.2 Dynamic Burn-in and Operating Life Tests. Dynamic burn-in and operating life tests shall be performed with the devices connected as specified in Table IV. When devices are measured at 25°C following these tests, they shall be cooled to room temperature prior to removal of the bias voltage.

4.5.3 Input Capacitance ( $C_i$ ) Tests. The input capacitance shall be measured using a capacitance bridge connected between the specified measurement terminal and the  $V_{SS}$  terminal. The measurement frequency shall be within the range of 100 kHz to 1.0 MHz.  $V_{dd}$  shall be tied to  $V_{SS}$ .

4.5.4 Quiescent Supply Current Measurements. When performing quiescent supply current measurements the meter shall be placed so that all current flows through the meter.

4.6 Data Reporting. When specified in the contract or order, a copy of the following data, as applicable, shall be supplied:

- a) Attributes and variables data for all dynamic burn-in and operating life tests (see 3.5 and 4.2).
- b) The quality assurance inspection data.
- c) Parameter distribution data.
- d) Final electrical parameters data (see 3.5).

4.7 Inspection of Preparation for Delivery. Inspection of preparation for delivery shall be in accordance with MIL-M-38510A, except that the rough handling test shall not apply.

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5. PREPARATION FOR DELIVERY

5.1 Preservation-Packaging and Packing. Microcircuits shall be prepared for delivery in accordance with good commercial practice. In addition, each part shall be in contact with a conductive material which shorts all leads together to prevent electrostatic damage.

6. NOTES

6.1 Notes. The notes specified in MIL-M-38510A are applicable to this specification.

6.2 Intended Use. Microcircuits conforming to this specification are intended for use in an advanced technology computer breadboard.

6.3 Ordering Data. The contract or order should specify the following:

- a) Complete part number (see 1.2).
- b) Requirements for delivery of one copy of the data (see 4.4) pertinent to the device inspection lot to be supplied with each shipment by the device manufacturer, if applicable.
- c) Requirement for certificate of compliance, if applicable.
- d) Requirement for notification of change of product or process to procuring activity in addition to notification to qualifying activity, if applicable.
- e) Requirements for packaging and packing (see 5.1). Appropriate level of MIL-M-55565 must be specified.
- f) Requirements for failure analysis (including required test condition of Method 5003), corrective action and reporting of results, if applicable.
- g) Requirements for product assurance screen.
- h) Requirements for carriers, special lead lengths or lead forming, if applicable.

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6.4 Abbreviations, Symbols, and Definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-STD-1313, MIL-STD-1331 and as follows:

$C_1$ -----Input terminal-to- $V_{SS}$  capacitance.

GND-----Ground. Zero voltage potential.

$T_A$ -----Free air temperature.

$t_f$  or  $t_{THL}$ -----Fall time. Time duration during which the amplitude of the trailing edge of the input forcing condition of waveform is decreasing from 90 to 10 percent of the maximum.

$t_f$  or  $t_{TLH}$ -----Rise time. Time duration during which the amplitude of the leading edge of the input forcing condition or waveform is increasing from 10 to 90 percent of the maximum amplitude.

$V_{DD}$ -----Positive supply voltage.

$V_{SS}$ -----Negative supply voltage.

$I_{SS}$  or  $I_{DD}$ -----Quiescent supply current.

$\overline{EN}$ -----Deselect waveform.

$\overline{CS}$ -----Chip output select waveform.

$\overline{DR}$ -----Data Ready output, used as  $\overline{EN}$  for second level of ROMs.

$A_i$ -----Address inputs.

$D_{\phi i}$ -----Data, Output

6.5 Substitutability. Microcircuits covered by this specification are not substitutable for any commercial device type.

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TABLE I ELECTRICAL PERFORMANCE CHARACTERISTICS

TEST	SYMBOL	CONDITIONS	LIMITS		UNITS
			MIN	MAX	
Input Protect Diode					
Source	$V_{ILD}$	$V_{DD} = 13Vdc, V_{SS} = 0Vdc$ See Note 3, Table III			
Sink	$V_{IHD}$	$I_{IN} = -9mA, T_A = 25^\circ C$ $I_{IN} = +9mA, T_A = 25^\circ C$ pulse < 50ms, < 1% duty cycle	--	-10.8 23.8	Vdc Vdc
Input Current					
Low Level	$I_{IL}$	$V_{DD} = 13Vdc, V_{SS} = 0Vdc$ See Note 3, Table III			
High Level	$I_{IH}$	$V_{IN} = 0Vdc$ $V_{IN} = 13Vdc$	--	1.0 1.0	$\mu A dc$ $\mu A dc$
Low Level Output Voltage					
Outputs 0	$V_{OL}$	$V_{DD} = 10Vdc, V_{SS} = 0Vdc,$ $\overline{CS} = \overline{EN0} = 1.2Vdc$ $D00 - D03 = 0Vdc, \overline{DR} = 0Vdc$ See notes 5 and 9, Table III			
Outputs 0	$V_{OLS}$	$A_0 - A_5 = 10Vdc, A_6 - A_7 = 0Vdc$ $I_O = 0$ $I_O = +10mA dc$	--	0.6 2.0	Vdc Vdc

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TABLE I ELECTRICAL PERFORMANCE CHARACTERISTICS (CONTINUED)

TEST	SYMBOL	CONDITIONS	LIMITS		UNITS
			MIN	MAX	
High Level Output Voltage		$V_{DD} = 10\text{Vdc}$ , $V_{SS} = 0\text{Vdc}$ $\overline{CS} = \overline{EN0} = 1.2\text{V}$ , $D00-D03 = 10\text{Vdc}$ , $DR = 12\text{Vdc}$ See Notes 5 and 9, Table III $A_0 - A_4 = 10\text{Vdc}$ , $A_5 - A_7 = 0\text{Vdc}$ $I_O = 0$ $I_O = -10\text{mAdc}$			
Outputs one	$V_{OH}$		--	9.4	Vdc
Outputs one	$V_{OHS}$		--	8.0	Vdc
Output Leakage Current		$V_{DD} = 13\text{Vdc}$ , $V_{SS} = 0\text{Vdc}$ $\overline{CS} = 11.8\text{Vdc}$ , See Note 4, Table III $V_{OUT} = 0\text{Vdc}$ $V_{OUT} = 13\text{Vdc}$			
Outputs Low	$I_{OLZM}$		--	15.0	$\mu\text{Adc}$
Outputs High	$I_{OHZM}$		--	30.0	$\mu\text{Adc}$
Output Short Circuit Current		$V_{DD} = 8\text{Vdc}$ , $V_{SS} = 0\text{Vdc}$ See Notes 2, 4 and 9, Table III $A_0 - A_5 = 10\text{Vdc}$ , $A_6 - A_7 = 0\text{Vdc}$ $V_{OUT} = 8\text{Vdc}$ , $t \leq 30\text{msec}$ $A_0 - A_4 = 10\text{Vdc}$ , $A_5 - A_7 = 0\text{Vdc}$ $V_{OUT} = 0\text{Vdc}$ , $t \leq 30\text{msec}$			
Output High	$I_{OLS}$		12		mAdc
Output Low	$I_{OHS}$		--	-12	mAdc

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TABLE I ELECTRICAL PERFORMANCE CHARACTERISTICS (CONTINUED)

TEST	SYMBOL	CONDITIONS	LIMITS		UNITS
			MIN	MAX	
Supply Surge Current		$V_{SS} = 0Vdc$ See Notes 2, 4 and 9, Table III			
Chip Select High, Low Current	$V_{DDMD1}$	$\overline{CS} = 13.8Vdc, I_{DD} = 100\mu A$	15		Vdc
Chip Select High, High Current	$V_{DDMD2}$	$\overline{CS} = 13.8Vdc, I_{DD} = 1.0mA$	15		Vdc
Chip Select Low, Low Current	$V_{DDMS1}$	$\overline{CS} = 1.2Vdc, I_{DD} = 100\mu A$	15		Vdc
Chip Select Low, High Current	$V_{DDMS2}$	$\overline{CS} = 1.2Vdc, I_{DD} = 1.0mA$	15		Vdc
Supply Current, Quiescent State (input currents excluded)		$V_{SS} = 0Vdc$ See Note 3, 5 and 10, Table III			
Inputs Low, Deselected	$I_{DDL1}$	$V_{DD} = 10Vdc, \overline{CS} = 8.8Vdc, V_{IN} = 1.2Vdc$		0.5	$\mu A$
Inputs High, Deselected	$I_{DDH1}$	$V_{DD} = 10Vdc, \overline{CS} = 8.8Vdc, V_{IN} = 8.8Vdc$		0.5	$\mu A$
Inputs Low, Deselected	$I_{DDL2}$	$V_{DD} = 13Vdc, \overline{CS} = 11.2Vdc, V_{IN} = 1.2Vdc$		0.7	$\mu A$
Inputs High, Deselected	$I_{DDH2}$	$V_{DD} = 13Vdc, \overline{CS} = 11.2Vdc, V_{IN} = 11.2Vdc$		0.7	$\mu A$
Inputs High, Selected	$I_{DDL3}$	$V_{DD} = 10Vdc, \overline{CS} = 1.2Vdc, V_{IN} = 10Vdc$		0.8	$\mu A$
Inputs High, Selected	$I_{DDH3}$	$V_{DD} = 10Vdc, \overline{CS} = 1.2Vdc, V_{IN} = 10Vdc$		0.8	$\mu A$
Inputs High, Selected	$I_{DDL4}$	$V_{DD} = 13Vdc, \overline{CS} = 1.2Vdc, V_{IN} = 13Vdc$		1.1	$\mu A$
Inputs High, Selected	$I_{DDH4}$	$V_{DD} = 13Vdc, \overline{CS} = 1.2Vdc, V_{IN} = 13Vdc$		1.1	$\mu A$

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TABLE I ELECTRICAL PERFORMANCE CHARACTERISTICS (CONTINUED)

TEST	SYMBOL	CONDITIONS	LIMITS		UNITS
			MIN	MAX	
Dynamic Supply Current		$V_{SS} = 0Vdc$			
Selected, Zero/One Pattern		$\overline{CS} = \overline{EN1} = 1.2Vdc$			
		Clock $\overline{EN0}$ , Address = 50			
		See Notes 5 and 6, Table III			
		$t_{cycle} = 500nsec$			
	$I_{DD}$	$V_{DD} = 10Vdc$		5.0	mAdc
	$I_{DD}$	$V_{DD} = 13Vdc$		10.0	mAdc
Input Capacitance	$C_{IN}$	$V_{DD} = 0Vdc, f = 1MHz$		7	pf
	$C_{IN}$	$\overline{EN0}, \overline{EN1}, A_0 - A_4$		5	pf
	$C_{IN}$	$A_5 - A_7$ $\overline{CS}$		6	pf
Output Capacitance	$C_{OUT}$	$V_{DD} = 0Vdc, f = 1MHz$ D00 - D03		5	pf

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TABLE I ELECTRICAL PERFORMANCE CHARACTERISTICS (CONTINUED)

TEST	SYMBOL	CONDITIONS	LIMITS		UNITS
			MIN	MAX	
Dynamic Characteristics		$V_{DD} = 10V_{dc}$ , $V_{SS} = 0V_{dc}$ , $\overline{CS} = 0V_{dc}$			
Data Delay Time	$t_{ACC_{LH}}$	See Notes 6, 7 and 8, Table III		148	nsec
Data Delay Time	$t_{ACC_{HL}}$	See Notes 6, 7 and 8, Table III		148	nsec
Data Ready Delay Time	$t_{DR}$	See Notes 6, 7 and 8, Table III		166	nsec
Transition Delay Time	$t_{TLH}$	Address 3F to 1F, $C_{LOAD} = 15pf$		20	nsec
	$t_{THL}$	Address 1F to 3F, $C_{LOAD} = 15pf$		20	nsec
Chip Select Delay Time	$t_{CSD}$	$t_{cycle} = 250ns$ , $t_{ED} = 40ns$ , $t_{AS} = 40ns$ , $t_{CS} = 150ns$ , address = 50, See Note 7, Table III		60	nsec

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TABLE II ELECT. AL TEST REQUIREMENTS

MIL-STD-883 TEST REQUIREMENT	TEST REQUIREMENTS (SUBGROUPS OF TABLE III)
Interim electrical parameters (Pre Burn-in) (Method 5004)	1, 7
Final electrical test parameters (Method 5004)	1, 2, 3, 7, 9
Group A test requirements (Method 5005)	1, 2, 3, 7, 8, 9
Groups B and C end point electrical parameters (Method 5005) (Environmental tests)	1, 2, 3, 7, 8, 9
Additional electrical subgroups for Group C periodic inspections	10

INDEX TO TABLE III SUBGROUPS FOR REFERENCE

Subgroup	Type of Tests	Temp
1	Static	25C
2	Static	+25C
3	Static	-55C
7	Truth Table	25C
8	Truth Table	+125C & -55C
9	Dynamic	25C
10	Dynamic	25C

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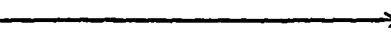


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TABLE III. GROUP A INSPECTION

Subgroup 1 -  $T_A = 25^\circ\text{C}$ 

Terminal Conditions (Terminals not designated are open)

SYM- BOL	MIL STD-883 METHOD	TEST NO.	INPUT CONDITIONS				MEASURED TERMINAL	TEST LIMITS		
			SPECIFIC		GENERAL	L-F/N		PIN #	MIN.	MAX. UNIT
			L-F/N	PIN #						
$ V_{ILD} $ (Source)  $ V_{ILD} $	--	1	A <sub>0</sub>	39	-9.0mA	V <sub>DD</sub> =13Vdc (Pin 14) V <sub>SS</sub> =0V (Pin 28) See Note 3	A <sub>0</sub>	39	-10.8	V
		2	A <sub>1</sub>	38		A <sub>1</sub>	38		V	
		3	A <sub>2</sub>	35		A <sub>2</sub>	35			
		4	A <sub>3</sub>	34		A <sub>3</sub>	34			
		5	A <sub>4</sub>	33		A <sub>4</sub>	33			
		6	A <sub>5</sub>	1		A <sub>5</sub>	1			
		7	A <sub>6</sub>	2		A <sub>6</sub>	2			
		8	A <sub>7</sub>	7		A <sub>7</sub>	7			
		9	$\overline{\text{EN0}}$	31		$\overline{\text{EN0}}$	31			
		10	$\overline{\text{EN1}}$	32		$\overline{\text{EN1}}$	32			
		11	$\overline{\text{CS}}$	27		$\overline{\text{CS}}$	27			
$V_{IHD}$ (Sink)  $V_{IHD}$	--	12	A <sub>0</sub>	39	+9.0mA	V <sub>DD</sub> =13Vdc (Pin 14) V <sub>SS</sub> =0V (Pin 28)	A <sub>0</sub>	39	23.8	V
		13	A <sub>1</sub>	38		A <sub>1</sub>	38		V	
		14	A <sub>2</sub>	35		A <sub>2</sub>	35			
		15	A <sub>3</sub>	34		A <sub>3</sub>	34			
		16	A <sub>4</sub>	33		A <sub>4</sub>	33			
		17	A <sub>5</sub>	1		A <sub>5</sub>	1			
		18	A <sub>6</sub>	2		A <sub>6</sub>	2			
		19	A <sub>7</sub>	7		A <sub>7</sub>	7			
		20	$\overline{\text{EN0}}$	31		$\overline{\text{EN0}}$	31			
		21	$\overline{\text{EN1}}$	32		$\overline{\text{EN1}}$	32			
		22	$\overline{\text{CS}}$	27		$\overline{\text{CS}}$	27			

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TABLE III GROUP A INSPECTION

Subgroup 1 -  $T_A = 25^\circ\text{C}$ 

Terminal Conditions (Terminals not designated are open)

SYM-BOL	MIL STD-883 METHOD	TEST NO.	INPUT CONDITIONS		MEASURED TERMINAL L-F/N	TEST LIMITS	
			SPECIFIC PIN #	GENERAL CONDITIONS		MIN.	MAX. UNIT
$I_{IL}$		23	A <sub>0</sub> 39	$V_{DD} = 13\text{Vdc}$	A <sub>0</sub> 39		1.0 $\mu\text{A}$
		24	A <sub>1</sub> 38	(Pin 14)	A <sub>1</sub> 38		
		25	A <sub>2</sub> 35	$V_{SS} = 0\text{V}$	A <sub>2</sub> 35		
		26	A <sub>3</sub> 34	(Pin 28)	A <sub>3</sub> 34		
		27	A <sub>4</sub> 33		A <sub>4</sub> 33		
		28	A <sub>5</sub> 1		A <sub>5</sub> 1		
		29	A <sub>6</sub> 2		A <sub>6</sub> 2		
		30	A <sub>7</sub> 7		A <sub>7</sub> 7		
		31	$\overline{\text{EN0}}$ 31		$\overline{\text{EN0}}$ 31		
		32	$\overline{\text{EN1}}$ 32		$\overline{\text{EN1}}$ 32		
		33	$\overline{\text{CS}}$ 27		$\overline{\text{CS}}$ 27		
				OV $\rightarrow$ OV			
				1.2V			
$ I_{IH} $		34	A <sub>0</sub> 39	$V_{DD} = 13\text{Vdc}$	A <sub>0</sub> 39		1.0 $\mu\text{A}$
		35	A <sub>1</sub> 38	(Pin 14)	A <sub>1</sub> 38		
		36	A <sub>2</sub> 35	$V_{SS} = 0\text{V}$	A <sub>2</sub> 35		
		37	A <sub>3</sub> 34	(Pin 28)	A <sub>3</sub> 34		
		38	A <sub>4</sub> 33		A <sub>4</sub> 33		
		39	A <sub>5</sub> 1		A <sub>5</sub> 1		
		40	A <sub>6</sub> 2		A <sub>6</sub> 2		
		41	A <sub>7</sub> 7		A <sub>7</sub> 7		
		42	$\overline{\text{EN0}}$ 31		$\overline{\text{EN0}}$ 31		
		43	$\overline{\text{EN1}}$ 32		$\overline{\text{EN1}}$ 32		
		44	$\overline{\text{CS}}$ 27		$\overline{\text{CS}}$ 27		
				13Vdc $\rightarrow$ 13Vdc			

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TABLE III GROUP A INSPECTION

Subgroup 1 -  $T_A = 25^\circ\text{C}$ 

Terminal Conditions (Terminals not designated are open)

SYM-BOL	MIL STD-883 METHOD	TEST NO.	INPUT CONDITIONS			MEASURED TERMINAL L-F/N	PIN #	TEST LIMITS		
			L-F/N	SPECIFIC PIN #	GENERAL CONDITIONS			MIN.	MAX.	UNIT
$V_{OL}$  $V_{OL}$		45	A <sub>0</sub> -A <sub>5</sub>	Fig 2	12Vdc	DØ0	8	--	0.6	Vdc
		46	A <sub>6</sub> -A <sub>7</sub>	"	0Vdc					
			A <sub>0</sub> -A <sub>5</sub>	"	12Vdc	DØ1	12	--		
			A <sub>6</sub> -A <sub>7</sub>	"	0Vdc					
		47	A <sub>0</sub> -A <sub>5</sub>	"	12Vdc	DØ2	13	--		
			A <sub>6</sub> -A <sub>7</sub>	"	0Vdc					
		48	A <sub>0</sub> -A <sub>5</sub>	"	12Vdc	DØ3	25	--		
			A <sub>6</sub> -A <sub>7</sub>	"	0Vdc					
		49	A <sub>0</sub> -A <sub>5</sub>	"	12Vdc	$\overline{DR}$	26	--		
			A <sub>6</sub> -A <sub>7</sub>	"	0Vdc				0.6	Vdc
$V_{OLS}$  $V_{OLS}$		50	A <sub>0</sub> -A <sub>5</sub>	"	12Vdc	DØ0	8	--	2.0	Vdc
		51	A <sub>6</sub> -A <sub>7</sub>	"	0Vdc					
			A <sub>0</sub> -A <sub>5</sub>	"	12Vdc	DØ1	12	--		
			A <sub>6</sub> -A <sub>7</sub>	"	0Vdc					
		52	A <sub>0</sub> -A <sub>5</sub>	"	12Vdc	DØ2	13	--		
			A <sub>6</sub> -A <sub>7</sub>	"	0Vdc					
		53	A <sub>0</sub> -A <sub>5</sub>	"	12Vdc	DØ3	25	--		
			A <sub>6</sub> -A <sub>7</sub>	"	0Vdc					
		54	A <sub>0</sub> -A <sub>5</sub>	"	12Vdc	$\overline{DR}$	26	--	2.0	Vdc
			A <sub>6</sub> -A <sub>7</sub>	"	0Vdc					

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TABLE III. GROUP A INSPECTION

Subgroup 1 -  $T_A = 25^\circ\text{C}$ 

Terminal Conditions (Terminals not designated are open)

SYM-BOL	MIL STD-883 METHOD	TEST NO.	INPUT CONDITIONS				MEASURED TERMINAL	TEST LIMITS						
			SPECIFIC		GENERAL	L-F/N		PIN #	L-F/N	PIN #	MIN.	MAX.	UNIT	
			L-F/N	PIN #										CONDITIONS
$V_{OH}$  $V_{OH}$		55	A <sub>0</sub> -A <sub>4</sub>	Fig 2	12Vdc	$V_{DD}=10Vdc$	DØ0	8	--	9.4	Vdc			
			A <sub>5</sub> -A <sub>7</sub>	"	0Vdc	$V_{SS}=0V$								
	56	A <sub>0</sub> -A <sub>4</sub>	"	12Vdc	$\overline{CS} = 1.2V$	DØ1	12	--	9.4	Vdc				
		A <sub>5</sub> -A <sub>7</sub>	"	0Vdc	$\overline{EN0} = 1.2V$									
	57	A <sub>0</sub> -A <sub>4</sub>	"	12Vdc	DØ0 thru	DØ2	13	--	9.4	Vdc				
$V_{OH}$			A <sub>5</sub> -A <sub>7</sub>	"	0Vdc	DØ3 = 8.8V								
	58	A <sub>0</sub> -A <sub>4</sub>	"	12Vdc	$I_O = 0$	DØ3	25	--	9.4	Vdc				
		A <sub>5</sub> -A <sub>7</sub>	"	0Vdc	See notes 5 and 9									
	59	A <sub>0</sub> -A <sub>4</sub>	"	12Vdc	$V_{DD}=10Vdc$	DØ0	8	--	8.0	Vdc				
	60	A <sub>5</sub> -A <sub>7</sub>	"	0Vdc	$V_{SS} = 0V$									
$V_{OHS}$  $V_{OHS}$			A <sub>0</sub> -A <sub>4</sub>	"	12Vdc	$\overline{CS} = 1.2V$	DØ1	12	--	8.0	Vdc			
			A <sub>5</sub> -A <sub>7</sub>	"	0Vdc	$\overline{EN0} = 1.2V$								
	61	A <sub>0</sub> -A <sub>4</sub>	"	12Vdc	DØ0 thru	DØ2	13	--	8.0	Vdc				
		A <sub>5</sub> -A <sub>7</sub>	"	0Vdc	DØ3 = 8.8V									
	62	A <sub>0</sub> -A <sub>4</sub>	"	12Vdc	$I_O = -10mA$	DØ3	25	--	8.0	Vdc				
			A <sub>5</sub> -A <sub>7</sub>	"	0Vdc	See notes 5 and 9								

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TABLE III GROUP A INSPECTION

Subgroup 1 -  $T_A = 25^\circ\text{C}$ 

Terminal Conditions (Terminals not designated are open)

SYM-BOL	MIL STD-883 METHOD	TEST NO.	INPUT CONDITIONS			MEASURED TERMINAL	TEST LIMITS		
			L-F/N	SPECIFIC PIN #	GENERAL CONDITIONS		L-F/N	PIN #	MIN. MAX. UNIT
$I_{OLZM}$ → $I_{OLZM}$		63	DØ0	8	OV	DØ0		8	-- 15.0 $\mu\text{A}$ dc
		64	DØ1	12		DØ1		12	-- --
		65	DØ2	13		DØ2		13	-- --
		66	DØ3	25		DØ3		25	-- --
		67	DR	36	OV	DR		36	-- 15.0 $\mu\text{A}$ dc
$I_{OHZM}$ → $I_{OHZM}$		68	DØ0	8	13Vdc	DØ0		8	-- 30.0 $\mu\text{A}$ dc
		69	DØ1	12		DØ1		12	-- --
		70	DØ2	13		DØ2		13	-- --
		71	DØ3	25	13Vdc	DØ3		25	-- 30.0 $\mu\text{A}$ dc

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TABLE III GROUP A INSPECTION

Subgroup 1 -  $T_A = 25^\circ\text{C}$ 

Terminal Conditions (Terminals not designated are open)

SYN- BOL	MIL STD-883 METHOD	TEST NO.	INPUT CONDITIONS			MEASURED TERMINAL		TEST LIMITS	
			SPECIFIC		GENERAL	L-F/N	PIN #	MIN.	MAX. UNIT
			L-F/N	PIN #					
$I_{OLS}$ →		72	A <sub>0</sub> -A <sub>5</sub> A <sub>6</sub> -A <sub>7</sub> DØ0	Fig 2 " 8	12Vdc 0Vdc 8Vdc	V <sub>DD</sub> = 8Vdc (Pin 14) V <sub>SS</sub> = 0V (Pin 28)	DØ0	8	12
		73	A <sub>0</sub> -A <sub>5</sub> A <sub>6</sub> -A <sub>7</sub> DØ1	Fig 2 " 12	12Vdc 0Vdc 8Vdc	See notes 2, 4 and 9	DØ1	12	12
		74	A <sub>0</sub> -A <sub>5</sub> A <sub>6</sub> -A <sub>7</sub> DØ2	Fig 2 " 13	12Vdc 0Vdc 8Vdc	$t \leq 30\text{msec}$	DØ2	13	12
		75	A <sub>0</sub> -A <sub>5</sub> A <sub>6</sub> -A <sub>7</sub> DØ3	Fig 2 " 25	12Vdc 0Vdc 8Vdc		DØ3	25	12
		76	A <sub>0</sub> -A <sub>5</sub> A <sub>6</sub> -A <sub>7</sub> DØ4	Fig 2 " 36	12Vdc 0Vdc 8Vdc		DØ4	36	12
									mAdc

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TABLE III GROUP A INSPECTION

Subgroup 1 -  $T_A = 25^\circ\text{C}$ 

Terminal Conditions (Terminals not designated are open)

SYM- NOL	MIL STD-883 METHOD	TEST NO.	INPUT CONDITIONS		MEASURED TERMINAL	TEST LIMITS	
			L-F/N	SPECIFIC PIN #		L-F/N	UNIT
$I_{OHS}$		77	A <sub>0</sub> -A <sub>4</sub>	Fig 2	DØ0	8	mAdc
			A <sub>5</sub> -A <sub>7</sub>	"			
			DØ0	8			
		78	A <sub>0</sub> -A <sub>4</sub>	Fig 2	DØ1	12	mAdc
			A <sub>5</sub> -A <sub>7</sub>	"			
			DØ1	12			
		79	A <sub>0</sub> -A <sub>4</sub>	Fig 2	DØ2	13	mAdc
			A <sub>5</sub> -A <sub>7</sub>	"			
			DØ2	13			
		80	A <sub>0</sub> -A <sub>4</sub>	Fig 2	DØ3	25	mAdc
			A <sub>5</sub> -A <sub>7</sub>	"			
			DØ3	25			

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TABLE III GROUP A INSPECTION

Subgroup 1 -  $T_A = 25^\circ\text{C}$ 

Terminal Conditions (Terminals not designated are open)

SYM- BOL	MIL STD-883 METHOD	TEST NO.	INPUT CONDITIONS		MEASURED TERMINAL	TEST LIMITS	
			L-F/N	SPECIFIC PIN #		L-F/N	UNIT
$V_{DDMD1}$	--	81	$V_{DD}$	14	$I_{DD} = 100\mu\text{A}$	$V_{SS} = 0\text{Vdc}$ (Pin 28) $\overline{CS} = 13.8\text{Vdc}$ (Pin 27)	$V_{DD}$
$V_{DDMD2}$		82	$V_{DD}$	14	$I_{DD} = 1.0\text{mA}$		$V_{DD}$
$V_{DDMS1}$		83	$V_{DD}$	14	$I_{DD} = 100\mu\text{A}$	$V_{SS} = 0\text{Vdc}$ (Pin 28) $\overline{CS} = 1.2\text{Vdc}$ Clock $\overline{EN0}$ See note 5 Address=50	$V_{DD}$
$V_{DDMS2}$		84	$V_{DD}$	14	$I_{DD} = 1.0\text{mA}$		$V_{DD}$

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TABLE III GROUP A INSPECTION

Subgroup 1 -  $T_A = 25^\circ\text{C}$ 

Terminal Conditions (Terminals not designated are open)

SYM- BOL	MIL STD-883 METHOD	TEST NO.	INPUT CONDITIONS				MEASURED TERMINAL		TEST LIMITS			
			SPECIFIC		GENFRAI	L-F/N	PIN #	L-F/N	PIN #	MIN.	MAX.	UNIT
			L-F/N	PIN #								
I <sub>DDL1</sub>		85	A <sub>0</sub> -A <sub>7</sub>	Fig 2	1.2Vdc	V <sub>DD</sub> = 10Vdc (Pin 14) V <sub>SS</sub> = 0Vdc (Pin 28) CS = 8.8Vdc See note 10	I <sub>DD</sub>	14		0.5	μAdc	
			EN0	31	1.2Vdc							
			EN1	32	1.2Vdc							
I <sub>DDH1</sub>		86	A <sub>0</sub> -A <sub>7</sub>	Fig 2	8.8Vdc		I <sub>DD</sub>	14		0.5	μAdc	
			EN0	31	8.8Vdc							
			EN1	32	8.8Vdc							
I <sub>DDL2</sub>		87	A <sub>0</sub> -A <sub>7</sub>	Fig 2	1.2Vdc	V <sub>DD</sub> = 13Vdc (Pin 14) V <sub>SS</sub> = 0Vdc (Pin 28) CS = 11.2Vdc See note 10	I <sub>DD</sub>	14		0.7	μAdc	
			EN0	31	1.2Vdc							
			EN1	32	1.2Vdc							
I <sub>DDH2</sub>		88	CS1	27	1.2Vdc		I <sub>DD</sub>	14		0.7	μAdc	
			A <sub>0</sub> -A <sub>7</sub>	Fig 2	11.2Vdc							
			EN0	31	11.2Vdc							
			EN1	32	11.2Vdc							
			CS1	27	112.Vdc							

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TABLE III. GROUP A INSPECTION

Subgroup 1 -  $T_A = 25^\circ\text{C}$ 

Terminal Conditions (Terminals not designated are open)

SYM- BOL	MIL STD-883 METHOD	TEST NO.	INPUT CONDITIONS			MEASURED TERMINAL	TEST LIMITS	
			L-F/N	SPECIFIC PIN #	GENERAL CONDITIONS		L-F/N	UNIT
$I_{DDL3}$		89	$A_0-A_7$	Fig 2	10Vdc	$I_{DD}$	14	0.8 $\mu\text{A}$ dc
			$\overline{EN0}$	31	10Vdc.			
			$\overline{EN1}$	32	10Vdc			
$I_{DDH3}$		90	$A_0-A_7$	Fig 2	10Vdc	$I_{DD}$	14	0.8 $\mu\text{A}$ dc
			$\overline{EN0}$	31	10Vdc			
			$\overline{EN1}$	32	10Vdc			

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TABLE III GROUP A INSPECTION

Subgroup 1 -  $T_A = 25^\circ\text{C}$   
Terminal Conditions (Terminals not designated are open)

SYM- BOL	MIL STD-883 METHOD	TEST NO.	INPUT CONDITIONS		MEASURED TERMINAL	TEST LIMITS	
			L-F/N	SPECIFIC PIN #		MIN.	MAX. UNIT
$I_{DDL4}$		91	$A_0-A_7$	Fig 2	$V_{DD}=13\text{Vdc}$ (Pin 14) $V_{SS}=0\text{Vdc}$ (Pin 28) $\overline{CS}=1.2\text{Vdc}$ Clock $\overline{EN0}$ See note 5 Address=50		1.1 $\mu\text{A dc}$
			$\overline{EN0}$	31			
			$\overline{EN1}$	32			
$I_{DDH4}$		92	$A_0-A_7$	Fig 2	$V_{DD}=13\text{Vdc}$ (Pin 14) $V_{SS}=0\text{Vdc}$ (Pin 28) $\overline{CS}=1.2\text{Vdc}$ Clock $\overline{EN0}$ See note 5 Address=50		1.1 $\mu\text{A dc}$
			$\overline{EN0}$	31			
			$\overline{EN1}$	32			

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TABLE III GROUP A INSPECTION

Subgroup 1 -  $T_A = 25^\circ\text{C}$ 

Terminal Conditions (Terminals not designated are open)

SYM- BOL	MIL STD-883 METHOD	TEST NO.	INPUT CONDITIONS		MEASURED TERMINAL	TEST LIMITS	
			L-F/N	SPECIFIC PIN #		L-F/N	UNIT
$I_{DD1}$		93	$V_{DD}$	14	10Vdc	$I_{DD}$	mAdc
$I_{DD2}$		94	$V_{DD}$	14	13Vdc	$I_{DD}$	mAdc
					$V_{SS} = 0\text{Vdc}$ $\overline{CS} = 1.2\text{Vdc}$ $\overline{EN1} = 1.2\text{Vdc}$ $t_{\text{cycle}} = 500\text{nsec}$ See notes 5 and 6 Clock $\overline{EN0}$ Address=50		

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TABLE III GROUP A INSPECTION

Subgroup 2 -  $T_A = +125^\circ\text{C}$  1/

Same tests, Terminal Conditions and Limits as for Subgroup 1 except  $V_{ILD}$ ,  $V_{IHD}$  tests are omitted.

Subgroup 3 -  $T_A = -55^\circ\text{C}$  1/

Same tests, Terminal Conditions and Limits as for Subgroup 1 except  $V_{ILD}$ ,  $V_{IHD}$  tests are omitted.

Subgroup 7 -  $T_A = 25^\circ\text{C}$

Truth table tests for Programmed Devices (see Figure 5).

Test No. 95 - 351

General Inputs:

$V_{DD} = 10\text{Vdc}$

$V_{SS} = 0\text{Vdc}$

Specific Inputs:

The address inputs (A0 through A7) and the Data outputs (D00 through D03) shall be per the applicable truth table of the specific programmed device under test.

Subgroup 8 -

Test No. 351 - 607

Repeat Subgroup 7 at  $T_A = +125^\circ\text{C}$

Test No. 607 - 863

Repeat Subgroup 7 at  $T_A = -55^\circ\text{C}$

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TABLE III GROUP A INSPECTION

Subgroup 9 -  $T_A = 25^\circ\text{C}$ 

Terminal Conditions (Terminals not designated are open)

SYM-BOL	MIL STD-883 METHOD	TEST NO.	INPUT CONDITIONS				MEASURED TERMINAL	TEST LIMITS				
			SPECIFIC			GENERAL		L-F/N	PIN #	MIN.	MAX.	UNIT
			L-F/N	PIN #	CONDITIONS							
$t_{ACC_{LH}}$		864	Address	Fig 2	Switch from 0 to 1	$V_D = 10Vdc$ $V_{SS} = 0Vdc$ $CS = 0V$ $t_{cycle} = 250ns$	D00	8	--	148	nsec	
		865	$A_0-A_7$					D01	12	--	148	nsec
		866	See notes					D02	13	--	148	nsec
		867	6,7,&8					D03	25	--	148	nsec
		$t_{ACC_{HL}}$		868	Address	Fig 2	Switch from 1 to 0	$t_{ED} = 40ns$ $t_{AS} = 40ns$	D00	8	--	148
869	$A_0-A_7$							D01	12	--	148	nsec
870	See notes							D02	13	--	148	nsec
871	6,7,&8							D03	25	--	148	nsec
$t_{DR}$		872	Address	Fig 2		$V_{DD} = 10Vdc$ $V_{SS} = 0Vdc$ $CS = 0V$ $t_{cycle} = 250ns$ $t_{ED} = 40ns$ $t_{AS} = 40ns$	DR	26		166	nsec	
			$A_0-A_7$									
			See notes									
			6,7,&8									

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TABLE III GROUP A INSPECTION

Subgroup 9 -  $T_A = 25^\circ\text{C}$ 

Terminal Conditions (Terminals not designated are open)

SYM-BOL	MIL STD-883 METHOD	TEST NO.	INPUT CONDITIONS			MEASURED TERMINAL	TEST LIMITS		
			L-F/N	PIN #	GENFRAI		L-F/N	PIN #	MIN. MAX. UNIT
$t_{TLH}$		873	A <sub>0</sub> -A <sub>7</sub>	Fig 2	Address 3F to 1F See notes 6, 7, 8, and 10	$V_{DD} = 10\text{Vdc}$ $V_{SS} = 0\text{Vdc}$ $CS = 0\text{Vdc}$ Pulse EN $C_l = 15\text{pf}$	D00		20 nsec
		874							
		875							
		876							
		877							
		878	A <sub>0</sub> -A <sub>7</sub>	Fig 2	Address 1F to 3F		D00		20 nsec
		879							
		880							
		881					D01		
		882							
$t_{CSD}$		883	A <sub>0</sub> -A <sub>7</sub>	Fig 2	Address 3F	$V_{DD} = 10\text{Vdc}$ $V_{SS} = 0\text{Vdc}$ $t_{\text{cycle}} = 250\text{ns}$ $t_{ED} = 40\text{ns}$ $t_{AS} = 40\text{ns}$ $t_{CS} = 150\text{ns}$ $t_{CSW} = 100\text{ns}$	D00	8	60 nsec
		884							
		885							
		886							
		887							

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TABLE III GROUP A INSPECTION

NOTES:

1. Limits established for these tests are preliminary values and are to be used only to determine range of interest. Actual value is to be measured and recorded during verification of part performance.
2. Address inputs are specified in hexadecimal. (A7 is the MSB and A0 is the LSB). Given address locations correspond to definite data patterns within this particular ACT I test ROM (see Truth Table, Figure 5, and hexadecimal address table in Figure 5.)
3. Input pins are A0 through A7, \*EN0, \*EN1, \*CS and pin connections are shown in Figures 2 and 3.
4. Outputs are D00 through D03 and \*DR. \*DR is normally low when the ROM is selected, therefore, IOH2M, VOH, VOHS and IOHS tests do not apply.
5. Changing the address states will not enter new address into the ROM. The \*EN0 must be raised from  $V_{IL} = 1.2V$  to  $V_{IH} = V_{DD} - 1.2V$  for  $T_{ED}$ , then returned to  $V_{IL}$  before the parametric measurement.
6. Output loading shall be minimum reasonably attainable, equal on all outputs. Current limits are dependent on this value and 15 pf/channel is assumed. The DC load shall be minimum, >20K, and must be disconnected during parametric output leakage tests.
7. Pattern sensitivity is not used in verification tests. Address in ascending order all addresses from 0 through FF. Use a time resolution routine which goes from 27 through 42ns in 3ns steps, 42 through 50 in 4ns steps, 50 to 80 in 5ns steps, 80 through 110 in 6ns steps, 110 through 166 in 8ns steps. Thus 26 steps covers range from 27ns through 166ns keeping resolution of access time 10% or better. Write as subroutine terminating each selected time with parametric measurement

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TABLE LII GROUP A INSPECTION

NOTES (CONTINUED)

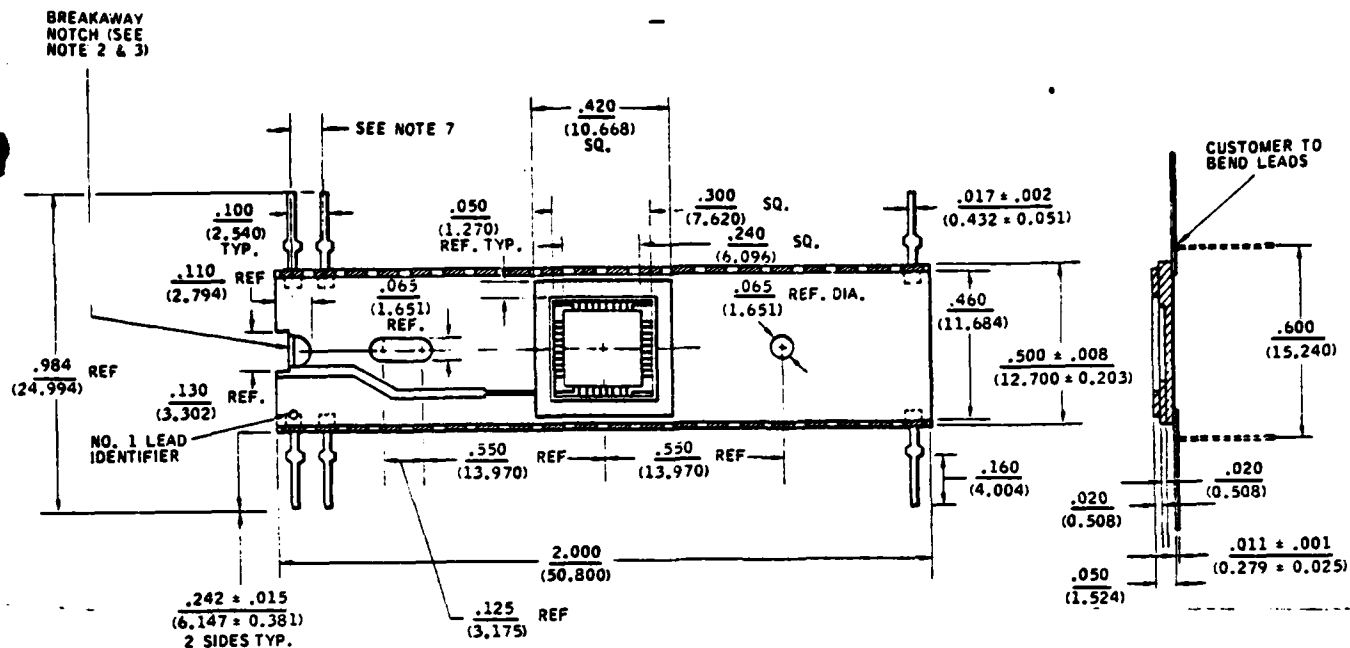
of Y6 with 270mV through 1.66 volts forced through 1.0K resistor to ground. Data log current to directly pass time results to minicomputer. This routine may be used for all time measurements.

8. Time zero is when addresses pass through 50% level, toward stable levels within following 10ns. The enable fall will occur TEN ns later after zero. The comparator error strobe position will be software corrected to measure 50% access time using comparator levels of  $V_{OL} = 0.6V$  and  $V_{OH} = V_{DD} - 0.6V$ . The transition time between the 50% level and  $V_{OL}$  will typically be about 10ns.

9. Power one channel at a time to limit current and power.

10. Small currents require at least 200ms to settle using Delay of Analogue to Digital conversion or DAD+10ms using code A (:) or B (;) in timing character of parametric statement.

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#### NOTES

1. STANDARD PACKAGE SHALL HAVE CHIP PAD AND SEAL RING ELECTRICALLY CONNECTED TO NO. 1 LEAD.
2. THE CHIP PAD SEAL RING AND NO. 1 LEAD MAY BE ELECTRICALLY ISOLATED BY MEANS OF BREAKAWAY NOTCH.
3. BREAKAWAY NOTCH IS LOCATED ON SAME LEVEL AS BONDING PADS - .020 (0.508) BELOW TOP SURFACE.
4. NO. 1 LEAD IS IDENTIFIED INSIDE CHIP PAD AREA WITH 45° NOTCH AT TERMINATION.
5. BONDING PADS .009 (0.229) ON .020 (0.508) CENTERS, EVERY FIFTH PAD PULLED BACK FOR IDENTIFICATION.
6. LEAD OFFSET FROM SIDE TO SIDE SHALL NOT EXCEED .015 (0.381) WHERE THE REFERENCE LINE IS DEFINED AS A PERPENDICULAR LINE TO THE LENGTH OF THE PACKAGE ON THE NO. 1 LEAD SIDE. THE .015 (0.381) MAXIMUM DEVIATION SHALL BE MEASURED FROM THE REFERENCE LINE AT THE SEATING PLANE.
7. LEAD ALIGNMENT FROM LEAD TO LEAD ON THE SAME SIDE SHALL BE ±.010 (±0.254) AT THE CERAMIC AND ±.005 (±0.127) AT THE TIE BAR.

#### TOLERANCES AND MATERIALS

1. TOLERANCES ±1% NOTHING LESS THAN ±.005 (0.127) UNLESS OTHERWISE SPECIFIED.
2. THICKNESS TOLERANCE: ±10% NOTHING LESS THAN ±.003 (0.076) UNLESS OTHERWISE SPECIFIED.
3. THICKNESS OF LEAD NOT CONTROLLED WITHIN .070 (1.778) OF CERAMIC DUE TO BRAZE INLAY (MINIMUM THICKNESS IN THIS AREA .0078 [0.198])
4. WIDTH AND THICKNESS OF LEAD NOT CONTROLLED WITHIN .020 (0.503) OF CERAMIC DUE TO BRAZE FILLET.
5. CERAMIC MATERIAL: (94%  $Al_2O_3$ ).
6. LEAD MATERIAL: ASTM F15 OR ASTM F30 (ALLOY 42).
7. METALLIZING: REFRACTORY METAL + NICKEL + GOLD, AS REQUIRED.
8. GOLD: TYPE III, GRADE A.
9. LEADS BRAZED TO METALLIZED CERAMIC USING COPPER-SILVER-EUTECTIC.

FIGURE 1 OUTLINE DIMENSIONS

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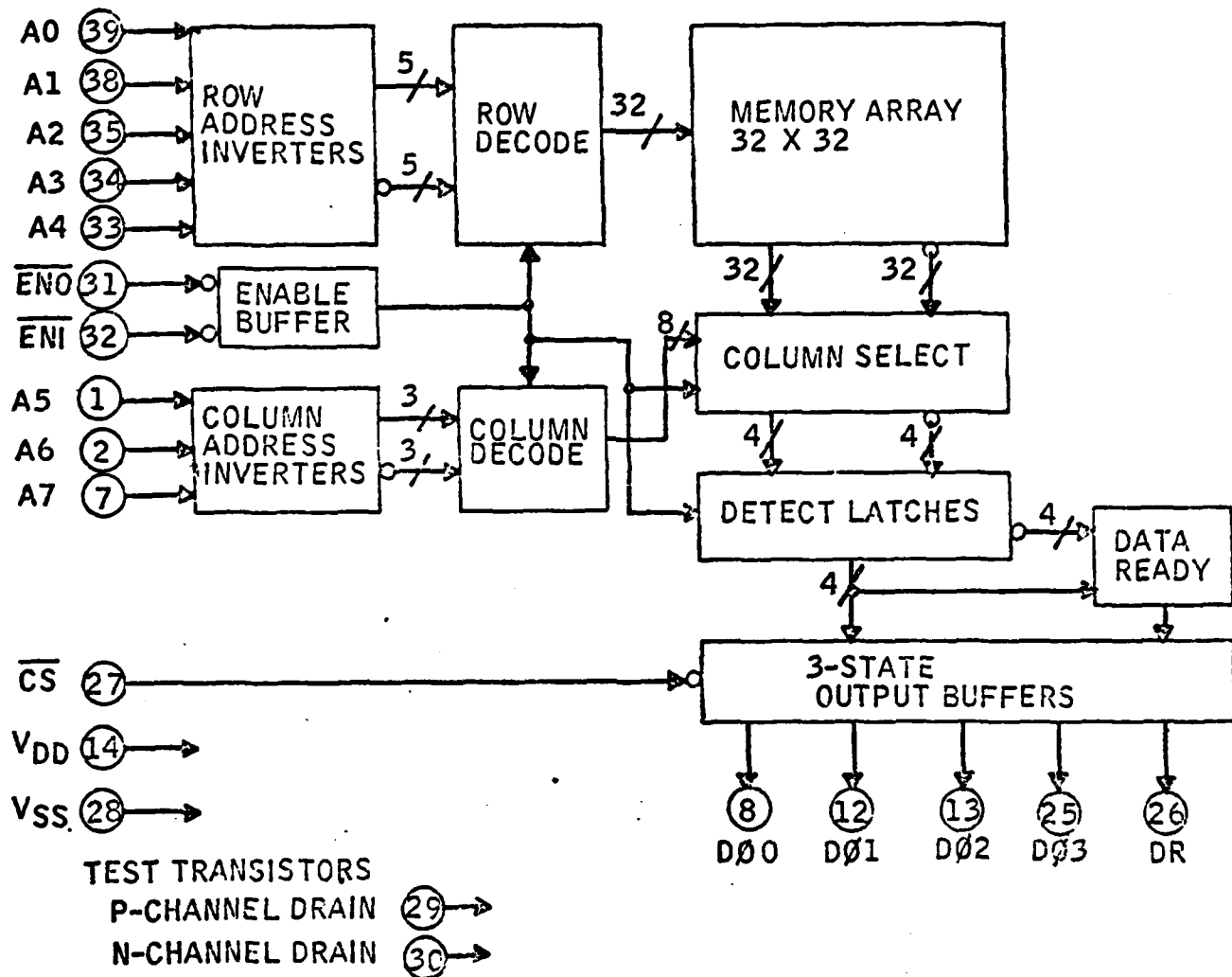


FIGURE 2 ROM BLOCK DIAGRAM

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SCALE				

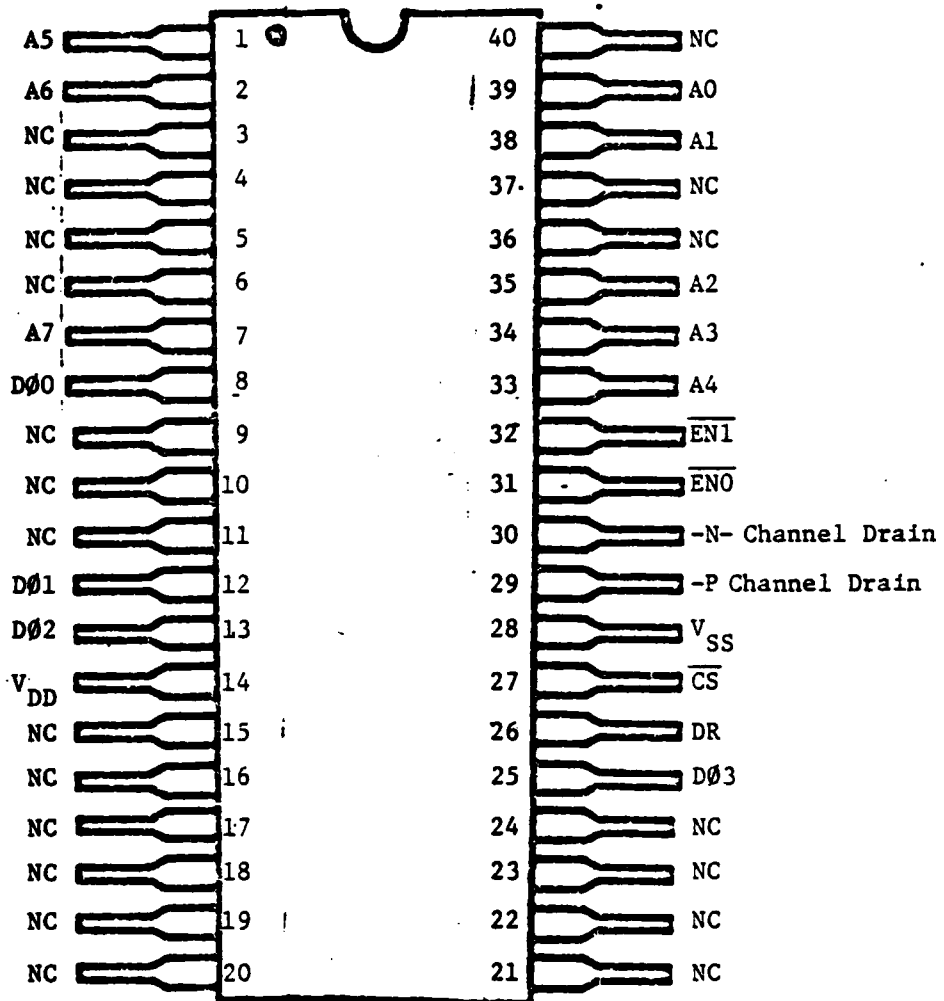


FIGURE 3 PIN CONNECTION DIAGRAM

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FIGURE 4. TYPICAL INPUT PROTECTION CIRCUIT MECHANIZATION

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SCALE				

# ACT I TEST ROM

256 X 4 ROM PATTERN

	D00								D01								D02								D03								
	0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7	
0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	} $\bar{A}_4$		
1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1				
2	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1					
3	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1					
4	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1					
5	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1					
6	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1					
7	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1					
8	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1					
9	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1					
10	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1					
11	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1					
12	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1					
13	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1					
14	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1					
15	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1					
16	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1					
17	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1					
18	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1					
19	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1					
20	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1					
21	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1					
22	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1					
23	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1					
24	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1					
25	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1					
26	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1					
27	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1					
28	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1					
29	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1					
30	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1					
31	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1					

ROW ADDRESSES  $A_0$  THRU  $A_4$

$\bar{A}_0$

$A_0$

$\bar{A}_1$

$A_1$

$\bar{A}_2$

$A_2$

$\bar{A}_3$

$A_3$

$\bar{A}_4$

$\bar{A}_5 = \text{EVEN}, A_5 = \text{ODD}$

$\bar{A}_6 A_6$

$\bar{A}_7 A_7$

FIGURE 5 TRUTH TABLE

Northrop Corporation Electronics Division Palos Verdes Peninsula, California	SIZE	CODE IDENT NO.	26760502
	A	22915	
SCALE		REV	SH 38

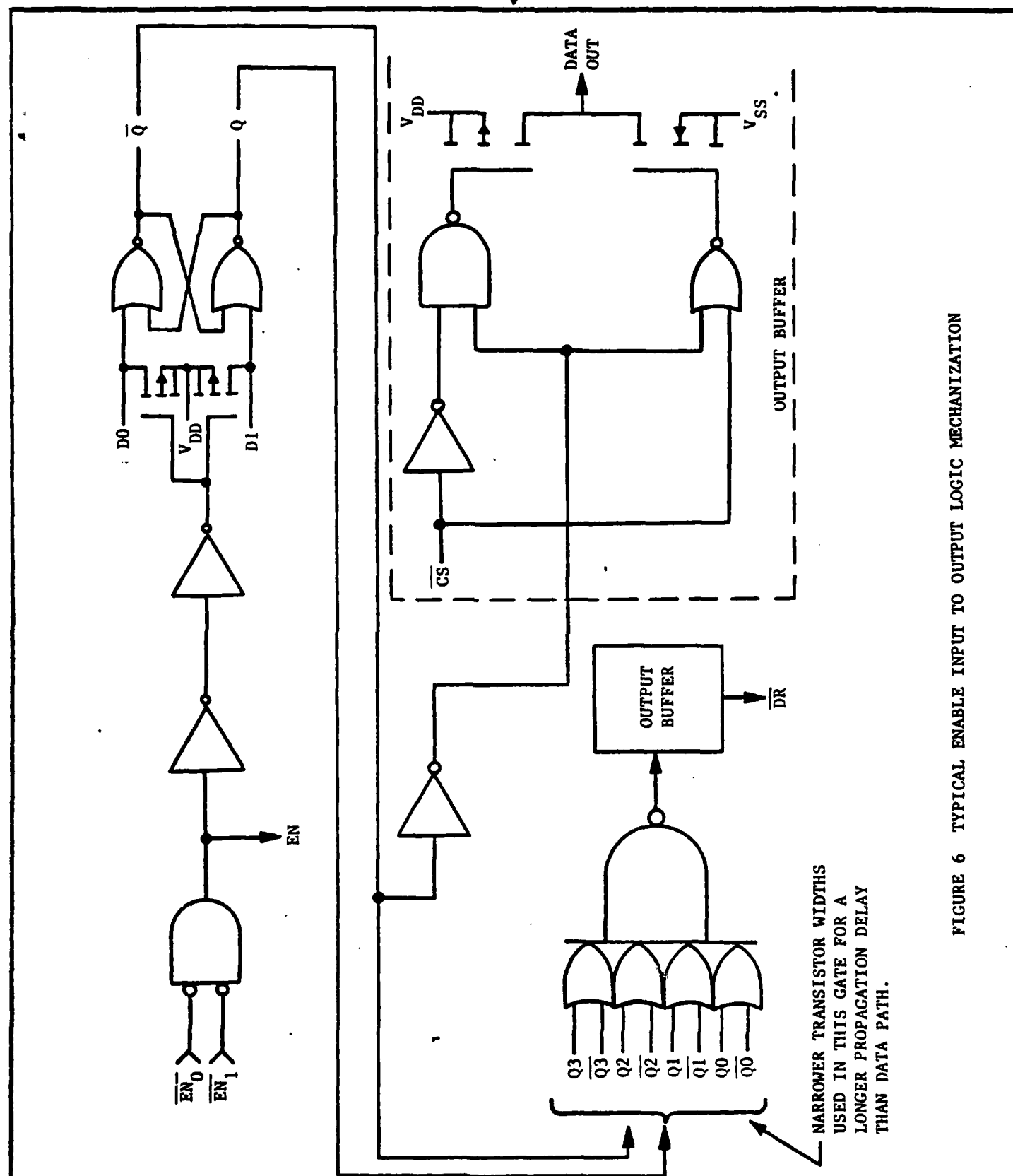


FIGURE 6 TYPICAL ENABLE INPUT TO OUTPUT LOGIC MECHANIZATION

Northrop Corporation  
Electronics Division  
Palos Verdes Peninsula, California

SIZE

A

CODE IDENT NO.

22915

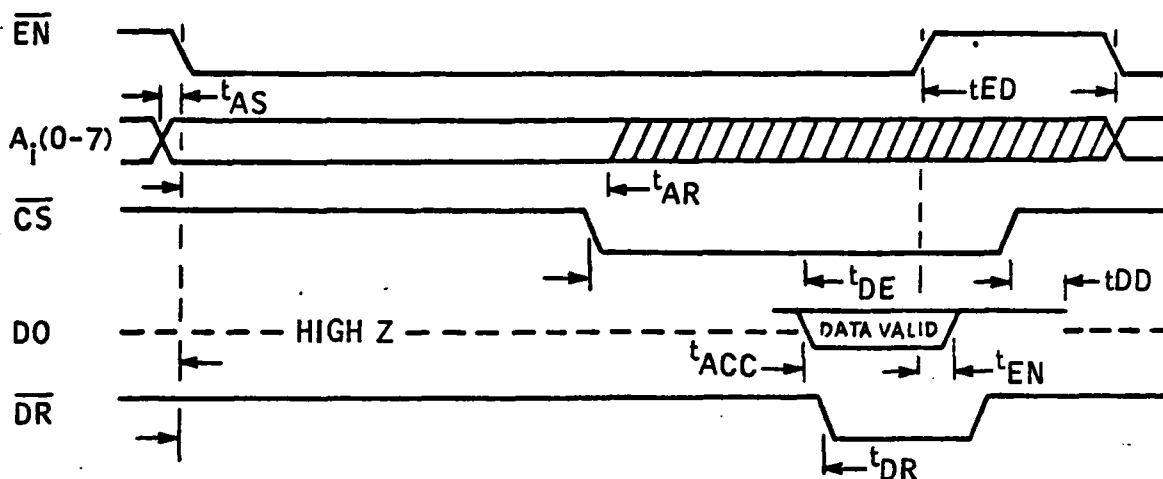
26760502

SCALE

REV

SH

39



<u>SYMBOL</u>	<u>PARAMETER OR CONDITION</u>	<u>TYPICAL DELAY TIMES</u>
$t_{AS}$	ADDRESS SETUP DELAY	40 ns MINIMUM
$t_{AR}$	ADDRESS RELEASE TIME	100 ns MINIMUM
$t_{DE}$	CS DELAY TO ENABLE DATA OUT	95 ns MAXIMUM
$t_{ACC}$	ACCESS TIME	148 ns MAXIMUM
$t_{EN}$	EN TO DATA OUT DELAY	20 ns MINIMUM
$t_{DD}$	CS DELAY TO DISABLE DATA OUT	55 ns MAXIMUM
$t_{ED}$	EN DESELECT WIDTH	40 ns MINIMUM
$t_{DR}$	DATA READY DELAY ( $t_{DR} > t_{ACC}$ )	166 ns MAXIMUM

FIGURE 7 DYNAMIC CHARACTERISTIC TIMING WAVEFORMS AND DEFINITIONS

Northrop Corporation Electronics Division Palos Verdes Peninsula, California	SIZE	CODE IDENT NO.	26760502
	A	22915	
	SCALE	REV	SH 40

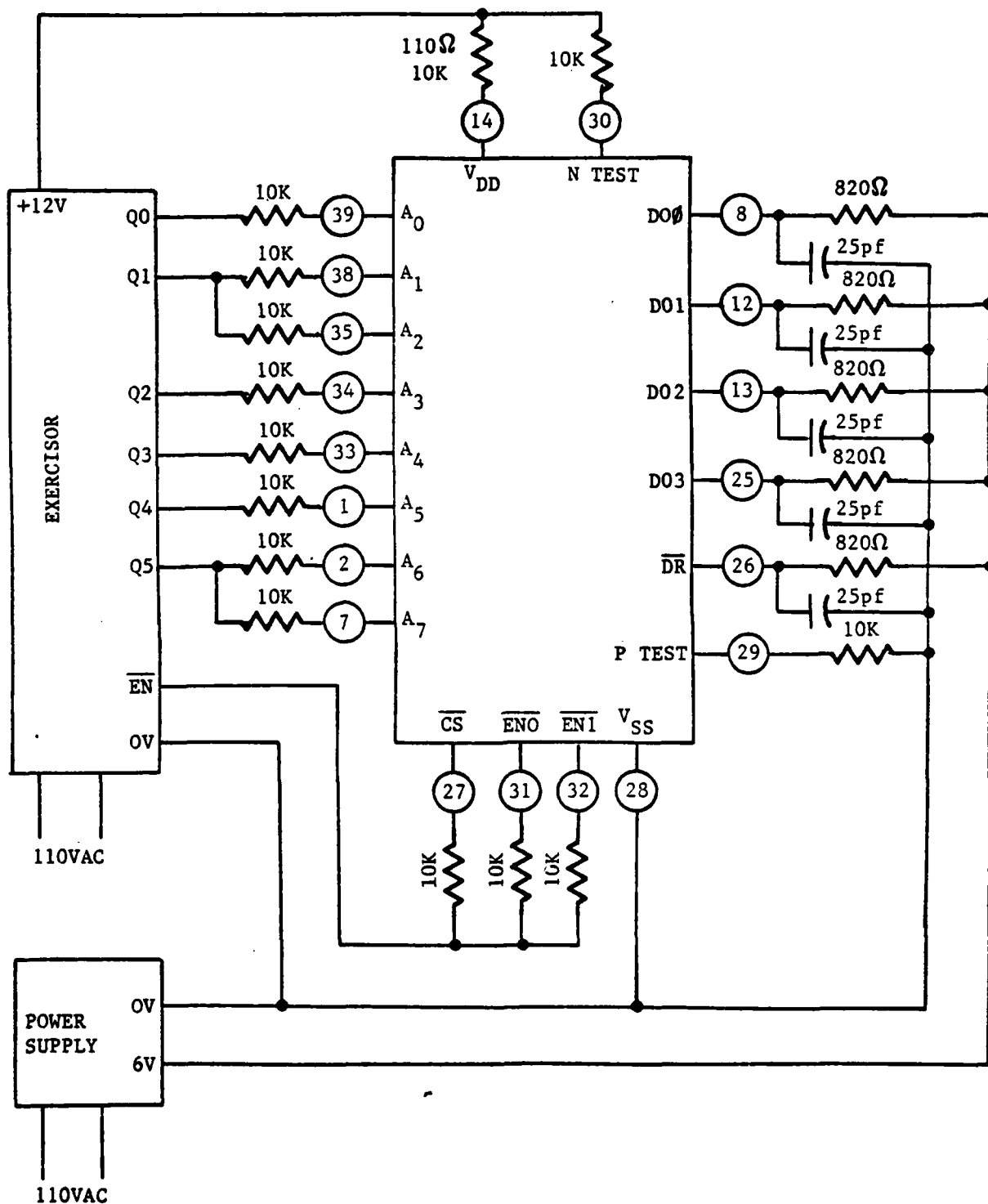


FIGURE 8A BURN-IN CIRCUIT, DYNAMIC PARALLEL

Northrop Corporation  
Electronics Division  
Palos Verdes Peninsula, California

SIZE	CODE IDENT NO.
A	22915
SCALE	REV

26760502

SH 41

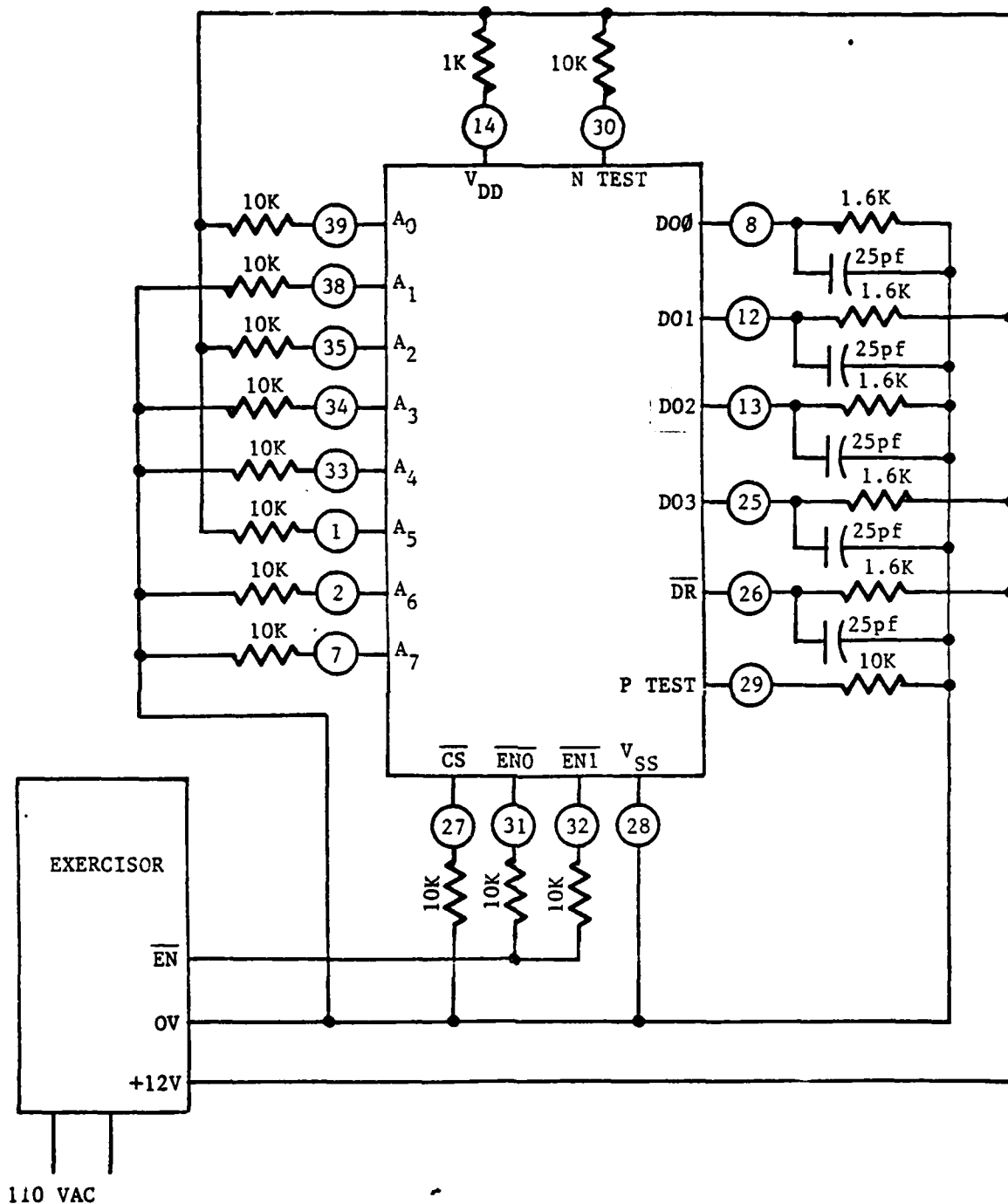


FIGURE 8B BURN-IN CIRCUIT, STATIC SELECT PARALLEL

Northrop Corporation  
Electronics Division  
Palos Verdes Peninsula, California

SIZE  
**A**  
CODE IDENT NO.  
**22915**

26760502

SCALE

REV

SH 42

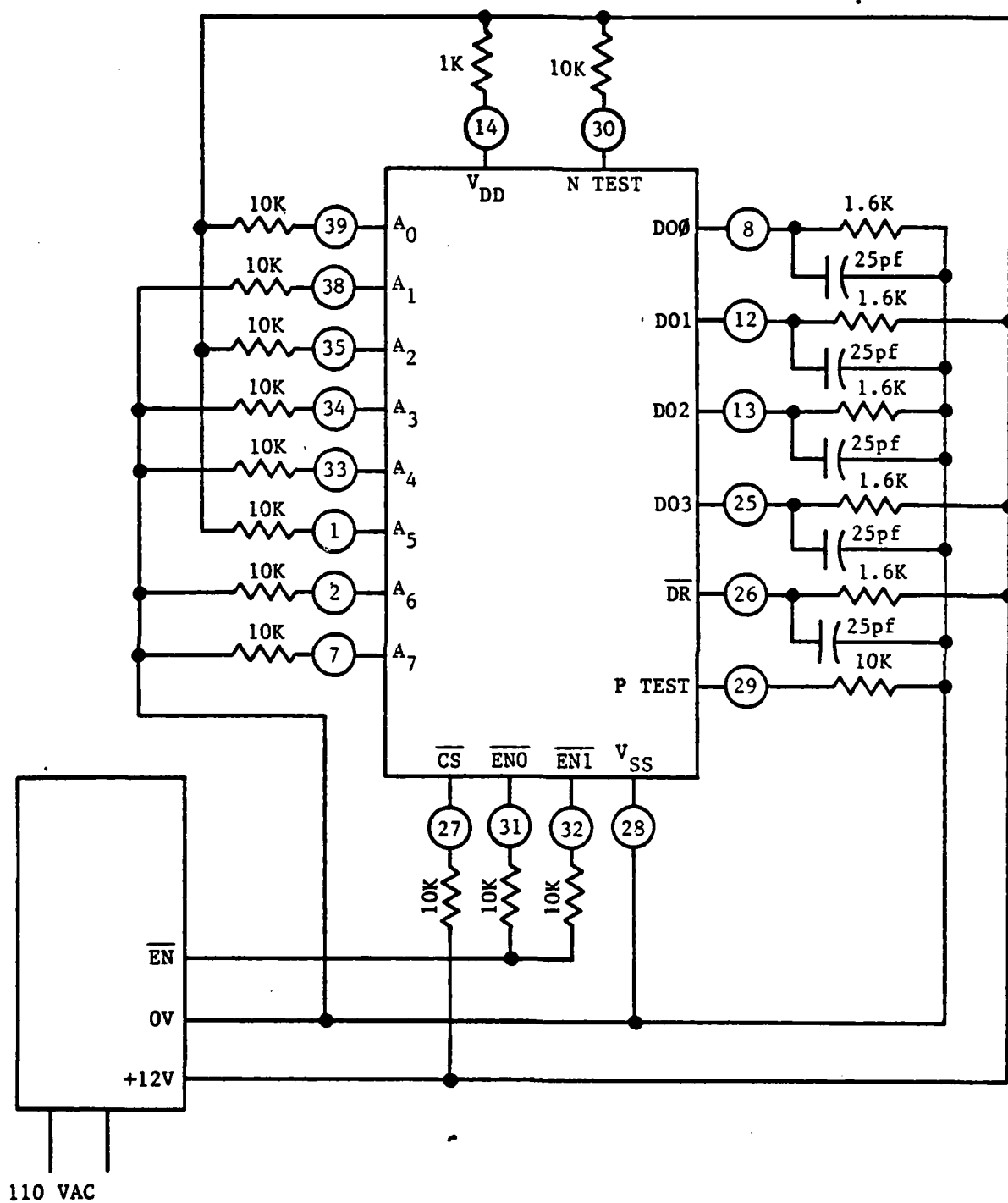


FIGURE 8C BURN-IN CIRCUIT, STATIC DESELECT PARALLEL

Northrop Corporation  
Electronics Division  
Palos Verdes Peninsula, California

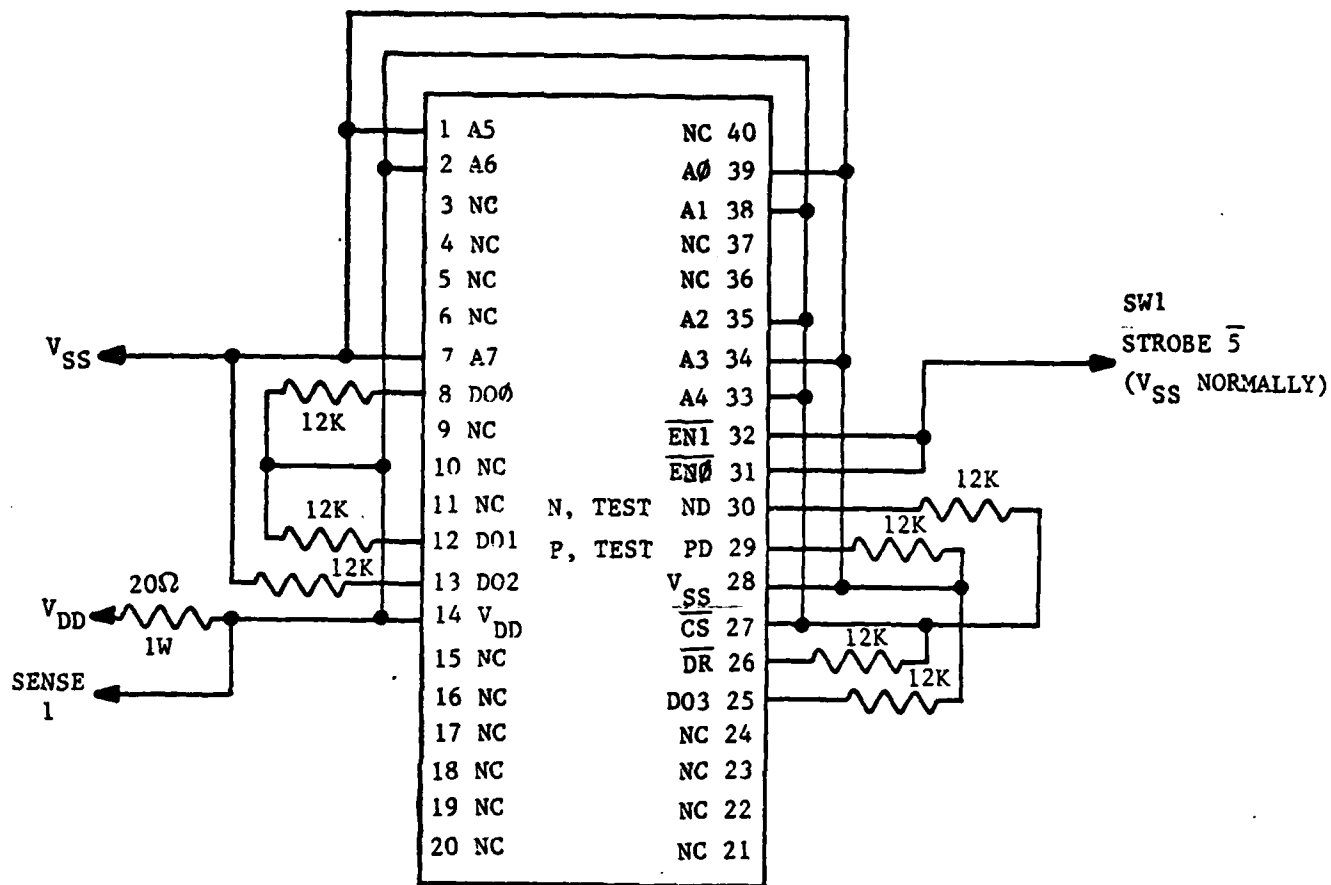
SIZE  
**A**  
SCALE

CODE IDENT NO.  
**22915**

26760502

REV

SH 43



**NOTE:**

1. ADDRESS 56
2.  $\overline{CS}$  TIED HIGH

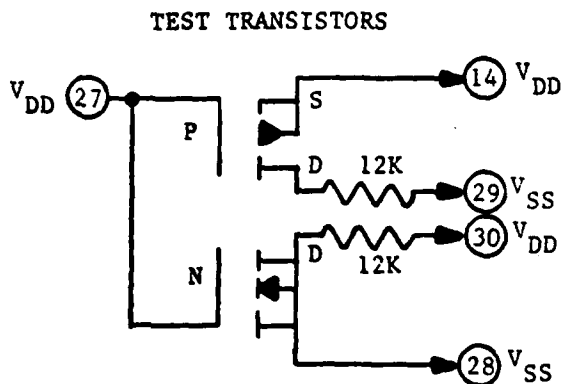


FIGURE 9A RADIATION BIAS CIRCUIT, STATIC DESELECT

Northrop Corporation  
Electronics Division  
Palos Verdes Peninsula, California

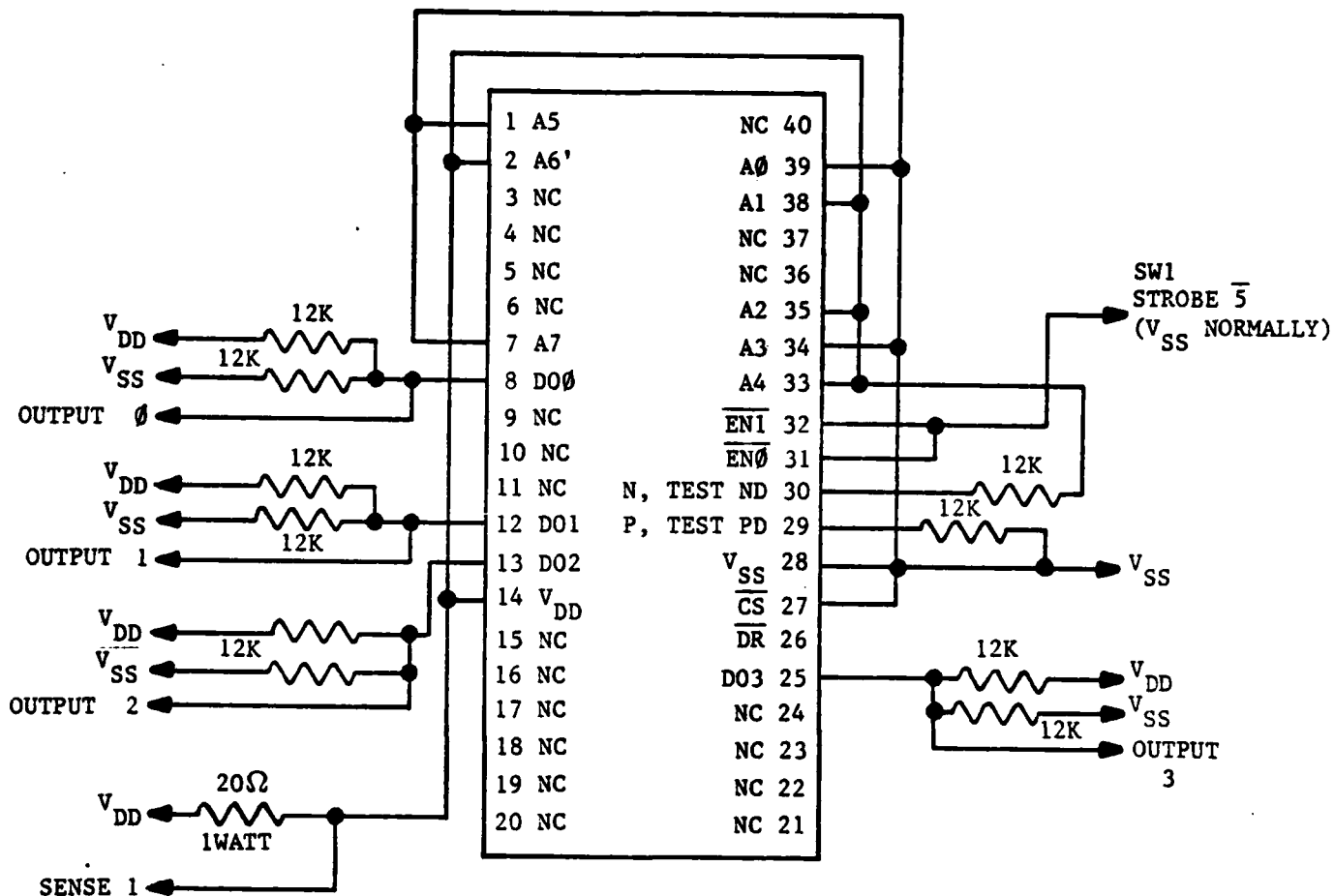
SIZE	CODE IDENT NO.
A	22915
SCALE	

26760502

REV

SH 44





**NOTE:**

1. ADDRESS 56
2. CS TIED LOW

**TEST TRANSISTORS**

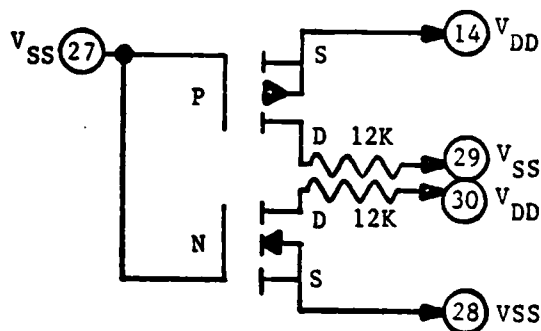


FIGURE 9B RADIATION BIAS CIRCUIT, STATIC SELECT

Northrop Corporation  
Electronics Division  
Palos Verdes Peninsula, California

SIZE

A

CODE IDENT NO.

22915

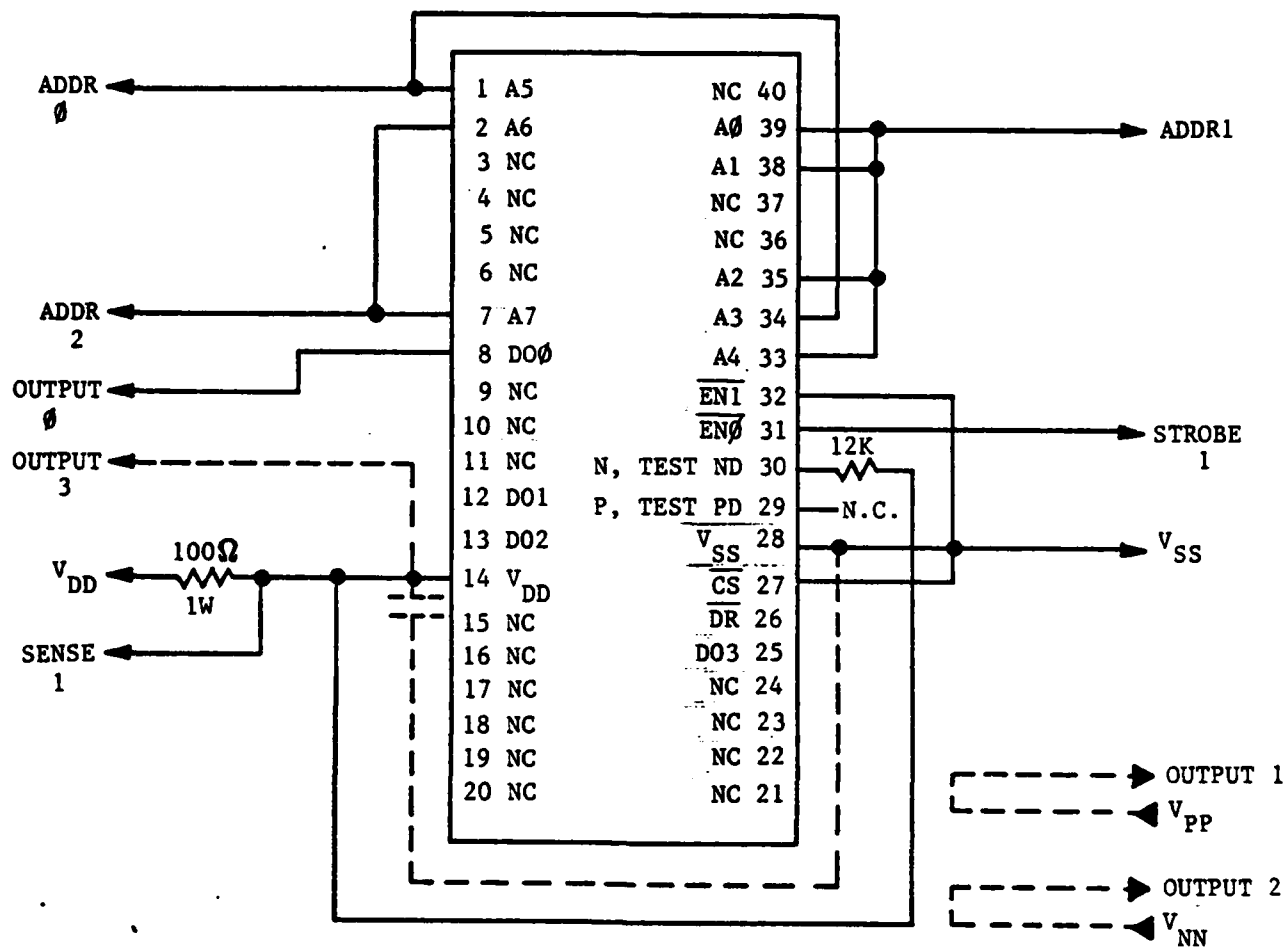
26760502

SCALE

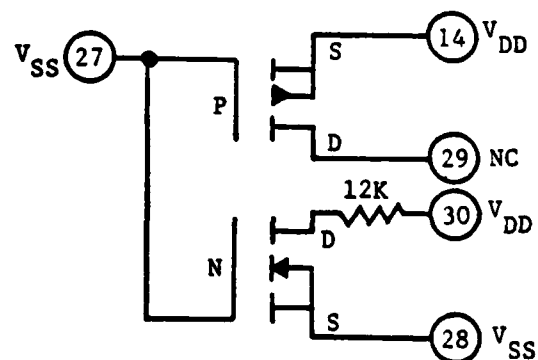
REV

SH

45



#### TEST TRANSISTORS



#### NOTE:

1. STROBES AND ADDRESSES AS PER NORTHROP RAD TEST FUTURE

FIGURE 9C RADIATION BIAS CIRCUIT, DYNAMIC

Northrop Corporation  
Electronics Division  
Palos Verdes Peninsula, California

SIZE CODE IDENT NO.  
A 22915

26760502

SCALE

REV

SH 46

**SUGGESTED SOURCES OF SUPPLY**

NORTHROP PART NUMBER	VENDOR		
	NAME AND ADDRESS	CODE IDENT NO.	VENDOR PART NO.
2676-0502	Westinghouse Electric Corp. Systems Development Division Baltimore, MD 21203	97942	4028-C-58

Northrop Corporation Electronics Division Palos Verdes Peninsula, California	SIZE	CODE IDENT NO.	26760502
	A	22915	
SCALE		REV	SH 47

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